

NFCS1060L3TT

2-in-1 PFC and Inverter Intelligent Power Module (IPM), 600 V, 10 A

The NFCS1060L3TT is a fully-integrated PFC and inverter power stage consisting of a high-voltage driver, six motor drive IGBT's, one PFC SJ-MOSFET, one PFC SiC-SBD for rectifier and a thermistor, suitable for driving permanent magnet synchronous (PMSM) motors, brushless-DC (BLDC) motors and AC asynchronous motors.

The IGBT's are configured in a 3-phase bridge with separate emitter connections for the lower legs for maximum flexibility in the choice of control algorithm.

An internal comparator and reference connected to the over-current protection circuit allows the designer to set individual over-current protection levels for the PFC and the inverter stages. Additionally, the power stage has a full range of protection functions including cross-conduction protection, external shutdown and under-voltage lockout functions.

Features

- Simple Thermal Design with PFC and Inverter Stage in One Package
- Cross-Conduction Protection
- Integrated Bootstrap Diodes and Resistors
- UL1577 Certification (File Number: E339285)

Typical Applications

- Heat Pumps
- Home Appliances
- Industrial Fans
- Industrial Pumps

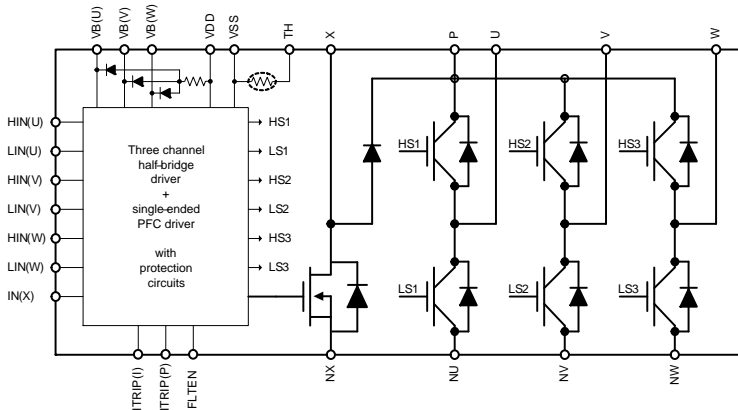
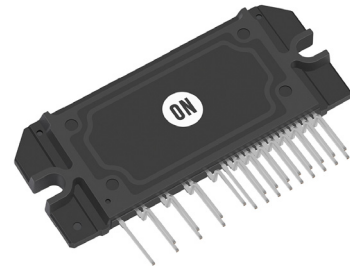


Figure 1. Function Diagram



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SIP35 56x25.8 / SIP2A-2
CASE 127DT

MARKING DIAGRAM



NFCS1060L3TT = Specific Device Code
 ZZZ = Assembly Lot Code
 A = Assembly Location
 T = Test Location
 Y = Year
 WW = Work Week
 Device marking is on package top side

ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|--------------|-----------------------------------|--------------------------|
| NFCS1060L3TT | SIP35 56x25.8 / SIP2A-2 (Pb-Free) | 8 / Tube |

NFCS1060L3TT

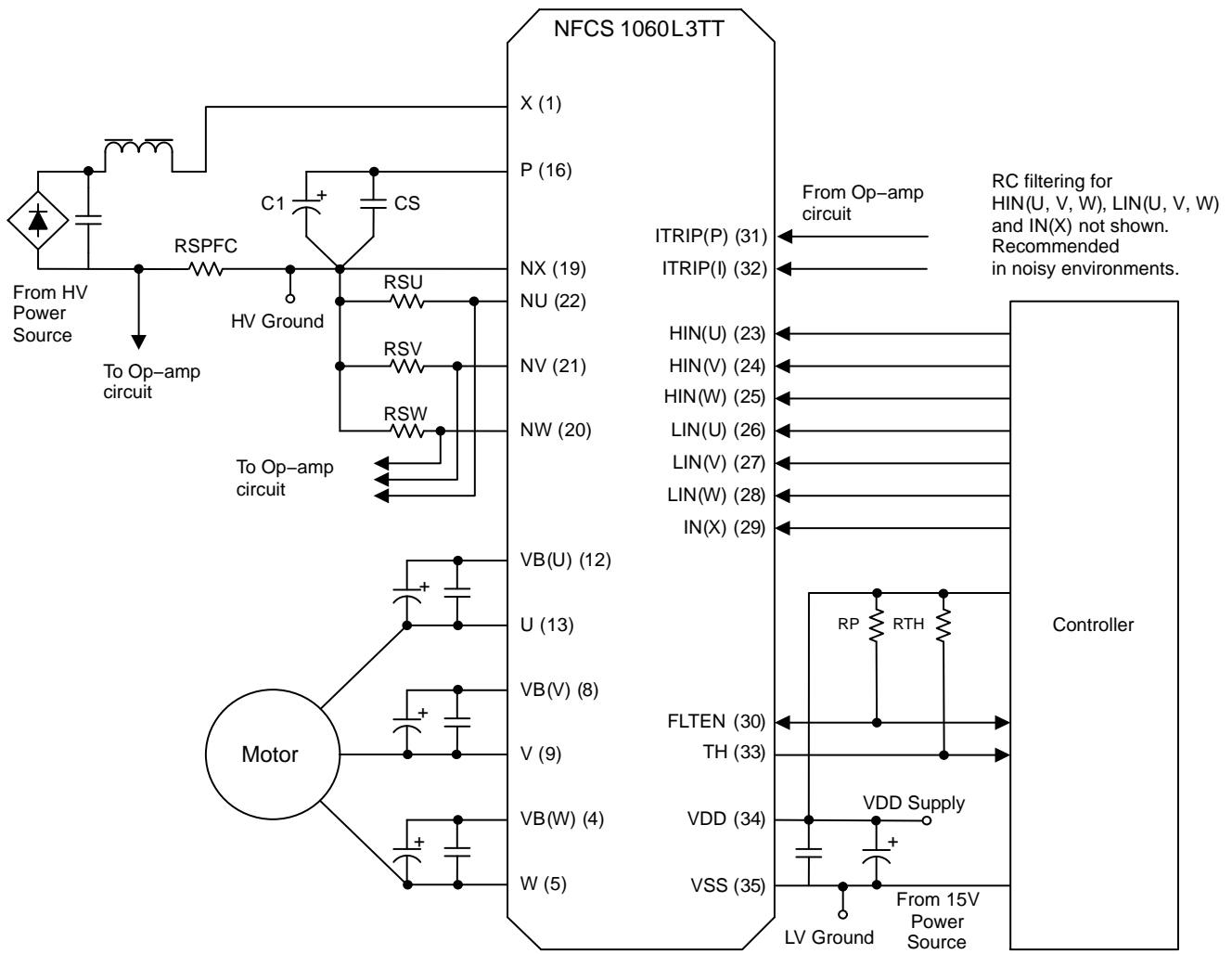


Figure 2. Application Schematic – Adjustable Option

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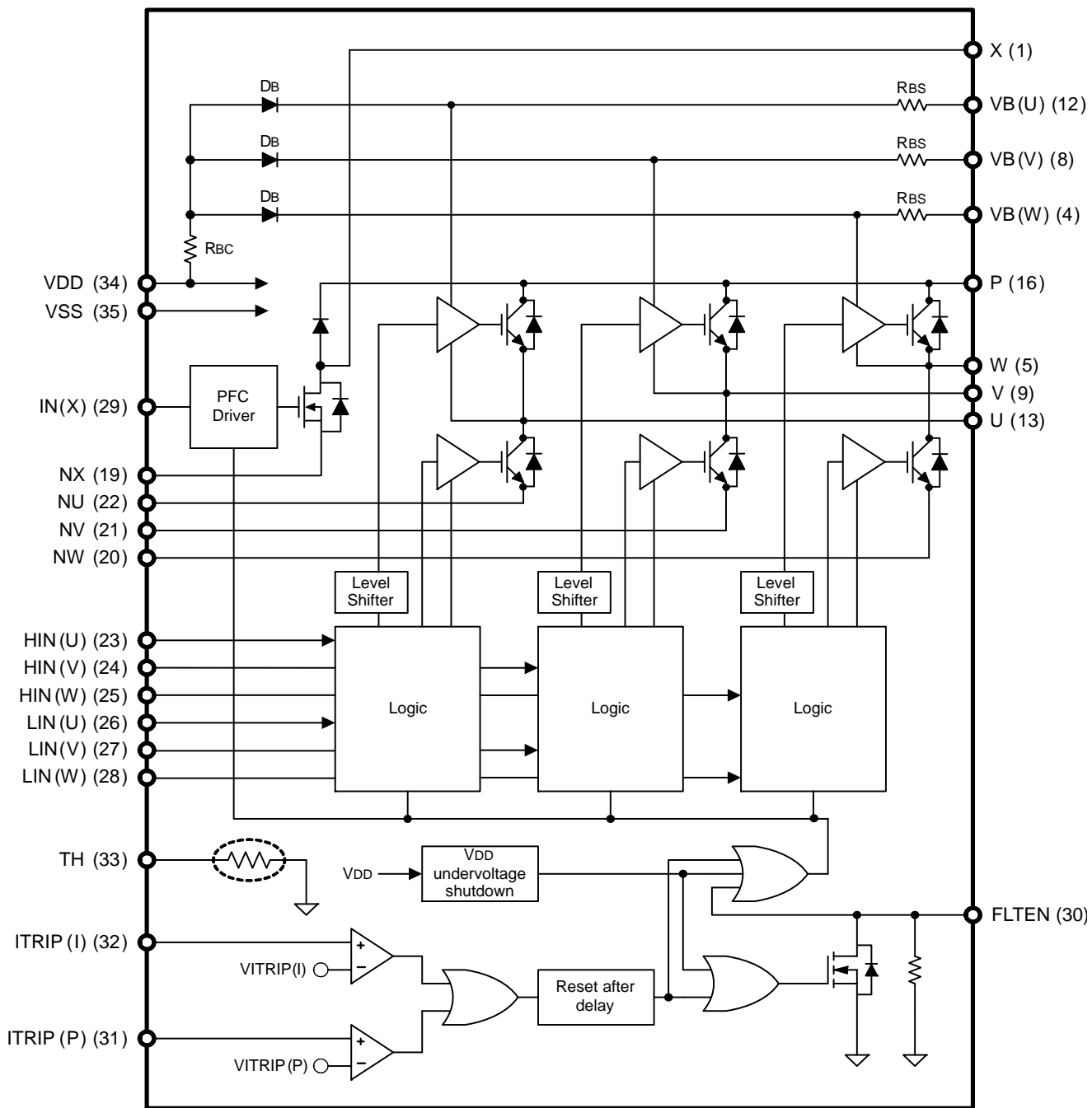


Figure 3. Equivalent Block Diagram

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Table 1. PIN FUNCTION DESCRIPTION

| Pin | Name | Description |
|-----|----------|--|
| 1 | X | X Phase MOSFET Drain for PFC Inductor Connection |
| 4 | VB(W) | High-Side Bias Voltage for W Phase IGBT Driving |
| 5 | W | Output for W Phase and High-Side Bias Voltage GND for W Phase IGBT Driving |
| 8 | VB(V) | High-Side Bias Voltage for V Phase IGBT Driving |
| 9 | V | Output for V Phase and High-Side Bias Voltage GND for V Phase IGBT Driving |
| 12 | VB(U) | High-Side Bias Voltage for U Phase IGBT Driving |
| 13 | U | Output for U Phase and High-Side Bias Voltage GND for U Phase IGBT Driving |
| 16 | P | Positive DC-Link Input / Positive PFC Output Voltage |
| 19 | NX | X Phase MOSFET Source for PFC |
| 20 | NW | Negative DC-Link Input for W Phase |
| 21 | NV | Negative DC-Link Input for V Phase |
| 22 | NU | Negative DC-Link Input for U Phase |
| 23 | HIN(U) | Signal Input for High-Side U Phase |
| 24 | HIN(V) | Signal Input for High-Side V Phase |
| 25 | HIN(W) | Signal Input for High-Side W Phase |
| 26 | LIN(U) | Signal Input for Low-Side U Phase |
| 27 | LIN(V) | Signal Input for Low-Side V Phase |
| 28 | LIN(W) | Signal Input for Low-Side W Phase |
| 29 | IN(X) | Signal Input for PFC X Phase |
| 30 | FLTEN | Fault Output / Enable |
| 31 | ITRIP(P) | Input for Current Protection for PFC |
| 32 | ITRIP(I) | Input for Current Protection for Inverter |
| 33 | TH | Thermistor Bias Voltage |
| 34 | VDD | Low-Side Bias Voltage for IC and IGBTs Driving |
| 35 | VSS | Low-Side Common Supply Ground |

NOTE: Pins 2, 3, 6, 7, 10, 11, 14, 15, 17 and 18 are not present.

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Table 2. ABSOLUTE MAXIMUM RATINGS (Note 1)

T_C = 25°C unless otherwise noted

| Rating | Symbol | Conditions | Value | Unit | |
|---------------------------------|----------------------------|------------|--|------|------|
| PFC Section | | | | | |
| PFC MOSFET | Drain–Source Voltage | VDSS | X – NX | 600 | V |
| | Drain Current (peak) | IDP | Pulse Width < 100 ms, VBS, VDD = 15 V | 30 | A |
| | Drain Current | ID | T _C = 25 °C | 20 | A |
| | | | T _C = 100 °C | 10 | A |
| Power Dissipation | PD1 | | 83 | W | |
| PFC Diode | Repetitive Reverse Voltage | VRRM | P – X | 600 | V |
| | Forward Current (peak) | IFP | Pulse Width < 100 ms | 30 | A |
| | Forward Current | IF | T _C = 25 °C | 20 | A |
| | | | T _C = 100 °C | 10 | A |
| Power Dissipation | PD2 | | 32 | W | |
| MOSFET Body Diode | Forward Current | ISD | T _C = 25 °C | 10 | A |
| Maximum AC Input Voltage | | VAC | Single–Phase Full–Rectified | 277 | Vrms |
| Maximum Output Voltage | | Vo | In the Application Circuit (VAC = 200 V) | 450 | V |
| Input AC Current (steady state) | | Iin | | 10 | Arms |

Inverter Section

| | | | | |
|------------------------------------|------|--|-----|---|
| Supply Voltage | VPN | P – NU, NV, NW surge < 500 V (Note 2) | 450 | V |
| Collector–Emitter Voltage | VCES | P – U, V, W or U – NU, V – NV, W – NW | 600 | V |
| Each IGBT Collector Current | IC | P, U, V, W, NU, NV, NW Terminal Current | ±10 | A |
| | | P, U, V, W, NU, NV, NW Terminal Current at T _C = 100 °C | ±5 | A |
| Each IGBT Collector Current (peak) | ICP | P, U, V, W, NU, NV, NW Terminal Current, Pulse Width 1 ms | ±20 | A |
| Corrector Dissipation | PC | IGBT per one chip | 29 | W |

Driver Section

| | | | | |
|--|-----------|---|---------------|---|
| High–Side Control Bias Voltage | VBS | VB(U) – U, VB(V) – V, VB(W) – W, | –0.3 to +20.0 | V |
| Control Supply Voltage | VDD | VDD – VSS | –0.3 to +20.0 | V |
| Input Signal Voltage | VIN | HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W), IN(X) | –0.3 to VDD | V |
| Fault Output Supply Voltage and Enable Input | VFLTEN | FLTEN Terminal | –0.3 to VDD | V |
| ITRIP(I) Terminal Voltage | VITRIP(I) | ITRIP(I) Terminal | 0.3 to +10.0 | V |
| ITRIP(P) Terminal Voltage | VITRIP(P) | ITRIP(P) Terminal | 1.5 to +2.0 | V |

Intelligent Power Module Total

| | | | | |
|-----------------------------------|------------------|---|-------------|------|
| Operating Junction Temperature | T _j | | 150 | °C |
| Storage Temperature | T _{stg} | | –40 to +125 | °C |
| Module Case Operation Temperature | T _c | IPM Case Temperature | 40 to +100 | °C |
| Tightening Torque | MT | Case Mounting Screws | 0.9 | Nm |
| Isolation Voltage | Viso | 60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate (Note 4) | 2000 | Vrms |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters
2. This surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminals.
3. VBS = VB(U) – U, VB(V) – V, VB(W) – W
4. Test conditions : AC 2500 V, 1 sec

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Table 3. THERMAL CHARACTERISTICS

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|------------|-------------------------------------|-----|-----|-----|------|
| Junction to Case Thermal Resistance | Rth(j-c) M | PFC MOSFET | – | 1.3 | 1.5 | °C/W |
| | Rth(j-c) R | PFC Diode | – | 3.2 | 3.9 | °C/W |
| | Rth(j-c) Q | Inverter IGBT Part (per 1/6 Module) | – | 3.5 | 4.2 | °C/W |
| | Rth(j-c) F | Inverter FRD Part (per 1/6 Module) | – | 6.8 | 8.2 | °C/W |

5. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters

Table 4. RECOMMENDED OPERATING RANGES

| Rating | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------|---|------|-----|------|------|
| Supply Voltage | VPN | P – NX, NU, NV, NW | 0 | 280 | 400 | V |
| High-Side Control Bias Voltage | VBS | VB(U) – U, VB(V) – V, VB(W) – W | 13.0 | 15 | 17.5 | V |
| Control Supply Voltage | VDD | VDD – VSS (see table note below) | 14.0 | 15 | 16.5 | V |
| ON Threshold Voltage | VIN(ON) | HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W), IN(X) | 2.5 | – | 5.0 | V |
| OFF Threshold Voltage | VIN(OFF) | | 0 | – | 0.3 | V |
| PWM Frequency (PFC) | fPWMp | | 1 | – | 125 | kHz |
| | | No load, Duty = 0.5, Tc = 25 °C | 1 | – | 300 | kHz |
| PWM Frequency (Inverter) | fPWMi | | 1 | – | 20 | kHz |
| Dead Time | DT | Turn-off to Turn-on (external) | 1 | – | – | µs |
| Allowable Input Pulse Width | PWIN | ON and OFF | 1 | – | – | µs |
| Tightening Torque | | 'M3' Type Screw | 0.6 | – | 0.9 | Nm |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 5. ELECTRICAL CHARACTERISTICS

T_C = 25 °C, VBIAS (VBS, VDD) = 15 V unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|-----------|-----------------|--------|-----|-----|-----|------|
|-----------|-----------------|--------|-----|-----|-----|------|

PFC Section

| | | | | | | |
|-------------------------------------|------------------------------------|---------|---|-------|------|----|
| Drain-Source Leakage Current | VDSS = 600 V | IDSS | – | – | 100 | µA |
| Reverse Leakage Current (PFC Diode) | VRRM = 600 V | IR | – | – | 500 | µA |
| Drain-Source On Resistance | ID = 20 A, Tj = 25 °C | RDS(on) | – | 0.125 | 0.18 | Ω |
| | ID = 10 A, Tj = 100 °C | | – | 0.23 | – | Ω |
| Diode Forward Voltage (PFC Diode) | IF = 20 A, Tj = 25 °C | VF | – | 1.85 | 2.6 | V |
| | IF = 10 A, Tj = 100 °C | | – | 1.55 | – | V |
| MOSFET Body Diode Forward Voltage | IF = 10 A, Tj = 25 °C | VSD | – | 1.0 | 1.5 | V |
| Switching Time | ID = 20 A, VPN = 300 V, Tj = 25 °C | ton | – | 0.4 | 0.9 | µs |
| | | toff | – | 0.6 | 1.1 | µs |

Inverter Section

| | | | | | | |
|--------------------------------------|------------------------------------|----------|---|-----|------|----|
| Collector-Emitter Leakage Current | VCES = 600 V | ICES | – | – | 100 | µA |
| Bootstrap Diode Leakage Current | VRRM(DB) = 600 V | IR(DB) | – | – | 100 | µA |
| Collector-Emitter Saturation Voltage | IC = 10 A, Tj = 25 °C | VCE(sat) | – | 2.0 | 2.65 | V |
| | IC = 5 A, Tj = 100 °C | | – | 1.7 | – | V |
| FWDi Forward Voltage | IF = 10 A, Tj = 25 °C | VF | – | 1.8 | 2.4 | V |
| | IF = 5 A, Tj = 100 °C | | – | 1.4 | – | V |
| Switching Times | IC = 10 A, VPN = 300 V, Tj = 25 °C | ton | – | 0.5 | 1.0 | µs |
| | | toff | – | 0.6 | 1.1 | µs |

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Table 5. ELECTRICAL CHARACTERISTICS (continued)

T_C = 25 °C, VBIAS (VBS, VDD) = 15 V unless otherwise noted.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|------------------------------------|--|------------------|-------------|-----|-----|------|
| Turn-on Switching Loss | IC = 10 A, VPN = 300 V, T _j = 25 °C | E _{ON} | – | 295 | – | μJ |
| Turn-off Switching Loss | | E _{OFF} | – | 155 | – | μJ |
| Total Switching Loss | | E _{TOT} | – | 450 | – | μJ |
| Turn-on Switching Loss | IC = 5 A, VPN = 300 V, T _j = 100 °C | E _{ON} | – | 195 | – | μJ |
| Turn-off Switching Loss | | E _{OFF} | – | 115 | – | μJ |
| Total Switching Loss | | E _{TOT} | – | 310 | – | μJ |
| Diode Reverse Recovery Energy | IC = 5 A, VPN = 300 V, T _j = 100 °C | E _{REC} | – | 50 | – | μJ |
| Diode Reverse Recovery Time | | trr | – | 200 | – | ns |
| Reverse Bias Safe Operating Area | IC = 20 A, VCES = 450 V | RBSOA | Full Square | | | – |
| Short Circuit Safe Operating Area | VCES = 400 V, T _j = 150 °C | SCSOA | 5 | – | – | μs |
| Allowable Offset Voltage Slew Rate | U – NU, V – NV, W – NW | dv/dt | –50 | – | 50 | V/ns |

Driver Section

| | | | | | | |
|--|--|-----------------------|------|-------|-------|----|
| Quiescent VBS Supply Current | VBS = 15 V, per driver | IQBS | – | 0.08 | 0.4 | mA |
| Quiescent VDD Supply Current | VDD = 15 V | IQDD | – | 0.85 | 2.4 | mA |
| ON Threshold Voltage | HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W), IN(X) – VSS | VIN(ON) | 2.5 | – | – | V |
| OFF Threshold Voltage | | VIN(OFF) | – | – | 0.8 | V |
| Logic Input Current | VIN = +3.3 V | I _{IN+} | – | 100 | 143 | μA |
| Logic Input Current | VIN = 0 V | I _{IN–} | – | – | 2 | μA |
| Bootstrap Diode Forward Voltage | IF(DB) = 0.1 A | VF(DB) | – | 0.8 | – | V |
| Bootstrap Circuit Resistance | Resistor Value for Common Boot Charge Line | RBC | – | 2 | – | Ω |
| | Resistor Values for Separate Boot Charge Lines | RBS | – | 10 | – | Ω |
| FLTEN Terminal Sink Current | VFLTEN : ON / VFAULT = 0.1 V | I _{oSD} | – | 2 | – | mA |
| FLTEN Output Pulse Width | | t _{FO} | 1.0 | – | 3.0 | ms |
| FLTEN Threshold | VEN ON–state Voltage | VEN(ON) | 2.5 | – | – | V |
| | VEN OFF–state Voltage | VEN(OFF) | – | – | 0.8 | V |
| ITRIP(I) Threshold Voltage | ITRIP(I) – VSS | VITRIPth(I) | 0.44 | 0.49 | 0.54 | V |
| ITRIP(P) Threshold Voltage | ITRIP(P) – VSS | VITRIPth(P) | 0.37 | –0.31 | –0.25 | V |
| Shutdown Propagation Delay for INV | | t _{ITRIP(I)} | 490 | 600 | 850 | ns |
| Shutdown Propagation Delay for PFC | | t _{ITRIP(P)} | 440 | 550 | 800 | ns |
| ITRIP Blanking Time | | t _{ITRIPBL} | 290 | 350 | – | ns |
| Supply Circuit Under–voltage Protection | Reset Level | UVBSR UVDDR | 10.5 | 11.1 | 11.7 | V |
| Supply Circuit Under–voltage Protection | Detection Level | UVBSD UVDDD | 10.3 | 10.9 | 11.5 | V |
| Supply Circuit Under–voltage Protection Hysteresis | | UVBSHYS UVDDHYS | 0.14 | 0.2 | – | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – PFC SECTION

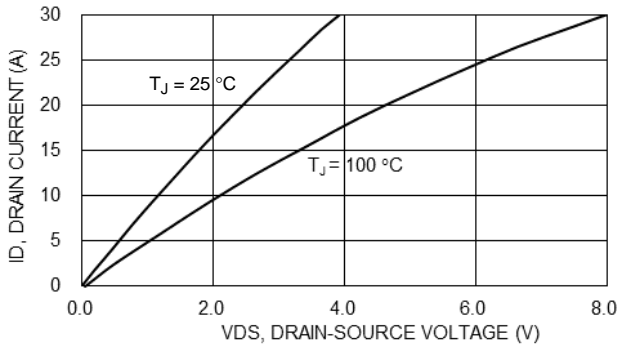


Figure 4. VDS versus ID for Different Temperatures (VDD = 15 V)

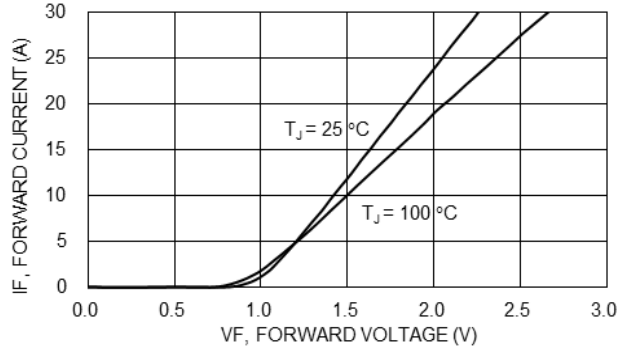


Figure 5. PFC Diode VF versus IF for Different Temperatures

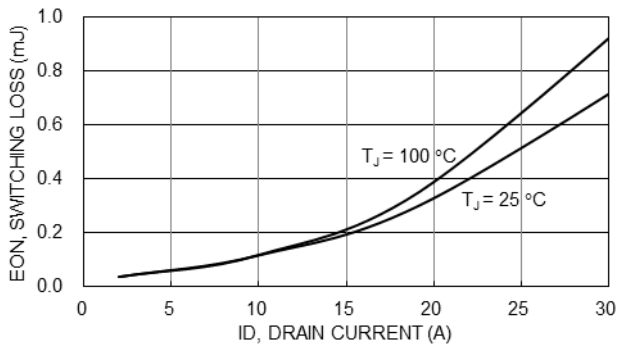


Figure 6. EON versus ID for Different Temperatures

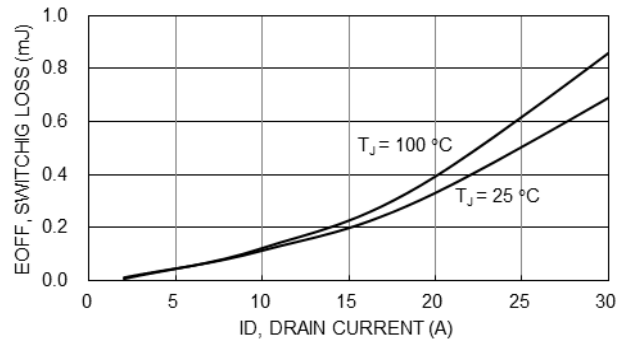


Figure 7. EOFF versus ID for Different Temperatures

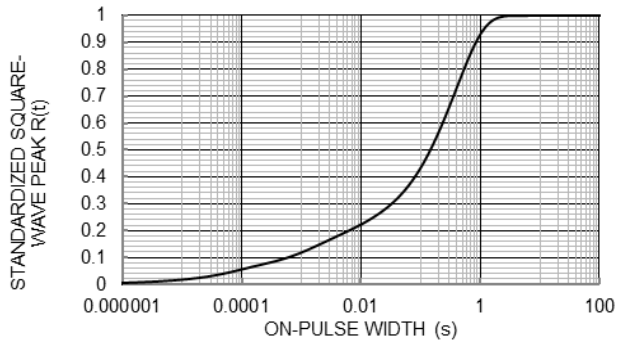


Figure 8. Thermal Impedance Plot (PFC MOSFET)

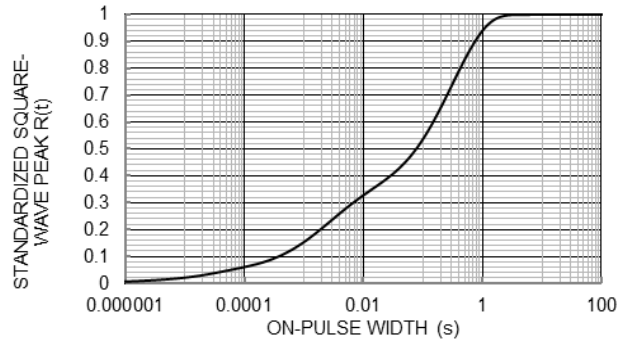


Figure 9. Thermal Impedance Plot (PFC Diode)

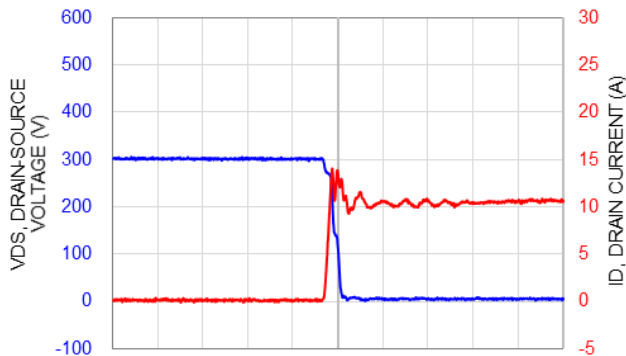


Figure 10. Turn-on Waveform Tj = 100°C, VPN = 300 V

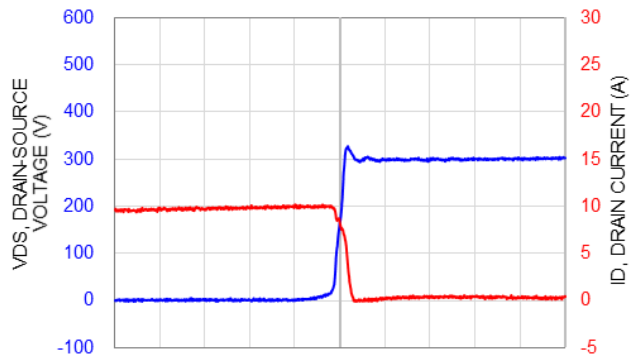


Figure 11. Turn-off Waveform Tj = 100°C, VPN = 300 V

TYPICAL CHARACTERISTICS – INVERTER SECTION

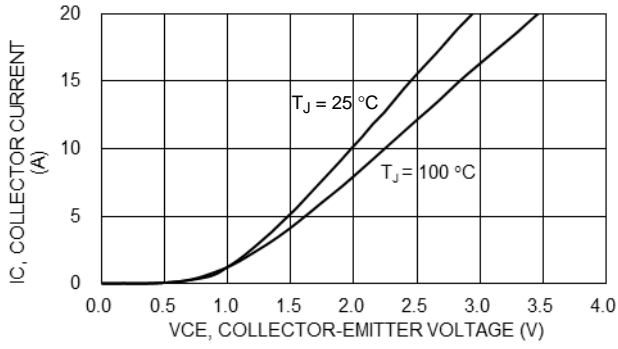


Figure 12. VCE versus IC for Different Temperatures (VDD/VBS = 15 V)

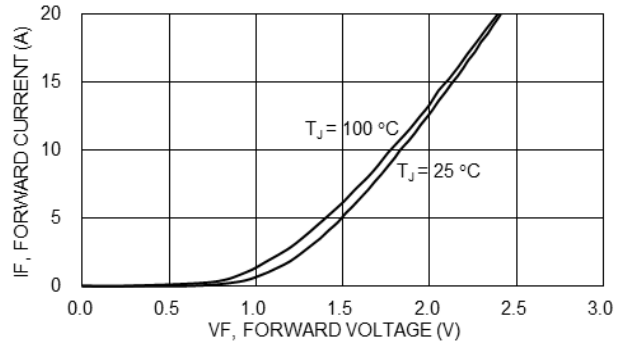


Figure 13. VF versus IF for Different Temperatures

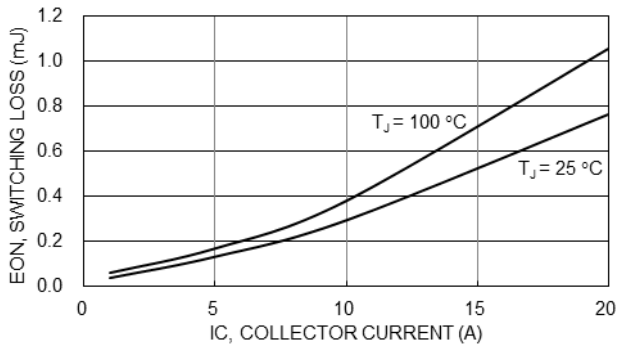


Figure 14. EON versus IC for Different Temperatures

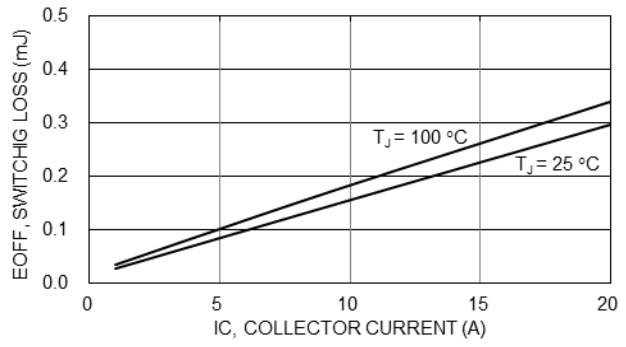


Figure 15. EOFF versus IC for Different Temperatures

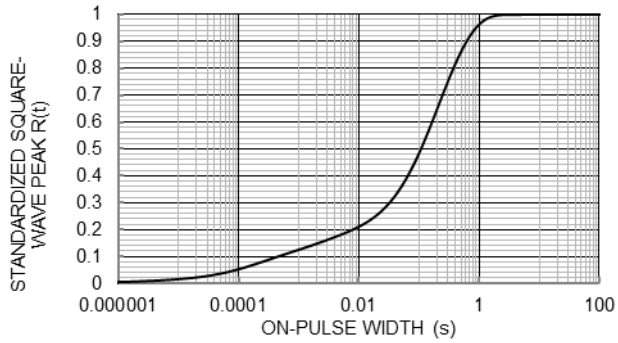


Figure 16. Thermal Impedance Plot (IGBT)

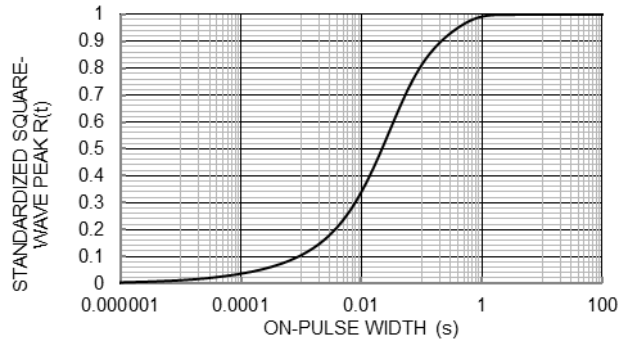


Figure 17. Thermal Impedance Plot (FRD)

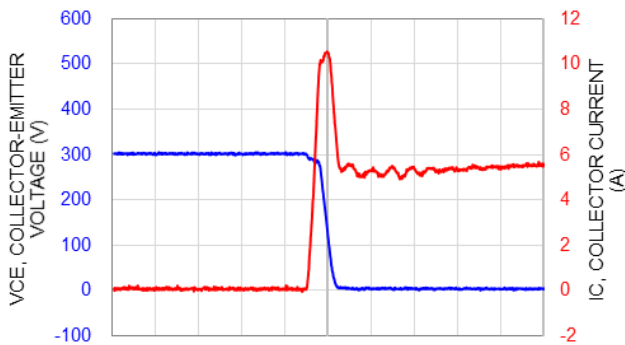


Figure 18. Turn-on Waveform Tj = 100 °C, VPN = 300 V

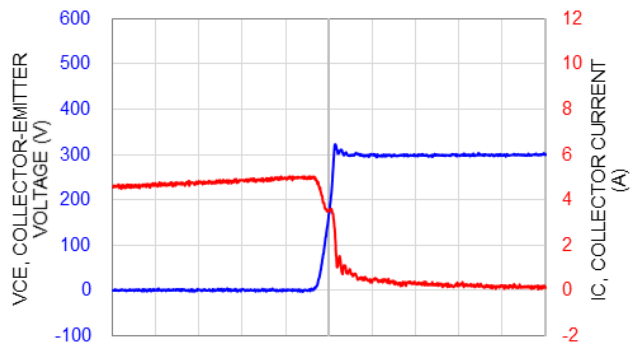
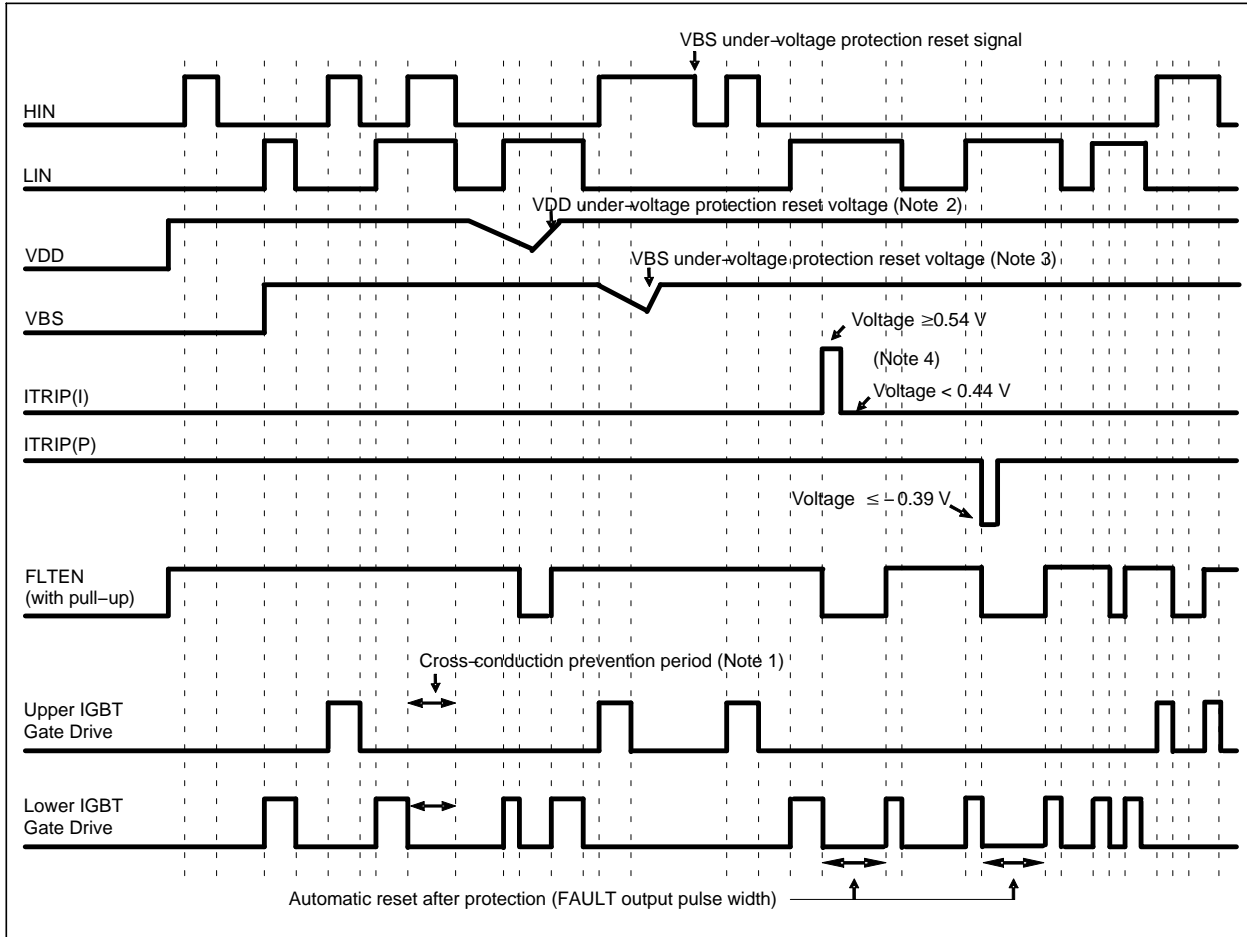


Figure 19. Turn-off Waveform Tj = 100 °C, VPN = 300 V

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APPLICATIONS INFORMATION

Input / Output Timing Chart



NOTES:

1. This section of the timing diagram shows the effect of cross-conduction prevention.
2. This section of the timing diagram shows that when the voltage on VDD decreases sufficiently all gate output signals will go low, switching off all six IGBTs and PFC MOSFET. When the voltage on VDD rises sufficiently, normal operation will resume.
3. This section shows that when the bootstrap voltage on VBS drops, the corresponding high side output U (V, W) is switched off. When the voltage on VBS rises sufficiently, normal operation will resume.
4. This section shows that when the voltage on ITRIP(I) exceeds the threshold, all IGBTs and PFC MOSFET are turned off. Normal operation resumes later after the over-current condition is removed. Similarly, when the voltage on ITRIP(P) exceeds the threshold, all IGBTs and PFC MOSFET are turned off. Normal operation resumes later after the over-current condition is removed.
5. After VDD has risen above the threshold to enable normal operation, the driver waits to receive an input signal on the LIN input before enabling the driver for the HIN signal.

Figure 20. Input / Output Timing Chart

Table 6. INPUT / OUTPUT LOGIC TABLE

| INPUT | | | | OUTPUT | | | |
|-------|-----|----------|----------|----------------|---------------|----------------|--------|
| HIN | LIN | ITRIP(I) | ITRIP(P) | High side IGBT | Low side IGBT | U,V,W | VFLTEN |
| H | L | L | L | ON (Note 5) | OFF | P | OFF |
| L | H | L | L | OFF | ON | NU,NV,NW | OFF |
| L | L | L | L | OFF | OFF | High Impedance | OFF |
| H | H | L | L | OFF | OFF | High Impedance | OFF |
| X | X | H | X | OFF | OFF | High Impedance | ON |
| X | X | X | H | OFF | OFF | High Impedance | ON |

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Table 7. THERMISTOR CHARACTERISTICS

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------|------------------|------------------------|--------|------|--------|------|
| Resistance | R ₂₅ | T _c = 25°C | 44.65 | 47 | 49.35 | kΩ |
| | R ₁₂₅ | T _c = 125°C | 1.29 | 1.41 | 1.53 | kΩ |
| B-Constant (25–50°C) | – | B | 4009.5 | 4050 | 4090.5 | K |
| Temperature Range | – | – | –40 | – | +125 | °C |

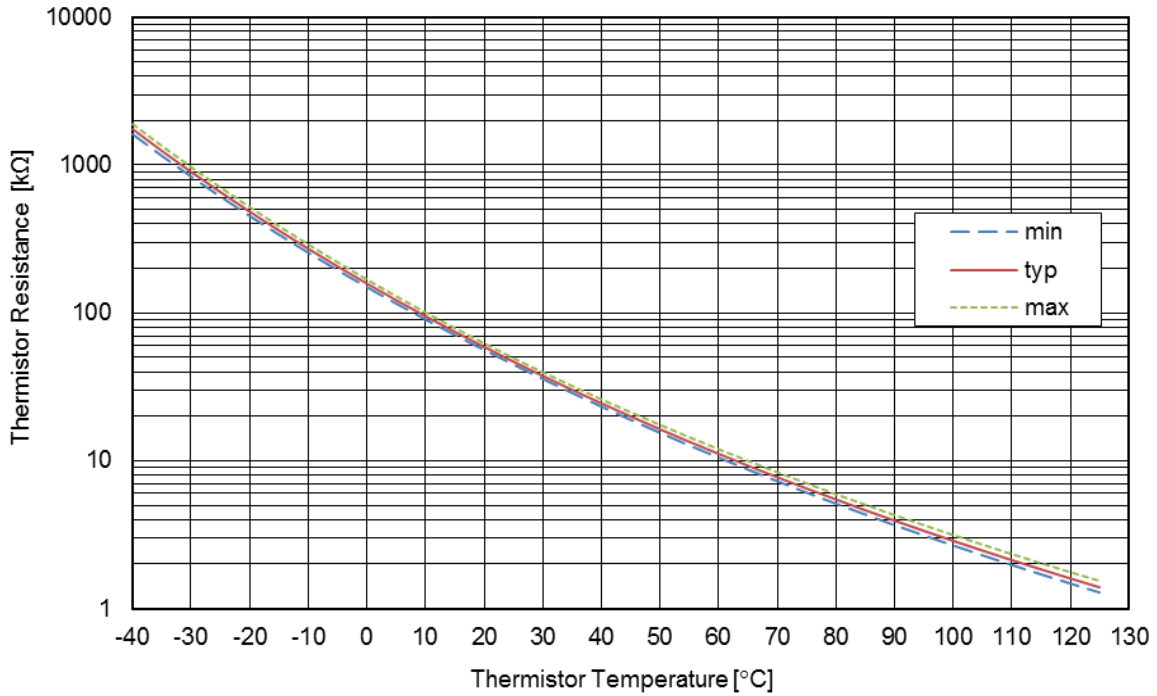


Figure 21. Thermistor Resistance – Thermistor Temperature

Signal Inputs

Each signal input has a pull-down resistor internally. An additional pull-down resistor of between 2.2 kΩ and 3.3 kΩ is recommended on each input to improve noise immunity.

FLTEN pin

The FLTEN pin is connected internally to an open-drain FAULT output and an ENABLE input requiring a pull-up resistor. If the pull-up voltage is 5 V, use a pull-up resistor with a value of 6.8 kΩ or higher. If the pull-up voltage is 15 V, use a pull-up resistor with a value of 20 kΩ or higher. The pulled up voltage in normal operation for the FLTEN pin should be above 2.5 V, noting that it is connected to an internal ENABLE input. The FAULT output is triggered if there is a VDD under-voltage or an overcurrent condition on either the PFC or inverter stages.

Driving the FLTEN terminal pin is used to enable or shut down the built-in driver. If the voltage on the FLTEN pin rises above the positive going FLTEN threshold, the output drivers are enabled. If the voltage on the FLTEN pin falls below the negative going FLTEN threshold, the drivers are disabled.

Under-voltage Protection

If VDD goes below the VDD supply undervoltage lockout falling threshold, the FAULT output is switched on. The FAULT output stays on until VDD rises above the VDD supply under-voltage lockout rising threshold. The hysteresis is approximately 200 mV.

Overcurrent Protection

An over-current condition is detected if the voltage on the ITRIP(I) or ITRIP(P) pins are exceed the reference voltage (Refer to Table 6 – Input / Output Logic Table). There is a blanking time of typically 350 ns to improve noise immunity. After a shutdown propagation delay of typically 0.6 μs, the FAULT output is switched on.

The over-current protection threshold should be set to be equal or lower to 2 times the module rated current (Io).

An additional fuse is recommended to protect against system level or abnormal over-current fault conditions.

Capacitors on High Voltage and VDD supplies

Both the high voltage and VDD supplies require an electrolytic capacitor and an additional high frequency capacitor. The recommended value of the high frequency capacitor is between 100 nF and 10 μF.

Minimum Input Pulse Width

When input pulse width is less than 1 μs, an output may not react to the pulse. (Both ON signal and OFF signal)

Calculation of Bootstrap Capacitor Value

The bootstrap capacitor value CB is calculated using the following approach. The following parameters influence the choice of bootstrap capacitor:

- VBS: Bootstrap power supply.
15 V is recommended.
- QG: Total gate charge of IGBT at VBS = 15 V.
12.7 nC
- UVLO: Falling threshold for UVLO.
Specified as 12 V.
- IDMAX: High side drive power dissipation.
Specified as 0.4 mA
- TONMAX: Maximum ON pulse width of high side IGBT.

Capacitance calculation formula:

$$CB = (QG + IDMAX * TONMAX)/(VBS - UVLO)$$

CB is recommended to be approximately 3 times the value calculated above. The recommended value of CB is in the range of 1 to 47 μF, however, the value needs to be verified prior to production. When not using the bootstrap circuit, each high side driver power supply requires an external independent power supply.

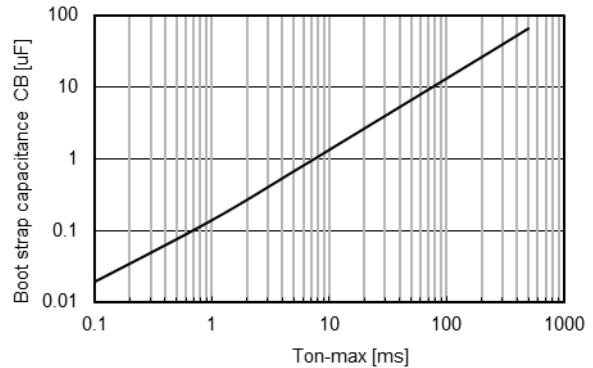


Figure 22. Bootstrap Capacitance versus Ton-max

Table 8. MOUNTING INSTRUCTIONS

| Item | Recommended Condition |
|-----------|---|
| Pitch | 56.0 ± 0.1 mm (Please refer to MECHANICAL CASE OUTLINE) |
| Screw | Diameter : M3 Screw head types: pan head, truss head, binding head |
| Washer | Plane washer The size is D: 7 mm, d: 3.2 mm and t: 0.5 mm JIS B 1256 |
| Heat sink | Material: Aluminum or Copper Warpage (the surface that contacts IPM) : -50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM. |
| Torque | Temporary tightening : 20 to 30 % of final tightening on first screw Temporary tightening : 20 to 30 % of final tightening on second screw Final tightening : 0.6 to 0.9 Nm on first screw Final tightening : 0.6 to 0.9 Nm on second screw |
| Grease | Silicone grease. Thickness : 100 to 200 μm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance. |

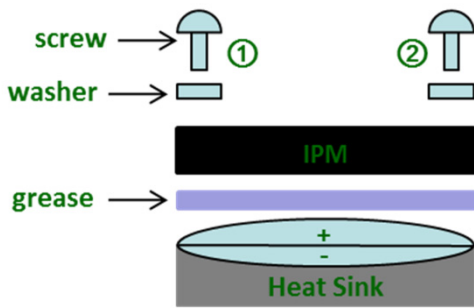


Figure 23. Mount IPM on a Heat Sink

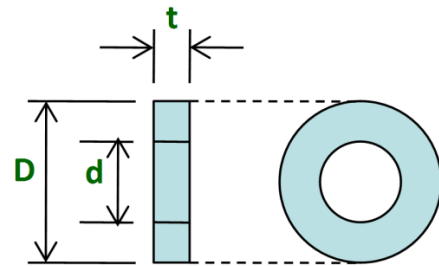


Figure 24. Size of Washer

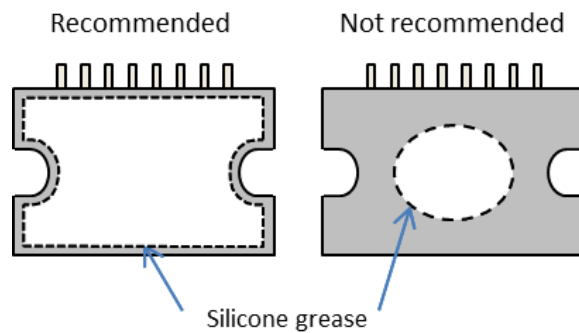


Figure 25. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink

- 1st : Temporarily tighten maintaining a left/right balance.
- 2nd : Finally tighten maintaining a left/right balance.

NFCS1060L3TT

TEST CIRCUITS

- ICES, IDSS, IR, IR(DB)

| | Inverter High Side | | | Inverter Low Side | | | PFC MOSFET |
|---|--------------------|----|----|-------------------|----|----|------------|
| | U | V | W | U | V | W | |
| A | 16 | 16 | 16 | 13 | 9 | 5 | 1 |
| B | 13 | 9 | 5 | 22 | 21 | 20 | 19 |

| | Boot Strap Diode | | | PFC Diode |
|---|------------------|----|----|-----------|
| | U | V | W | |
| A | 12 | 8 | 4 | 16 |
| B | 35 | 35 | 35 | 1 |

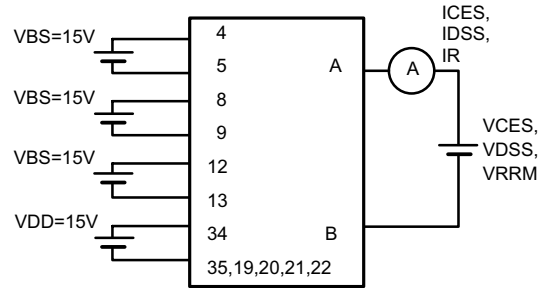


Figure 26. Test Circuit for ICES, IDSS, IR

- VCE(sat), RDS(on) (Test by pulse)

| | Inverter High Side | | | Inverter Low Side | | | PFC MOSFET |
|---|--------------------|----|----|-------------------|----|----|------------|
| | U | V | W | U | V | W | |
| A | 16 | 16 | 16 | 13 | 9 | 5 | 1 |
| B | 13 | 9 | 5 | 22 | 21 | 20 | 19 |
| C | 23 | 24 | 25 | 26 | 27 | 28 | 29 |

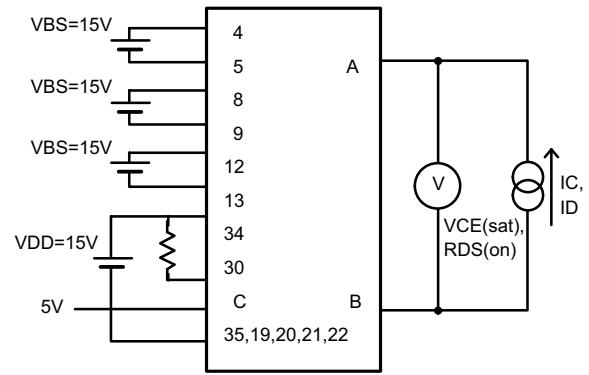


Figure 27. Test Circuit for VCE(sat)

- VF, VF(DB), VSD (Test by pulse)

| | Inverter High Side | | | Inverter Low Side | | |
|---|--------------------|----|----|-------------------|----|----|
| | U | V | W | U | V | W |
| A | 16 | 16 | 16 | 13 | 9 | 5 |
| B | 13 | 9 | 5 | 22 | 21 | 20 |

| | Boot Strap Diode | | | PFC Diode | MOSFET Body Diode |
|---|------------------|----|----|-----------|-------------------|
| | U | V | W | | |
| A | 12 | 8 | 4 | 16 | 1 |
| B | 34 | 34 | 34 | 1 | 19 |

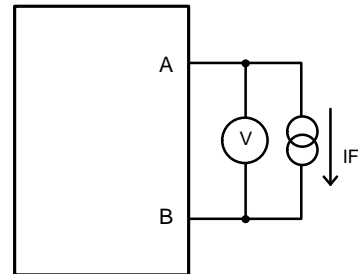


Figure 28. Test Circuit for VF

- IQBS, IQDD

| | VBS U | VBS V | VBS W | VDD |
|---|-------|-------|-------|-----|
| A | 12 | 8 | 4 | 34 |
| B | 13 | 9 | 5 | 35 |

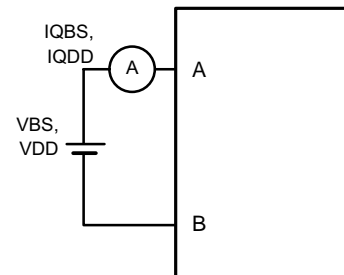


Figure 29. Test Circuit for IQBS, IQDD

• VITRIP(I), VITRIP(P)

| | VITRIP(I) (U-) | VITRIP(P) |
|---|----------------|-----------|
| A | 13 | 1 |
| B | 22 | 19 |
| C | 26 | 29 |
| D | 32 | 31 |

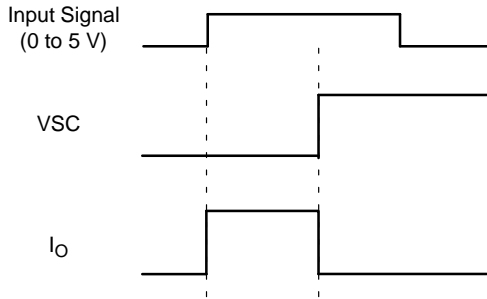


Figure 30.

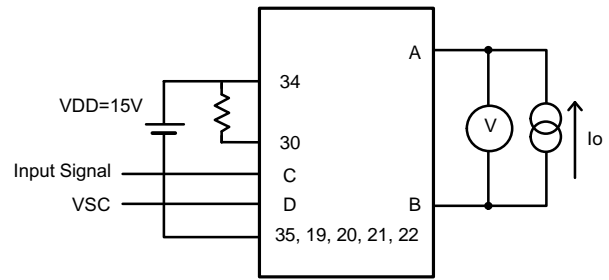


Figure 31. Test Circuit for VITRIP(I), VITRIP(P)

• Switching Time (The circuit is a representative example of the Inverter Low side U phase.)

| | Inverter High Side | | | Inverter Low Side | | | PFC MOSFET |
|---|--------------------|----|----|-------------------|----|----|------------|
| | U | V | W | U | V | W | |
| A | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| B | 22 | 21 | 20 | 22 | 21 | 20 | 19 |
| C | 13 | 9 | 5 | 13 | 9 | 5 | 1 |
| D | 22 | 21 | 20 | 16 | 16 | 16 | 16 |
| E | 23 | 24 | 25 | 26 | 27 | 28 | 29 |

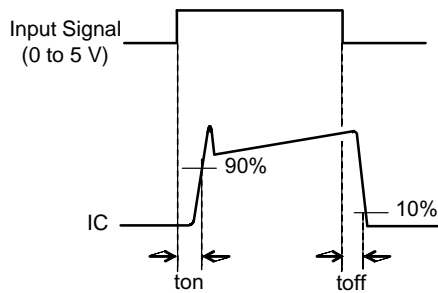


Figure 32.

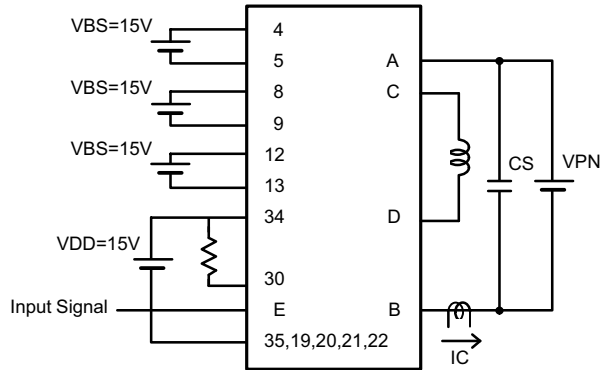


Figure 33. Test Circuit for Switching Time

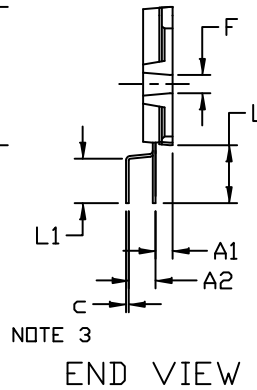
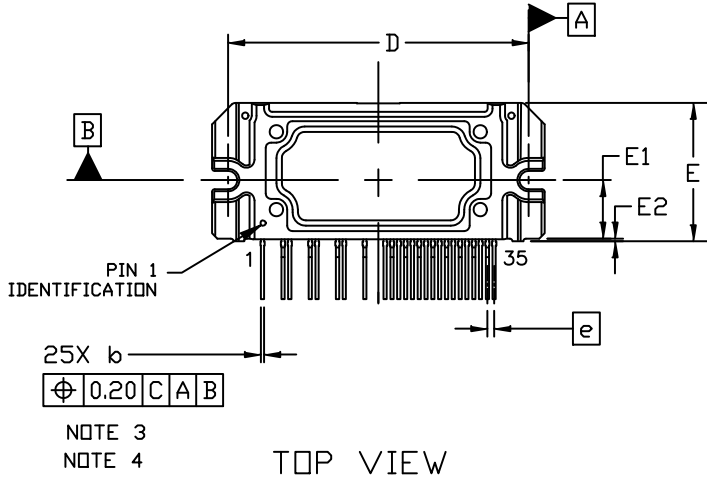
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

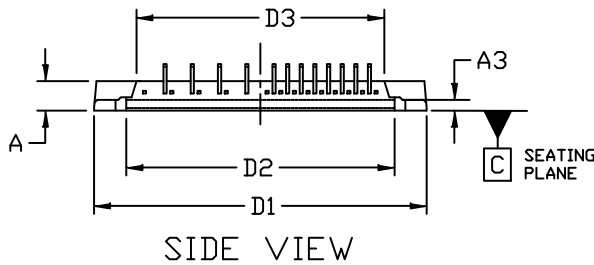


SIP35 56x25.8 / SIP2A-2
CASE 127DT
ISSUE A

DATE 05 MAR 2019



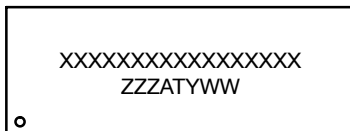
| DIM | MILLIMETERS | | |
|-----|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 5.00 | 5.50 | 6.00 |
| A1 | 2.70 | 3.20 | 3.70 |
| A2 | 4.50 | 5.00 | 5.50 |
| A3 | 1.50 | 2.00 | 2.50 |
| b | 0.55 | 0.60 | 0.80 |
| c | 0.45 | 0.50 | 0.70 |
| D | 55.50 | 56.00 | 56.50 |
| D1 | 61.50 | 62.00 | 62.50 |
| D2 | 49.50 | 50.00 | 50.50 |
| D3 | 45.70 | 46.20 | 46.70 |
| E | 25.30 | 25.80 | 26.30 |
| E1 | 10.90 REF | | |
| E2 | 0.00 | 0.50 | 1.00 |
| e | 1.27 BSC | | |
| F | 2.90 | 3.40 | 3.90 |
| L | 10.30 | 10.80 | 11.30 |
| L1 | 7.80 | 8.30 | 8.80 |



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS b AND c APPLY TO THE PLATED LEAD AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEADS IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. MIRROR SURFACE MARK INDICATES PIN 1 POSITION.
6. MISSING PINS ARE: 2, 3, 6, 7, 10, 11, 14, 15, 17, AND 18.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 ZZZ = Assembly Lot Code
 AT = Assembly & Test Location
 Y = Year
 WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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