

Ultra-Low Noise Amplifier for Global Navigation Satellite Systems (GNSS)

Features

- Reduce RF environment Interference with patented Smart-Linearity-Technology (SLT);
- Low noise figure(NF)=0.79dB@1.575GHz; NF=0.79dB@1.227GHz;NF=0.80dB@1.176GHz;
- High power gain=18.3dB@1.575GHz;power gain=18.9dB@1.227GHz;power gain=18.7dB@1.176 GHz;
- High linearity IIP3oob=-0.3dBm;
- High input 1dB-compression point=-9.0dBm;
- Requires only one input matching inductor for L1 band while additional output matching capacitor and inductor are needed for L2/L5 band ;
- RF output internally matched to 50 ohm;
- Supply voltage: 1.5V to 3.6V;
- Operating frequencies: GPS L1、 L2/L5 band;
- DFN 1.5mmX1.0mmX0.55mm-6L package;
- 3KV HBM ESD protection (including RFIN and RFOUT pin);

Applications

- Smart phones, feature phones;
- Tablet PCs;
- Personal Navigation Devices;
- Digital Still Cameras, Digital Video Cameras;
- RF Front End modules;
- Complete GPS chipset modules;
- Theft protection(laptop, ATM);

General Description

- The AW5005EDNR is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, GLONASS, Galileo and Compass. With on-chip DC blocking capacitors at RFIN and RFOUT, The AW5005EDNR can be close to the antenna, requires only one input matching inductor for L1 band while additional output matching capacitor and inductor are needed for L2/L5 band, and reduces assembly complexity and the PCB area, enabling a cost-effective solution.
- The AW5005EDNR with patented Smart Linearity Technology (SLT) achieves ultra-low noise figure, high linearity, high gain, over a wide range of supply voltages from 1.5V up to 3.6V. All these features make AW5005EDNR an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provides better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.
- The AW5005EDNR is available in a small lead-free, RoHS-Compliant, DFN 1.5mm X 1.0mm X 0.55mm -6L package.

Typical Application Circuit

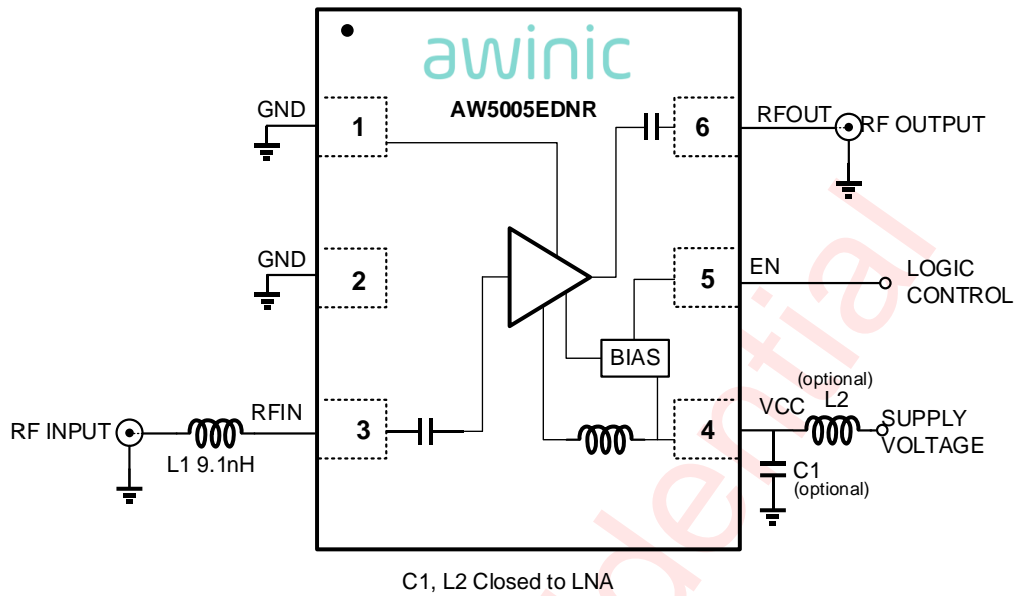


Figure 1(a) Typical Application Circuit of AW5005EDNR for GNSS L1

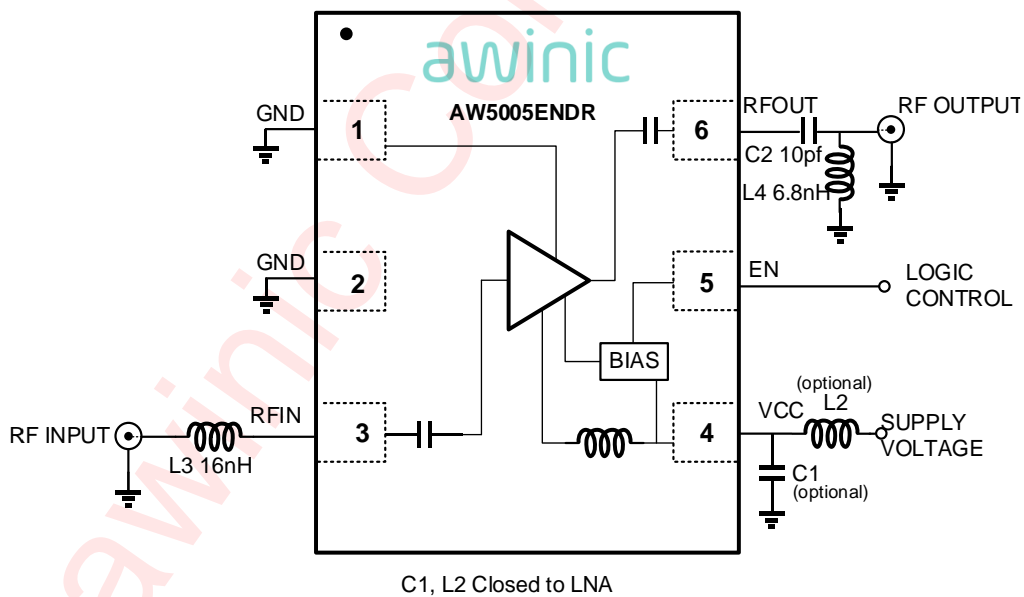


Figure 1(b) Typical Application Circuit of AW5005EDNR for GNSS L2/L5

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Pin Configuration And Top Mark

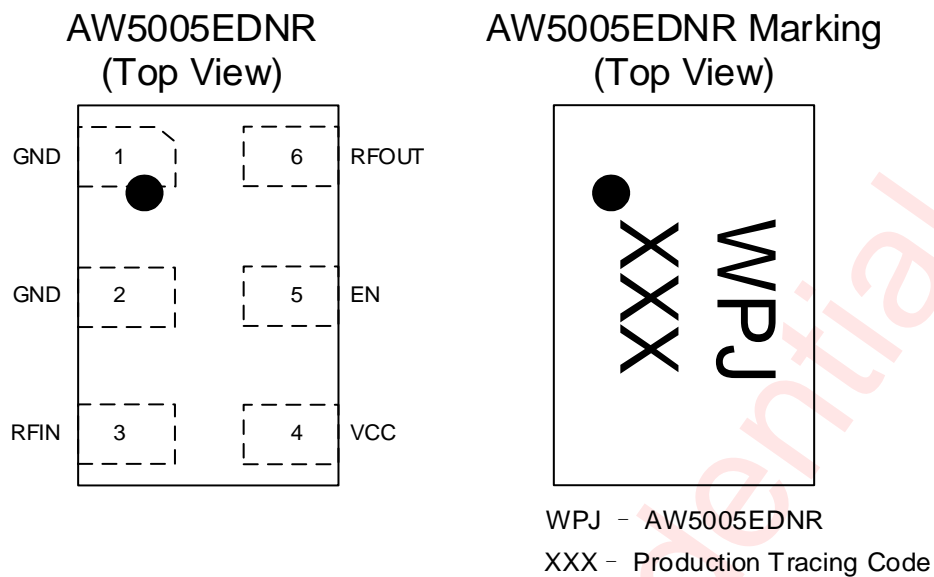


Figure 2 Pin Configuration and Top Mark

Pin Definition

| No. | NAME | DESCRIPTION |
|-----|-------|---------------|
| 1 | GND | Ground |
| 2 | GND | Ground |
| 3 | RFIN | LNA input |
| 4 | VCC | DC Supply |
| 5 | EN | Logic control |
| 6 | RFOUT | LNA output |

Functional Block Diagram

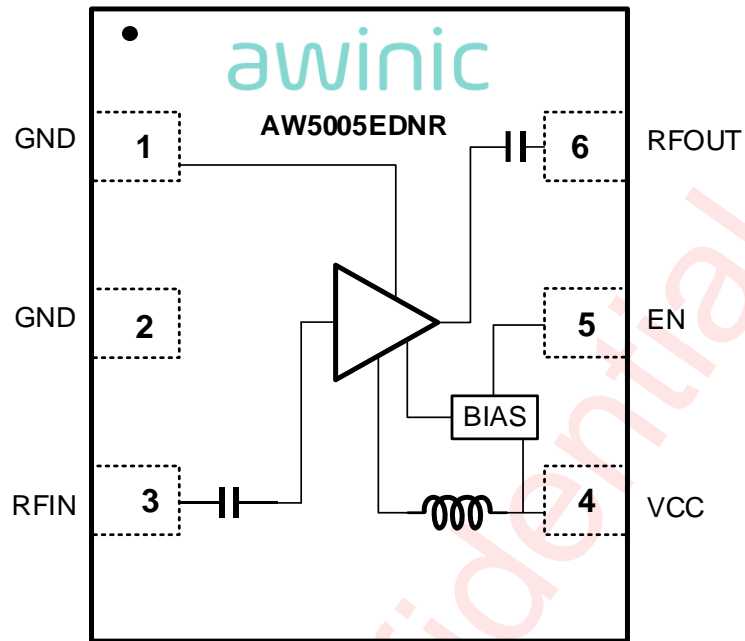


Figure 3 Functional Block Diagram

Ordering Information

| Part Number | Temperature | Package | Marking | Moisture Sensitivity Level | Environmental Information | Delivery Form |
|-------------|--------------|---------------------------|---------|----------------------------|---------------------------|------------------------------|
| AW5005EDNR | -40°C ~ 85°C | DFN 1.5mmX1.0mm- 6L | WPJ | MSL1 | ROHS+HF | 4500 units/ Tape and Reel |

Absolute Maximum Ratings ^[1]

| PARAMETERS | Symbol | Values | | | |
|----------------------------|---------------|------------------------|-------|------|------|
| | | Min. | Typ. | Max. | |
| Supply Voltage at pin VCC | VCC | -0.3 | - | 5 | V |
| Voltage at pin EN [2] | VEN | -0.3 | - | 5 | V |
| Current into pin VCC | ICC | - | - | 30 | mA |
| RF input power [3] | PIN | - | - | 10 | dBm |
| Package thermal resistance | θ_{JA} | - | 148.2 | - | °C/W |
| Junction temperature | TJ | - | - | 150 | °C |
| Storage temperature range | TSTG | -65 | - | 150 | °C |
| Ambient temperature range | Tamb | -40 | - | 85 | °C |
| Solder temperature(10s) | | - | 260 | - | °C |
| ESD range | | | | | |
| HBM [4] | | ±3000 | | | V |
| CDM[5] | | ±1000 | | | V |
| Latch-up | | | | | |
| Standard: JESD78E | | +IT: +400 -IT: -400 | | | mA |

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2: Warning: due to internal ESD diode protection, the applied DC voltage should not exceed 5.0V in order to avoid excess current.

Note3: The RF input and RF output are AC coupled through internal DC blocking capacitor.

Note4: HBM standard: ESDA/JEDEC JS-001-2017

Note5: CDM standard: ESDA/JEDEC JS-002-2018

Electrical Characteristics

(AW5005EDNR EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1550MHz to 1615MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1575.42MHz, input matched to 50Ω using a 9.1nH inductor, unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|-------|------|------|------|
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{CC} | Supply Voltage | | 1.5 | - | 3.6 | V |
| I _{SD} | Shut-Down Current | EN=Low | | | 1 | μA |
| I _{CC} | Supply Current | EN=High | | 8.0 | 13.0 | mA |
| V _{EN} | Digital Input-Logic High | | 0.80 | | VCC | V |
| V _{EN} | Digital Input-Logic Low | | | | 0.45 | V |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| G _p | Power Gain | Pin=-30dBm | 17 | 18.3 | 20 | dB |
| RL _{in} | Input Return Loss | | 5 | 6 | | dB |
| RL _{out} | Output Return Loss | | 8 | 10 | | dB |
| ISL | Reverse Isolation | | 25 | 28.5 | | dB |
| NF | Noise Figure ^[2] | Zs=50 ohm; No jammer | | 0.79 | 1.2 | dB |
| Kf | Stability factor | f=20MHz...10GHz | 1 | | | |
| IP1dB | In band input 1dB-compression point | f=1575.42MHz | -12.0 | -9.0 | | dBm |
| IIP3 | In-band input 3 rd -order intercept point | f1=1574.42MHz ^[3] ; f2=1575.42MHz; Pin=-25dBm; | -5.0 | -1.0 | | dBm |
| IIP3 _{oob} | Out-of-band input 3 rd -order intercept point | f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-25dBm; | -3.0 | -0.3 | | dBm |
| IIP3 _{oob} | Out-of-band input 3 rd -order intercept point | f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm; | -3.0 | -1.0 | | dBm |
| t _{on} | turn-on time | time from V _{EN} ON to 90% of the final gain | | 2.2 | 2.5 | μs |
| t _{off} | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1.7 | 2.0 | μs |

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1}-IM3)+Pi_{f1}$.

(AW5005EDNR EVB^[1] ; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1550MHz to 1615MHz; Typical values are at VCC=1.8V and TA=+25°C, f=1575.42MHz, input matched to 50Ω using a 9.1nH inductor, unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|-------|-------|------|------|
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{CC} | Supply Voltage | | 1.5 | - | 3.6 | V |
| I _{SD} | Shut-Down Current | EN=Low | | | 1 | μA |
| I _{CC} | Supply Current | EN=High | | 6.0 | 13.0 | mA |
| V _{EN} | Digital Input-Logic High | | 0.80 | | VCC | V |
| V _{EN} | Digital Input-Logic Low | | | | 0.45 | V |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| G _p | Power Gain | Pin=-30dBm | 16.5 | 17.5 | 19.5 | dB |
| RL _{in} | Input Return Loss | | 5 | 6 | | dB |
| RL _{out} | Output Return Loss | | 8 | 10 | | dB |
| ISL | Reverse Isolation | | 25 | 28.5 | | dB |
| NF | Noise Figure ^[2] | Zs=50 ohm; No jammer | | 0.82 | 1.2 | dB |
| Kf | Stability factor | f=20MHz...10GHz | 1 | | | |
| IP1dB | Inband input 1dB-compression point | f=1575.42MHz | -14.0 | -11.0 | | dBm |
| IIP3 | In-of-band input 3 rd -order intercept point | f1=1574.42MHz ^[3] ; f2=1575.42MHz; Pin=-25dBm; | -5.0 | -1.7 | | dBm |
| IIP3 _{oob} | Out-of-band input 3 rd -order intercept point | f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-25dBm; | -5.0 | -2.1 | | dBm |
| IIP3 _{oob} | Out-of-band input 3 rd -order intercept point | f1=1712.7MHz ^[3] ; f2=1850MHz; Pin=-30dBm; | -4.0 | -1.7 | | dBm |
| t _{on} | turn-on time | time from V _{EN} ON to 90% of the final gain | | 2.2 | 2.5 | μs |
| t _{off} | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1.7 | 2.0 | μs |

Note1: input matched to 50 ohm using a high quality-factor 9.1nH inductor.

Note2: 0.08dB PCB losses are subtracted.

Note3: $IIP3=0.5*(Po_{f1-IM3})+Pi_{f1}$.

(AW5005EDNR EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1227.60 ± 1.023MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1227.60MHz, input matched to 50Ω using a 16nH inductor, output matched to 50Ω with additional 10pF capacitor and 6.8nH inductor, unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|-------|-------|-----------------|------|
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{CC} | Supply Voltage | | 1.5 | - | 3.6 | V |
| I _{SD} | Shut-Down Current | EN=Low | | | 1 | μA |
| I _{CC} | Supply Current | EN=High | | 8 | 13.0 | mA |
| V _{EN} | Digital Input-Logic High | | 0.80 | | V _{CC} | V |
| V _{EN} | Digital Input-Logic Low | | | | 0.45 | V |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| G _p | Power Gain | Pin=-30dBm | 17.5 | 18.9 | 20.5 | dB |
| RL _{in} | Input Return Loss | | 4 | 6 | | dB |
| RL _{out} | Output Return Loss | | 8 | 12.3 | | dB |
| ISL | Reverse Isolation | | 22 | 26.2 | | dB |
| NF | Noise Figure ^[2] | Z _s =50 ohm; No jammer | | 0.79 | 1.2 | dB |
| K _f | Stability factor | f=20MHz...10GHz | 1 | | | |
| IP1dB | Inband input 1dB-compression point | f=1227.6MHz | -14.0 | -11.0 | | dBm |
| IIP3 | In-band input 3 rd -order intercept point | f1=1226.6MHz ^[3] ; f2=1227.6MHz; Pin=-25dBm; | -5.0 | -3.0 | | dBm |
| t _{on} | turn-on time | time from V _{EN} ON to 90% of the final gain | | 2.2 | 2.5 | μs |
| t _{off} | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1.7 | 2.0 | μs |

(AW5005EDNR EVB^[1]; V_{CC}=1.5 to 3.6V, T_A=-40~+85°C, f=1227.60 ± 1.023MHz; Typical values are at V_{CC}=1.8V and T_A=+25°C, f=1227.60MHz, input matched to 50Ω using a 16nH inductor, output matched to 50Ω with additional 10pF capacitor and 6.8nH inductor, unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------------|--------------------------|----------------|------|------|-----------------|------|
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{CC} | Supply Voltage | | 1.5 | - | 3.6 | V |
| I _{SD} | Shut-Down Current | EN=Low | | | 1 | μA |
| I _{CC} | Supply Current | EN=High | | 6.0 | 13.0 | mA |
| V _{EN} | Digital Input-Logic High | | 0.80 | | V _{CC} | V |
| V _{EN} | Digital Input-Logic Low | | | | 0.45 | V |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| G _p | Power Gain | Pin=-30dBm | 16.7 | 18.2 | 20 | dB |
| RL _{in} | Input Return Loss | | 4 | 6 | | dB |

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|-------------------|---|---|------|-------|-----|------|
| RL _{out} | Output Return Loss | | 8 | 12.4 | | dB |
| ISL | Reverse Isolation | | 22 | 25.6 | | dB |
| NF | Noise Figure ^[2] | Zs=50 ohm; No jammer | | 0.83 | 1.2 | dB |
| Kf | Stability factor | f=20MHz...10GHz | 1 | | | |
| IP1dB | In band input 1dB-compression point | f=1227.6MHz | -15 | -12.9 | | dBm |
| IIP3 | In-band input 3 rd -order intercept point | f1=1226.6MHz ^[3] ; f2=1227.6MHz; Pin=-25dBm; | -5.5 | -3.5 | | dBm |
| t _{on} | turn-on time | time from V _{EN} ON to 90% of the final gain | | 2.2 | 2.5 | μs |
| t _{off} | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1.7 | 2.0 | μs |

(AW5005EDNR EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1176.45 ± 1.023MHz; Typical values are at VCC=2.8V and TA=+25°C, f=1176.45MHz, input matched to 50Ω using a 16nH inductor, output matched to 50Ω with additional 10pF capacitor and 6.8nH inductor, unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|------|-------|------|------|
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{CC} | Supply Voltage | | 1.5 | - | 3.6 | V |
| I _{SD} | Shut-Down Current | EN=Low | | | 1 | μA |
| I _{CC} | Supply Current | EN=High | | 8.0 | 13.0 | mA |
| V _{EN} | Digital Input-Logic High | | 0.80 | | VCC | V |
| V _{EN} | Digital Input-Logic Low | | | | 0.45 | V |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| G _p | Power Gain | Pin=-30dBm | 17.0 | 18.7 | 20.5 | dB |
| RL _{in} | Input Return Loss | | 4 | 6 | | dB |
| RL _{out} | Output Return Loss | | 8 | 14.3 | | dB |
| ISL | Reverse Isolation | | 22 | 26.0 | | dB |
| NF | Noise Figure ^[2] | Zs=50 ohm; No jammer | | 0.80 | 1.2 | dB |
| Kf | Stability factor | f=20MHz...10GHz | 1 | | | |
| IP1dB | In band input 1dB-compression point | f=1176.45MHz | -14 | -11.0 | | dBm |
| IIP3 | In-band input 3 rd -order intercept point | f1=1175.45MHz ^[3] ; f2=1176.45MHz; Pin=-25dBm; | -5.0 | -2.3 | | dBm |

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|------------------|---------------|---|-----|-----|-----|------|
| t _{on} | turn-on time | time from V _{EN} ON to 90% of the final gain | | 2.2 | 2.5 | μs |
| t _{off} | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1.7 | 2.0 | μs |

(AW5005EDNR EVB^[1]; VCC=1.5 to 3.6V, TA=-40~+85°C, f=1176.45 ± 1.023MHz; Typical values are at VCC=1.8V and TA=+25°C, f=1176.45MHz, input matched to 50Ω using a 16nH inductor, output matched to 50Ω with additional 10pF capacitor and 6.8nH inductor, unless otherwise noted)

| PARAMETER | | TEST CONDITION | MIN | TYP | MAX | UNIT |
|--------------------------------------|---|---|-------|-------|------|------|
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| V _{CC} | Supply Voltage | | 1.5 | - | 3.6 | V |
| I _{SD} | Shut-Down Current | EN=Low | | | 1 | μA |
| I _{CC} | Supply Current | EN=High | | 6.0 | 13.0 | mA |
| V _{EN} | Digital Input-Logic High | | 0.80 | | VCC | V |
| V _{EN} | Digital Input-Logic Low | | | | 0.45 | V |
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| G _p | Power Gain | Pin=-30dBm | 16.5 | 18.0 | 19.5 | dB |
| RL _{in} | Input Return Loss | | 4 | 6 | | dB |
| RL _{out} | Output Return Loss | | 8 | 14.2 | | dB |
| ISL | Reverse Isolation | | 22 | 25.4 | | dB |
| NF | Noise Figure ^[2] | Z _s =50 ohm; No jammer | | 0.84 | 1.2 | dB |
| K _f | Stability factor | f=20MHz...10GHz | 1 | | | |
| IP1dB | In band input 1dB-compression point | f=1176.45MHz | -14.0 | -11.0 | | dBm |
| IIP3 | In-band input 3 rd -order intercept point | f1=1175.45MHz ^[3] ; f2=1176.45MHz; Pin=-25dBm; | -5.0 | -2.8 | | dBm |
| t _{on} | turn-on time | time from V _{EN} ON to 90% of the final gain | | 2.2 | 2.5 | μs |
| t _{off} | turn-off time | time from V _{EN} OFF to 10% of the gain | | 1.7 | 2.0 | μs |

Application Board

AW5005EDNR EVB is same as the one of AW5005DNRZ.

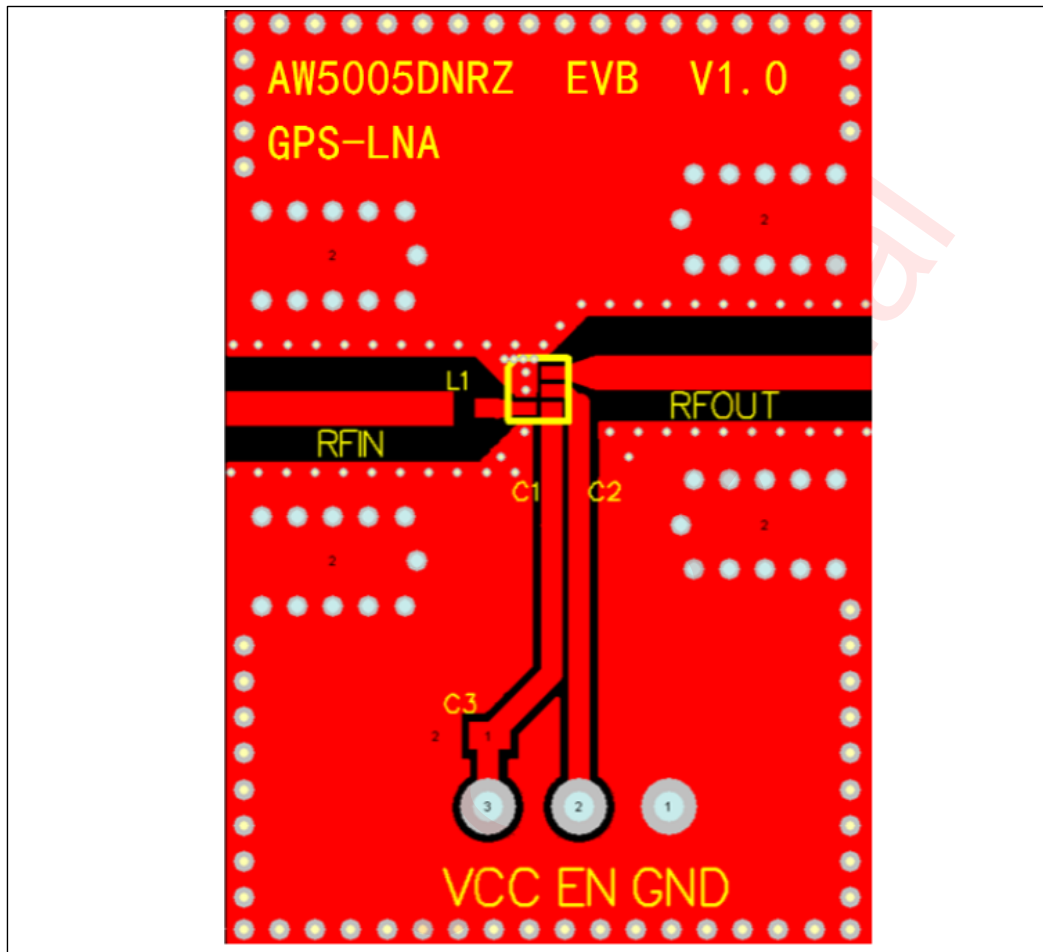


Figure 4 Drawing of Application Board for L1 band

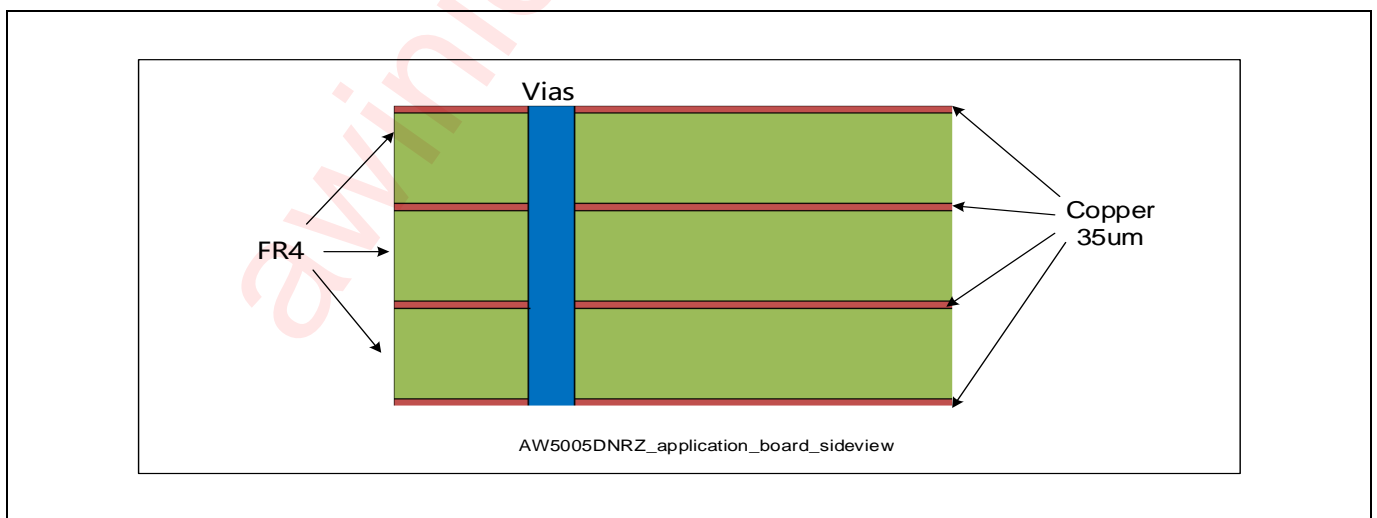
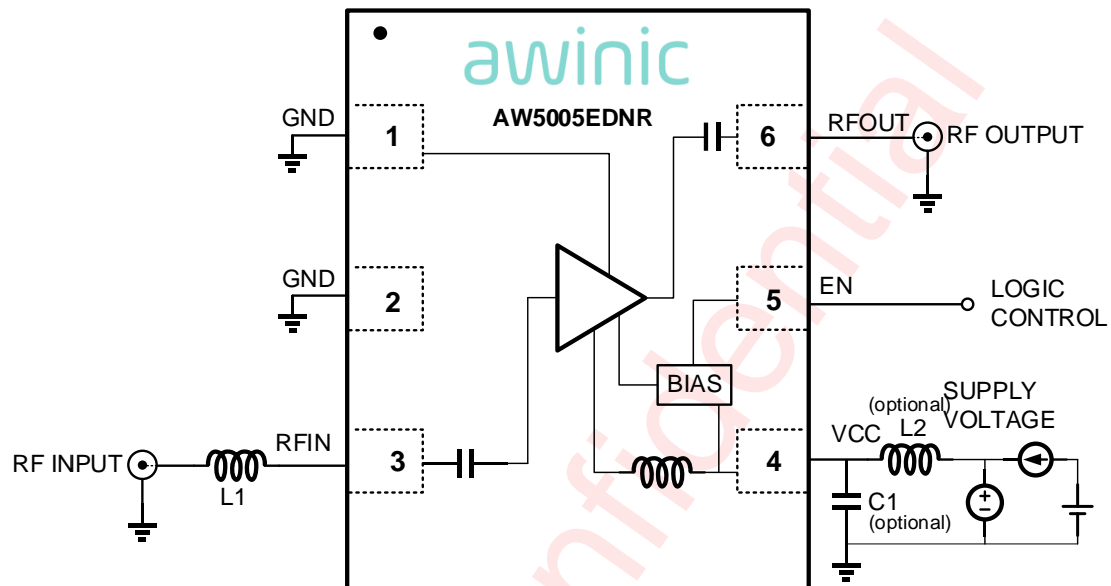


Figure 5 Application Board Cross-Section

Test Circuits

DC Characteristics

The following is the test bench for power supply, pin voltage, supply current, standby current



C1, L2 Closed to LNA

Figure 6 DC Test

S Parameter

The following is the test bench for input return loss, output return loss, reverse isolation, forward gain, and 1dB gain compression.

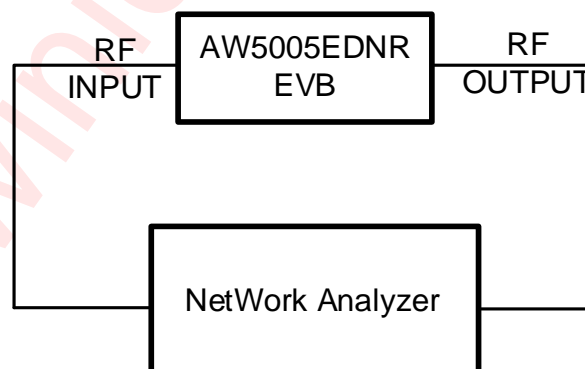


Figure 7 S Parameter Test

Noise Figure

The following is the test bench for noise figure, power gain.

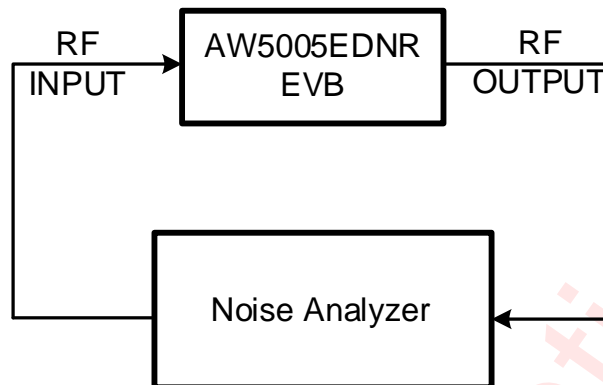


Figure 8 Noise Figure Test

Intermodulation distortion

The following is the test bench for third-order intercept point and second-order intercept point.

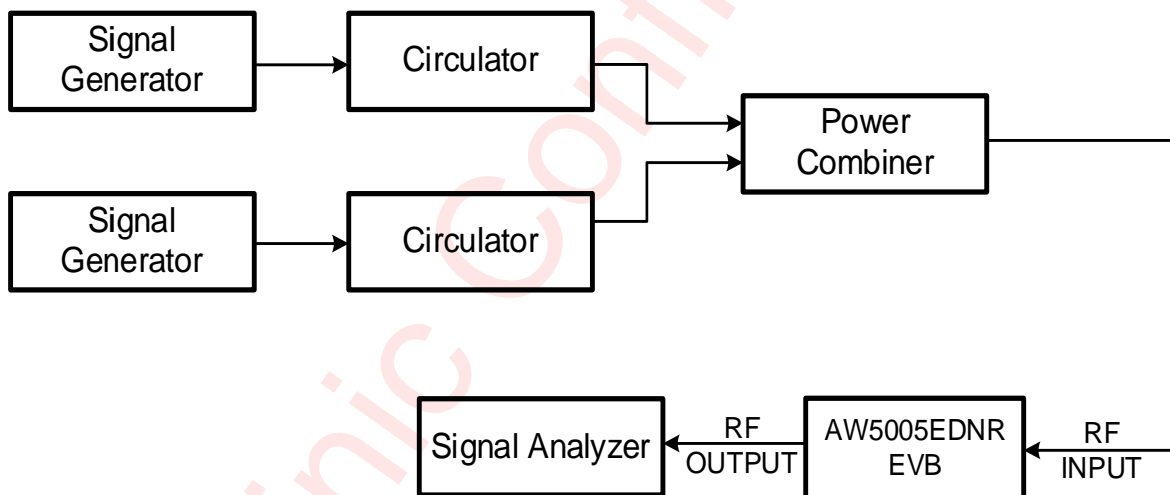


Figure 9 Intermodulation Distortion Test

Recommended Components List

Table1 lists the recommended inductor types and values; Table 2 lists the recommended capacitor types and values.

Table1: list of inductor

| Component | Part Number | Inductance | Q(min) | Q Test Frequency | Supplier | Size |
|-----------|-------------|------------|--------|------------------|----------|------|
| | Units | nH | | MHz | | |
| L1 | LQW15A | 9.1 | 25 | 250 | Murata | 0402 |
| L1 | SDWL1005C | 9.1 | 24 | 250 | Sunlord | 0402 |
| L2 | LQW15A | 100 | 20 | 150 | Murata | 0402 |
| L3 | LQW15A | 16 | 24 | 250 | Murata | 0402 |
| L4 | LQW15A | 6.8 | 30 | 250 | Murata | 0402 |

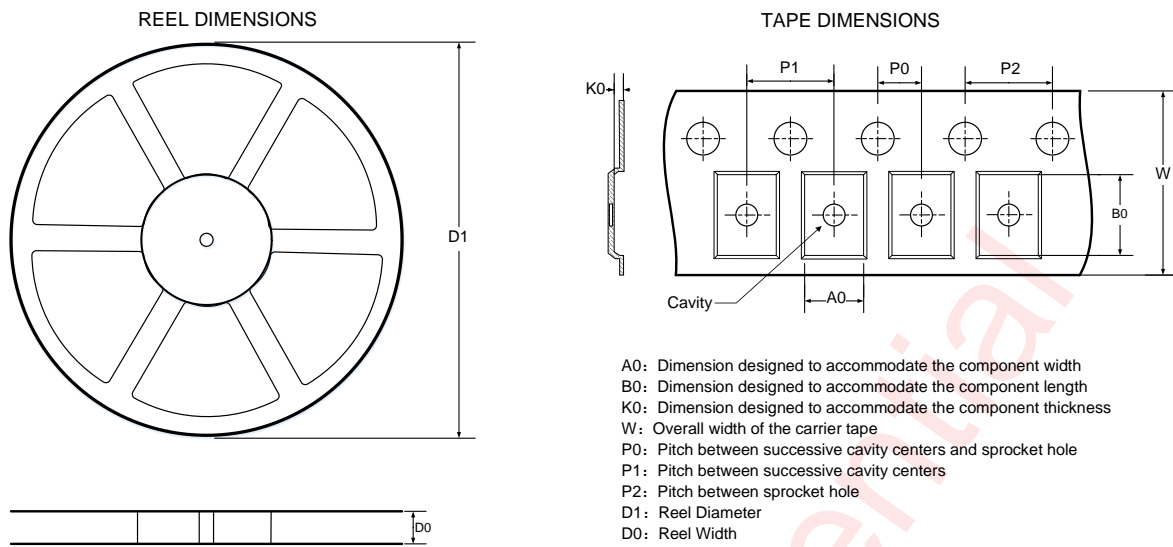
Table2: list of capacitor

| Component | Part Number | Capacitance | Rated Voltage | Supplier | Size |
|-----------|-------------|-------------|---------------|----------|------|
| | Units | pF | V | | |
| C1 | GRM155 | 1000 | 50 | Murata | 0402 |
| C2 | GRM155 | 10 | 50 | Murata | 0402 |

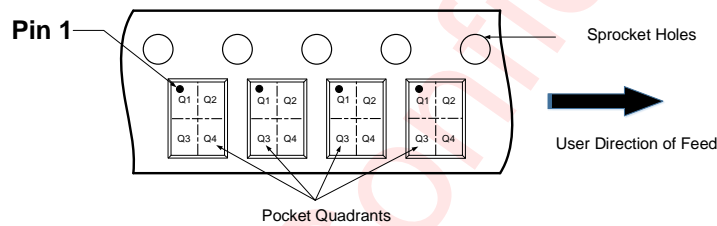
PCB Layout Consideration

1. The AW5005EDNR requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the capacitor we can get better performance like a little higher gain etc. The value is optimized for the best gain, noise figure, return loss performance. Typical value of inductor is 9.1nH, capacitor is 1nF. For schematics see Figure1.
2. The output of AW5005EDNR is internally matched to 50 ohm and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.
3. The AW5005EDNR should be placed close to the GPS antenna with the input-matching inductor. Use 50 ohm micro strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor should be located close to the device. For long VCC lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

Tape And Reel Information



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: The above picture is for reference only. Please refer to the value in the table below for the actual size

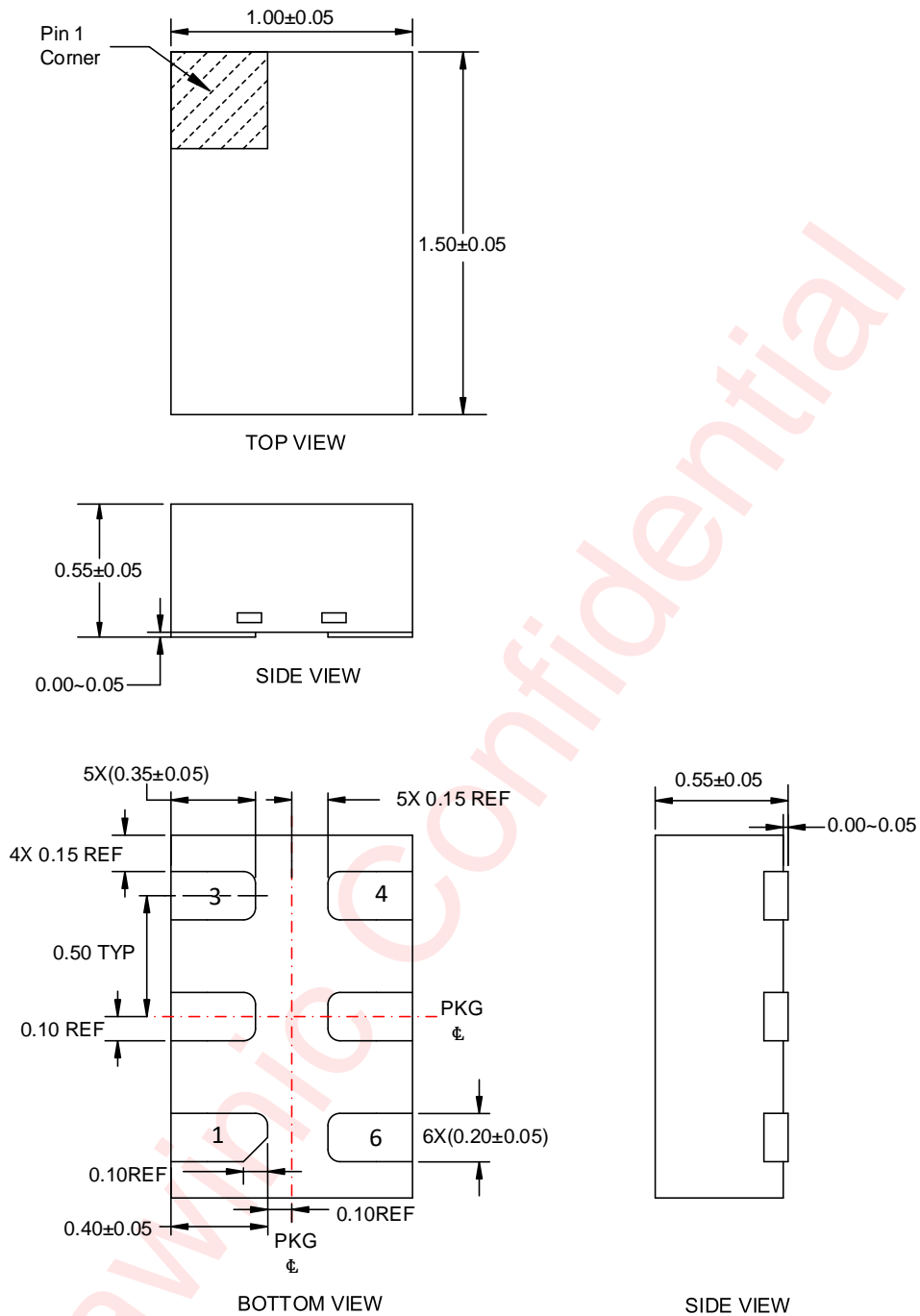
DIMENSIONS AND PIN1 ORIENTATION

| D1 (mm) | D0 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---------|---------|---------|---------|---------|---------|---------|---------|--------|---------------|
| 178 | 8.4 | 1.12 | 1.72 | 0.7 | 2 | 4 | 4 | 8 | Q1 |

All dimensions are nominal

Figure 10 Tape & Reel Description

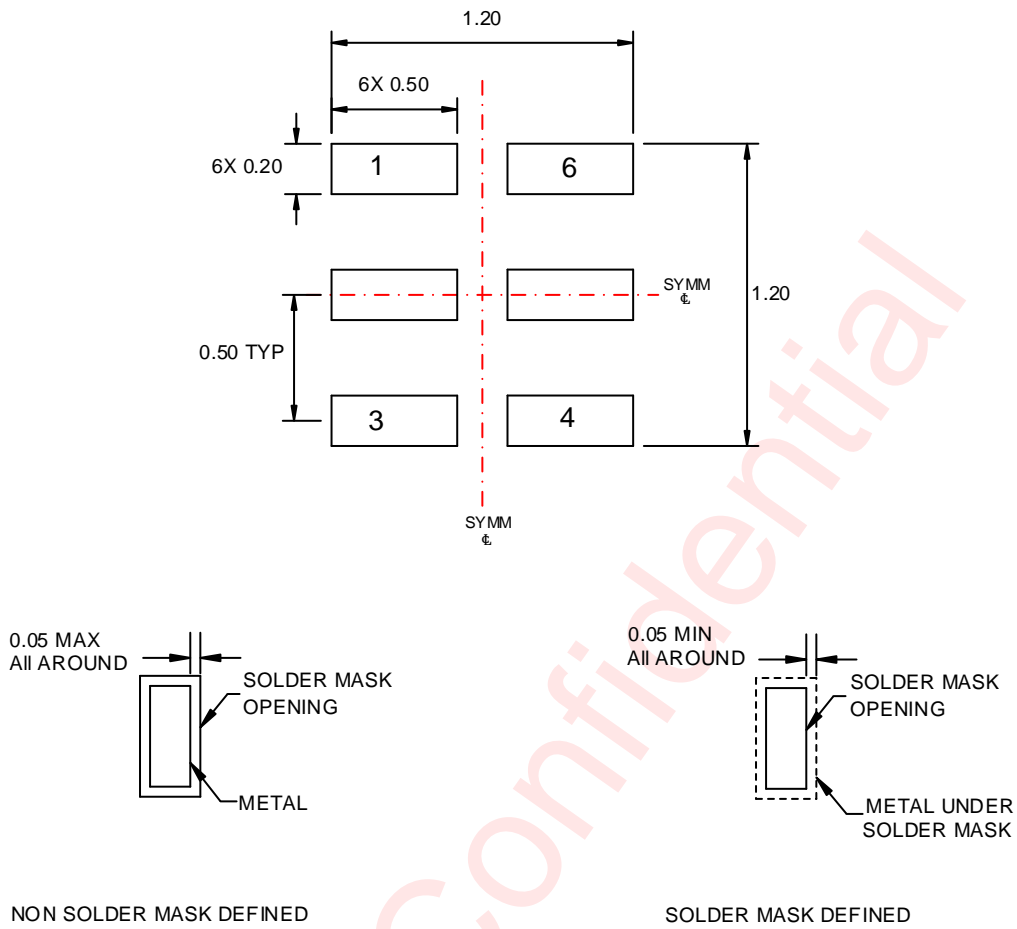
Package Outline Dimensions



Unit: mm

Figure 11 Package Outline

Land Pattern Data



Unit: mm

Figure 12 Land Pattern

Revision History

| Document ID | Release date | Change Record |
|-------------|--------------|--------------------------------|
| V1.0 | 2021-12 | Officially Released |
| V1.1 | 2022-6 | Added RF Characteristics Limit |
| V1.2 | 2022-8 | Modify Figure Number |
| V1.3 | 2023-1 | Update package outline |

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