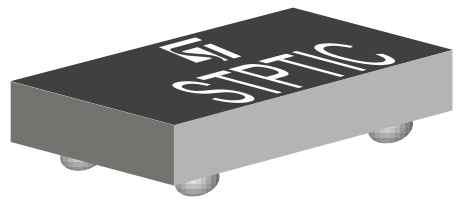
STPTIC-68G2

Parascan™ tunable integrated capacitor

Datasheet - production data



WLCSP 0.4 mm pitch

Features

- High power capability
- 5:1 tuning range
- High linearity
- High quality factor (Q)
- Low leakage current
- Compatible with high voltage control IC (STHVDAC series)
- Available in wafer level chip scale package:
  - WLCSP package 0.6 x 0.8 x 0.3 mm
- ECOPACK®2 compliant component

Benefit

- RF tunable passive implementation in mobile phones to optimize antenna radiated performance

Applications

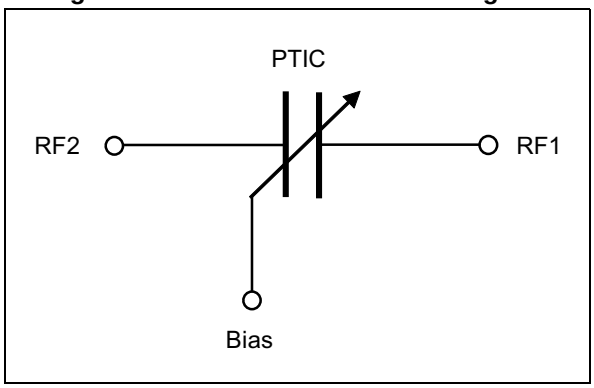
- Cellular antenna open loop tunable matching network in multi-band GSM/WCDMA/LTE mobile phone
- Open loop tunable RF filters

Description

The ST integrated tunable capacitor offers excellent RF performance, low power consumption and high linearity required in adaptive RF tuning applications. The fundamental building block of PTIC is a tunable material called Parascan™, which is a version of barium strontium titanate (BST) developed by Paratek microwave.

BST capacitors are tunable capacitors intended for use in mobile phone application and dedicated to RF tunable applications. These tunable capacitors are controlled through an extended bias voltage ranging from 1 to 24 V. The implementation of BST tunable capacitor in mobile phones enables significant improvement in terms of radiated performance making the performance almost insensitive to the external environment.

Figure 1. PTIC functional block diagram



TM: Parascan is a trademark of Paratek Microwave Inc.

1 Electrical characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter	Rating	Unit
P_{IN}	Input peak power RF_{IN} (CW mode)/all RF ports	+40	dBm
$V_{ESD(HBM)}$	Human body model, JESD22-A114-B, all I/O	Class 1B(1)	V
$V_{ESD(MM)}$	Machine model, JESD22-A115-A, all I/O	100	V
T_{device}	Device temperature	+125	°C
T_{stg}	Storage temperature	-55 to +150	
V_x	Bias voltage	25	V

1. Class 1B defined as passing 500 V, but fails after exposure to 1000V ESD pulse.

Table 2. Recommended operating conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
P_{IN}	RF input power		+33		dBm
F_{OP}	Operating frequency	700		2700	MHz
T_{device}	Device temperature			+100	°C
T_{OP}	Operating temperature	-30		+85	
V_{BIAS}	Bias voltage	1		24	V

Table 3. Representative performance (T_{amb} = 25 °C otherwise specified)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_{1V}	capacitor at 1 V bias	STPTIC-68G2	6.86	7.8	8.74	pF
C_{2V}	capacitor at 2 V bias	STPTIC-68G2		6.8		pF
C_{24V}	capacitor at 24 V bias	STPTIC-68G2	1.24	1.35	1.46	pF
ΔC	Tuning range	Ratio between C_{1V}/C_{24V} (1)	5/1			
I_L	Leakage current	Measured with V_{bias} = 24 V			100	nA
Q_{LB}	Quality factor	Measured at 700 MHz at 2 V	55	65		
Q_{HB}	Quality factor	Measured at 2700 MHz at 2 V	35	50		
IP3	Third order intercept point	V_{bias} = 1 V (2)(4)	52	60		dBm
		V_{bias} = 24 V (2)(4)		75		
H2	Second harmonic	V_{bias} = 1 V (3)(4)		-65	-45	dBm
		V_{bias} = 24 V (3)(4)		-75		
H3	Third harmonic	V_{bias} = 1 V (3)(4)		-35	-30	dBm
		V_{bias} = 24 V (3)(4)		-65		
t_T	Transition time	Average for any transition between C_{min} to C_{max} (5)		40		µs
		Average transition between C_{max} to C_{min} (5)		20		

1. Measured at low frequency
2. F_1 = 894 MHz, F_2 = 849 MHz, P_1 = +25 dBm, P_2 = +25 dBm, $2f_1 - f_2$ = 939 MHz
3. 850 MHz, P_{in} = +34 dBm
4. IP3 and harmonics are measured in the shunt configuration in a 50 Ω environment
5. One or both of RF_{in} and RF_{out} must be connected to DC ground, using the HVDAC turbo mode

Figure 2. Capacitor variation versus bias voltage

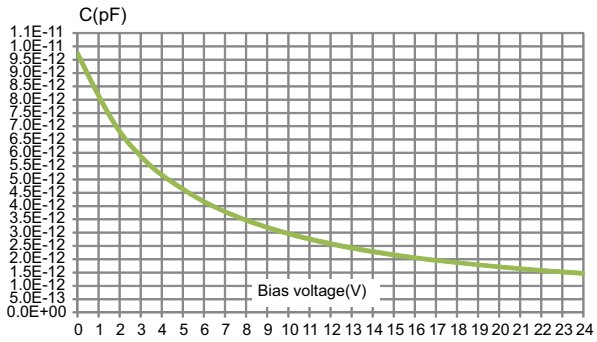


Figure 3. Quality factor versus frequency

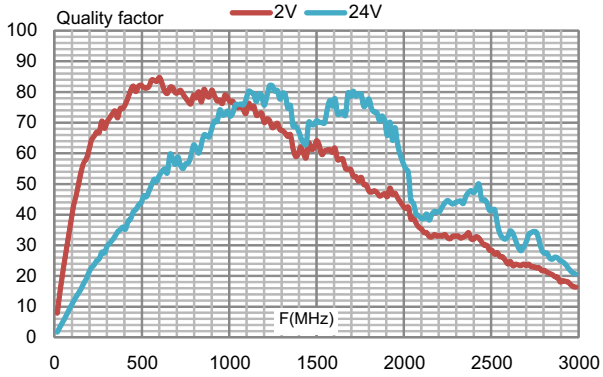


Figure 4. Harmonic power versus bias voltage (series)

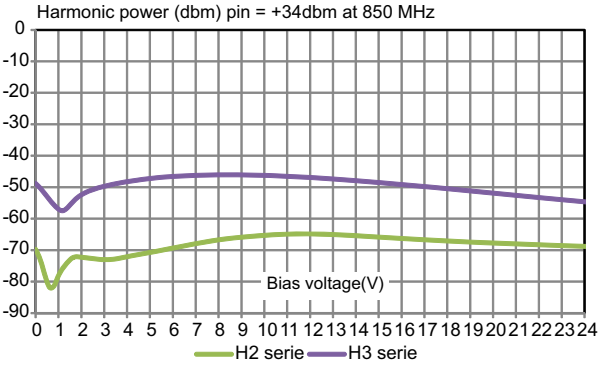


Figure 5. Harmonic power versus bias voltage (shunt)

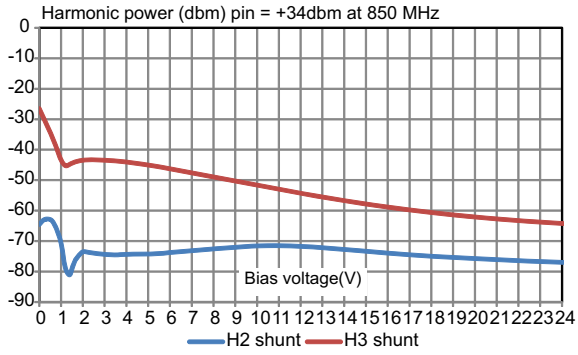
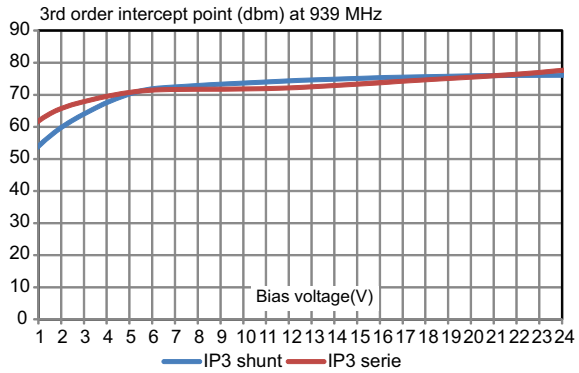


Figure 6. Third order intercept point (IP3)



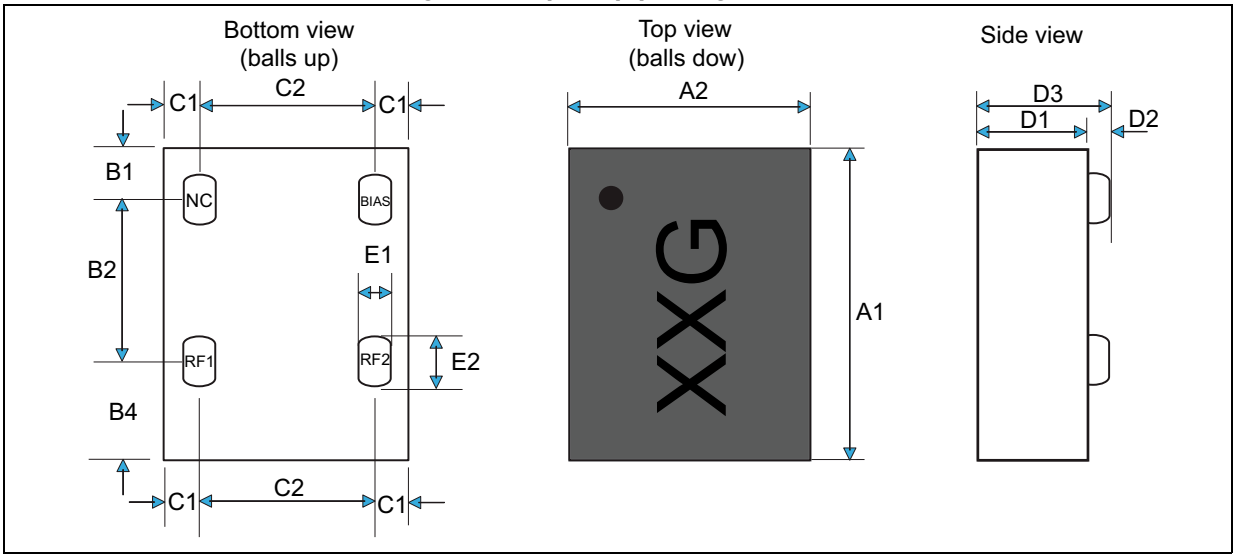
2 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

2.1 Flip-Chip package information

Figure 7. Flip-Chip package outline



The land pattern below is recommended for soldering the STPTIC-G2 on PCB.

NC stands for No Connect, this pad must not be connected on application board. Please leave this pad floating.

Table 4. Flip-Chip package dimensions

Dimensions (micron)	A1	A2	B1	B2	B4	C1	C2	D1	D2	D3	E1	E2
STPTIC-15/27/33/39/47G2	640	590	120	400	120	85	420	200	90	290	125	165
STPTIC-56G2	710				190							
STPTIC-68G2	780				260							
STPTIC-82G2	880				360							
Tolerance	±30	±30	±15	±10	±15	±15	±10	±20	±20	±40	±20	±20

Figure 8. Recommended PCB land pattern for Flip-Chip package

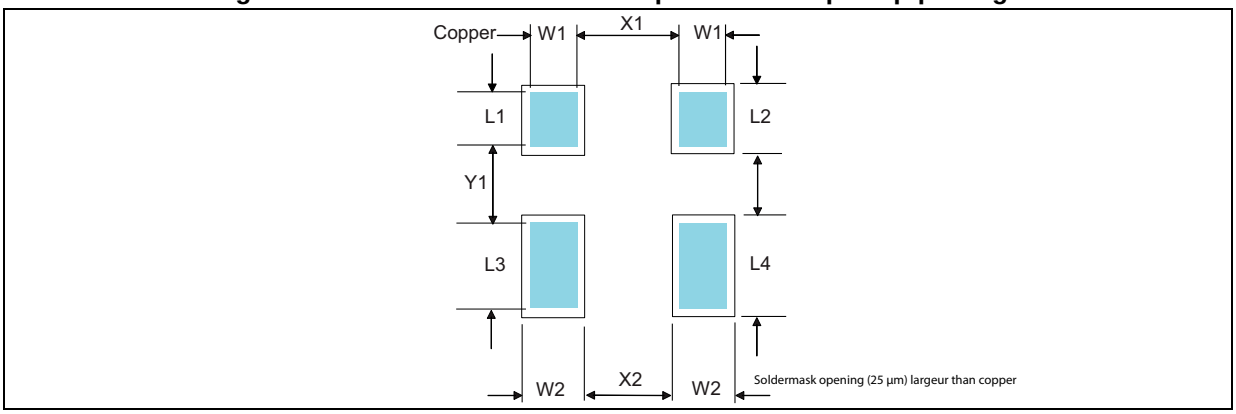


Table 5. Dimensions

Dimensions	L1	W1	L3	L2	W2	L4	X1	X2	Y1	Y2
Typical values (micron)	160	160	260	210	210	310	320	270	240	190

2.2 Packing information

Figure 9. Flip-Chip tape and reel outline

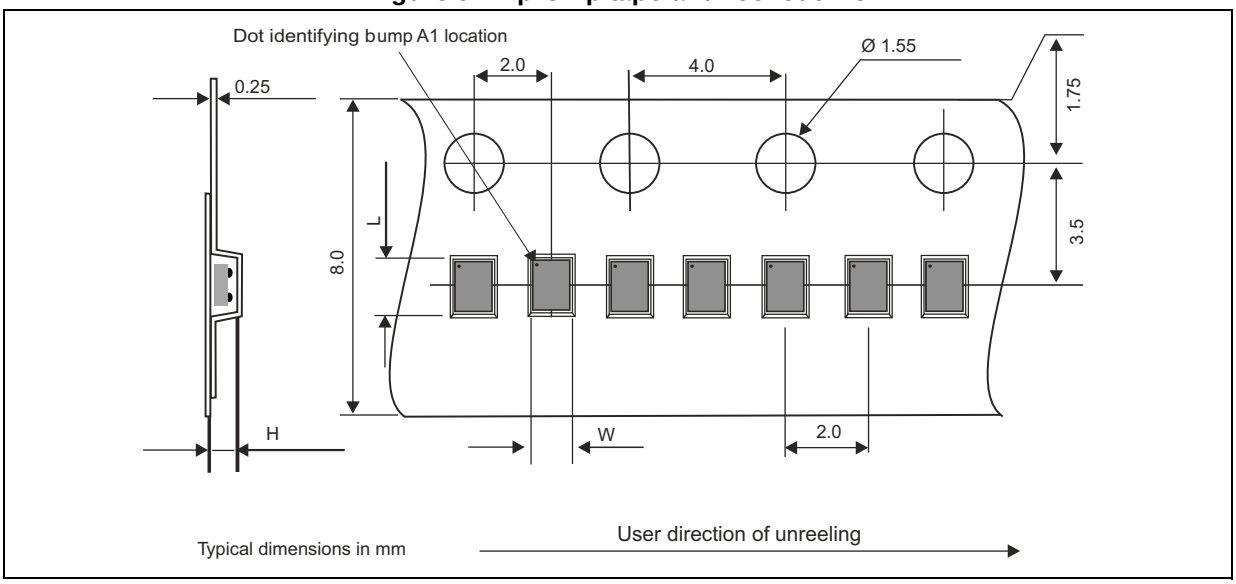


Table 6. Dimensions

Pocket dimensions	L	W	H
STPTIC-15/27/33/39/47G2	730	680	380
STPTIC-56G2	800	680	380
STPTIC-68G2	870	680	380
STPTIC-82G2	970	680	380

Figure 10. Flip-Chip marking

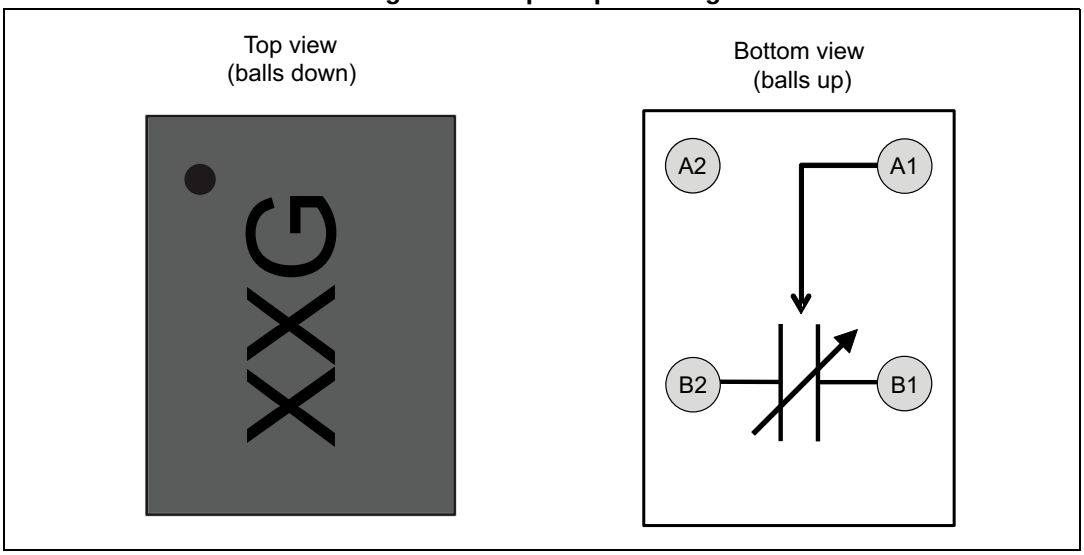


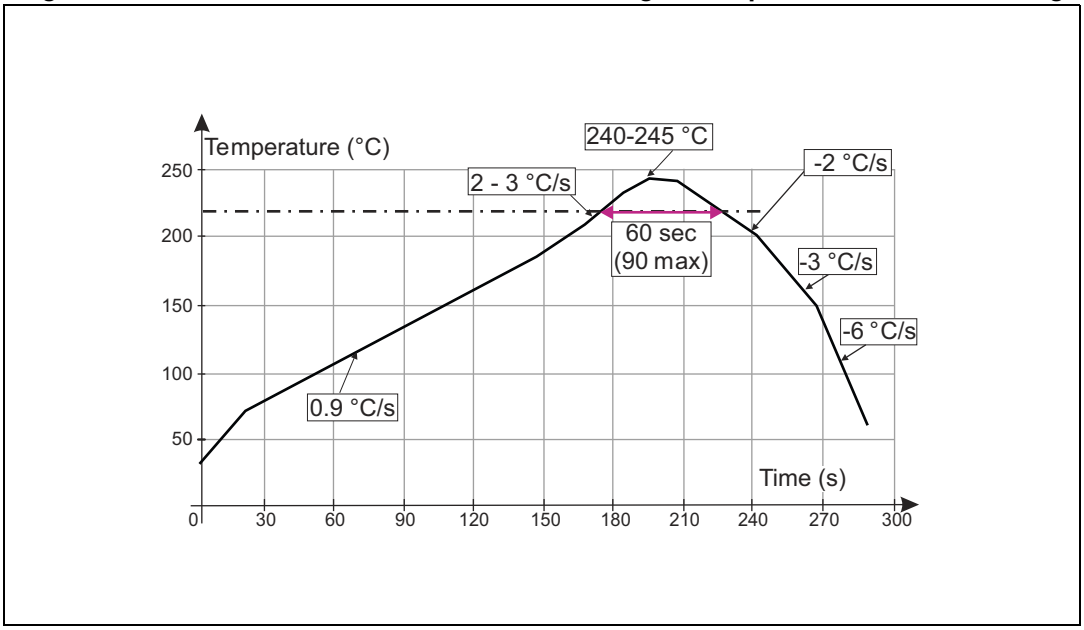
Table 7. Pinout description

Pad / ball number	Pin name	Description
A1	DC bias	DC bias voltage
B1	RF2	RF input / output(1)
A2	NC	Not connected
B2	RF1	RF input / output

1. When connected in shunt, please connect RF2 (B1 ball) to GND

3 Reflow profile

Figure 11. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 8. Recommended values for soldering reflow

Profile	Value	
	Typical	Max.
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s
Peak temperature in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

4 Evaluation board

Figure 12. Series and shunt connection

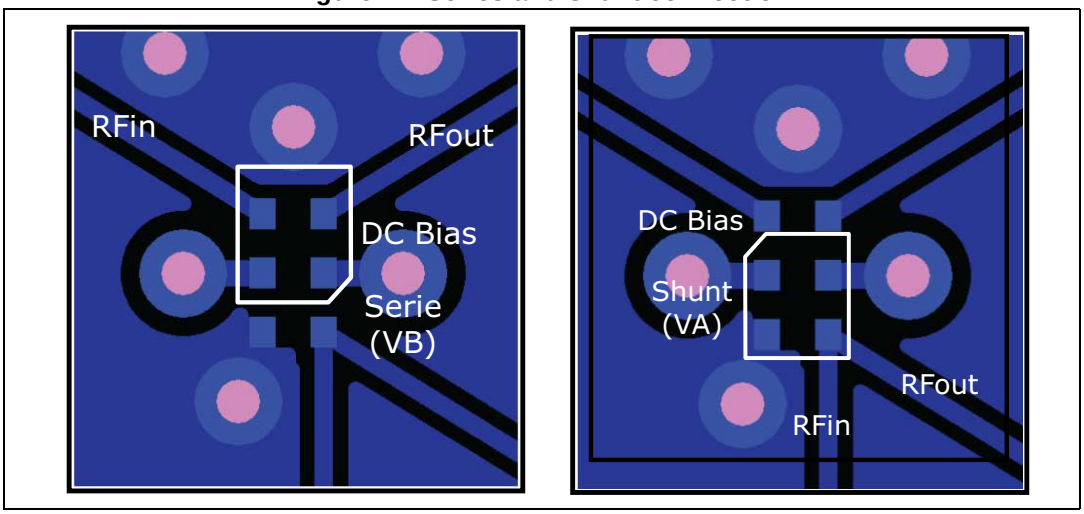


Figure 13. Layer 1 and layer 4

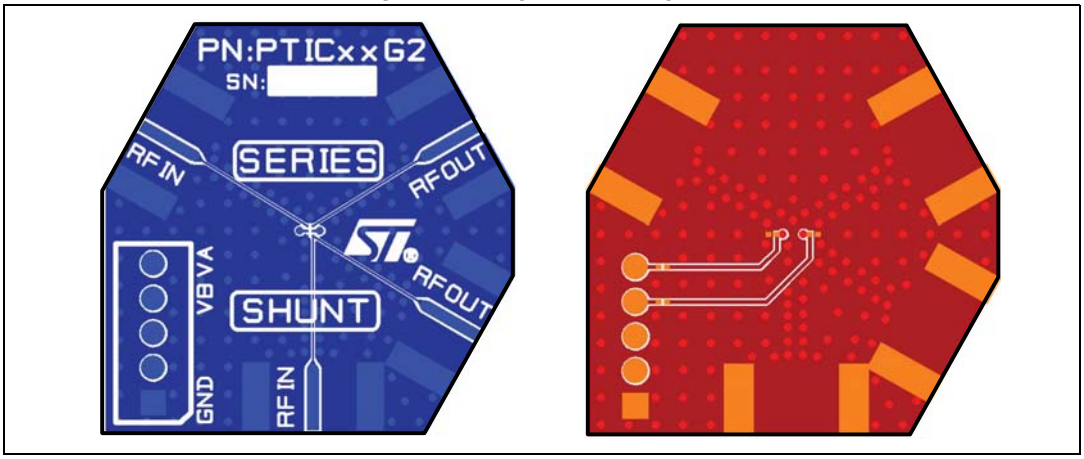
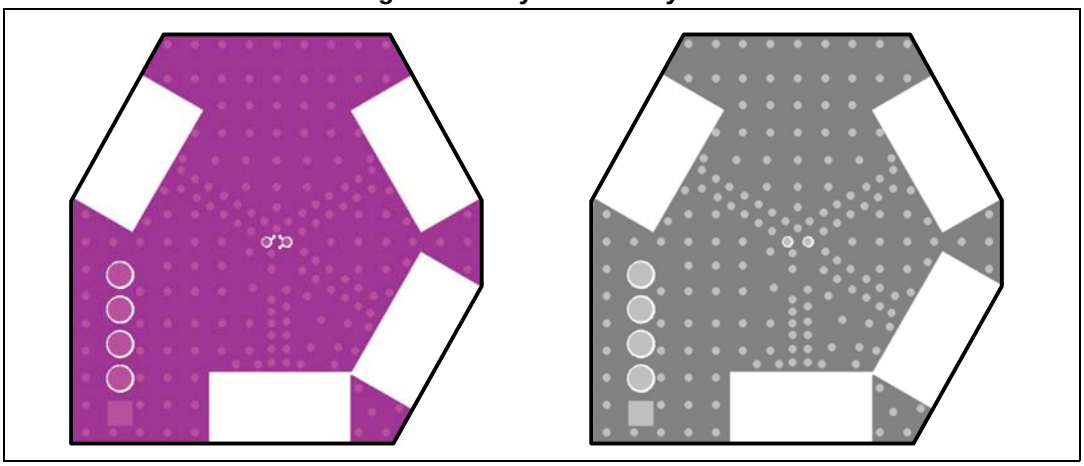


Figure 14. Layer 2 and layer 3



5 Ordering information

Figure 15. Ordering information scheme

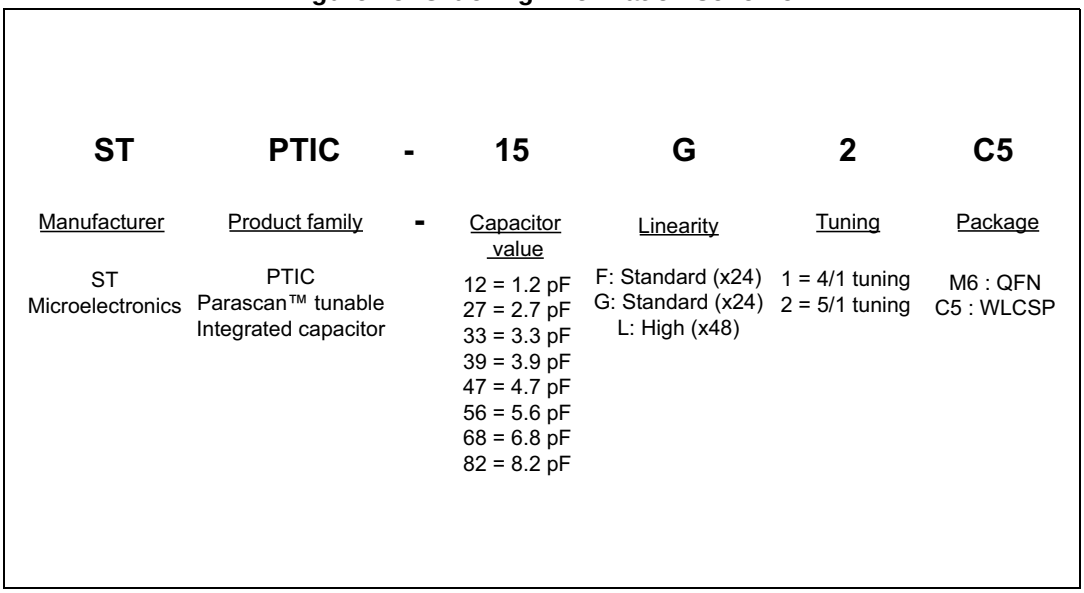


Table 9. Ordering information

Part number	Marking	Base qty	Package	Delivery mode
STPTIC-68G2C5	68G	15 000	Flip-Chip	Tape and reel

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Jul-2015	1	Initial release.

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