

74ALVT16827

20-bit buffer/line driver; non-inverting; 3-state

Rev. 4 — 24 January 2018

Product data sheet

1 General description

The 74ALVT16827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive. It is designed for V_{CC} operation at 2.5 V or 3.3 V with I/O compatibility to 5 V.

The 74ALVT16827 20-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($n\overline{OE}0$ and $n\overline{OE}1$) for maximum control flexibility.

2 Features and benefits

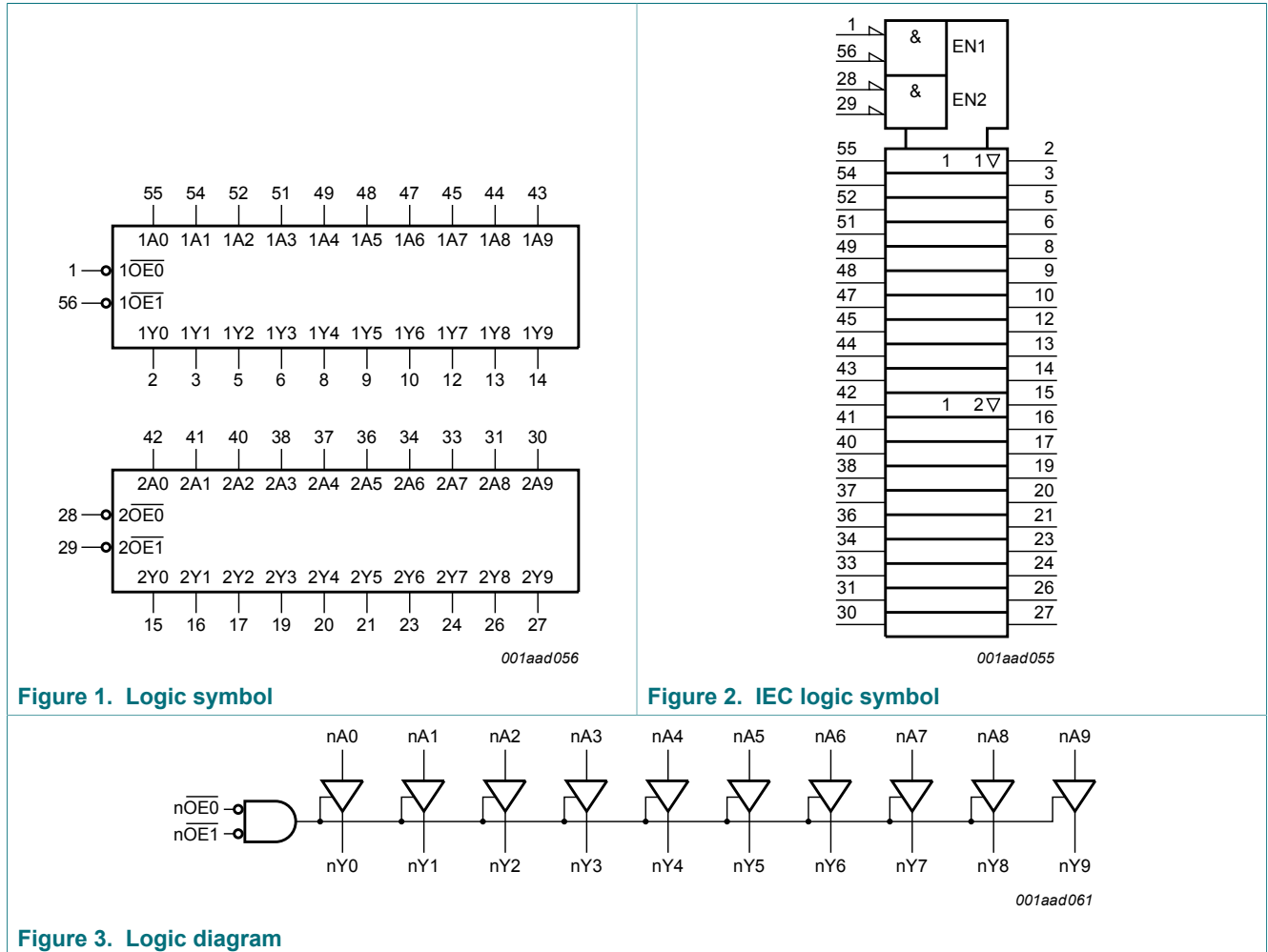
- Multiple V_{CC} and GND pins minimize switching noise
- 5 V I/O compatible
- Live insertion and extraction permitted
- 3-state output buffers
- Power-up 3-state
- Output capability: +64 mA and -32 mA
- Latch-up protection:
 - JESD 78 exceeds 500 mA
- ESD protection:
 - MIL STD 883 Method 3015: exceeds 2000 V
 - MM: exceeds 200 V
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs.

3 Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|----------------|-------------------|---------|--|----------|
| | Temperature range | Name | Description | |
| 74ALVT16827DGG | -40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

4 Functional diagram



5 Pinning information

5.1 Pinning

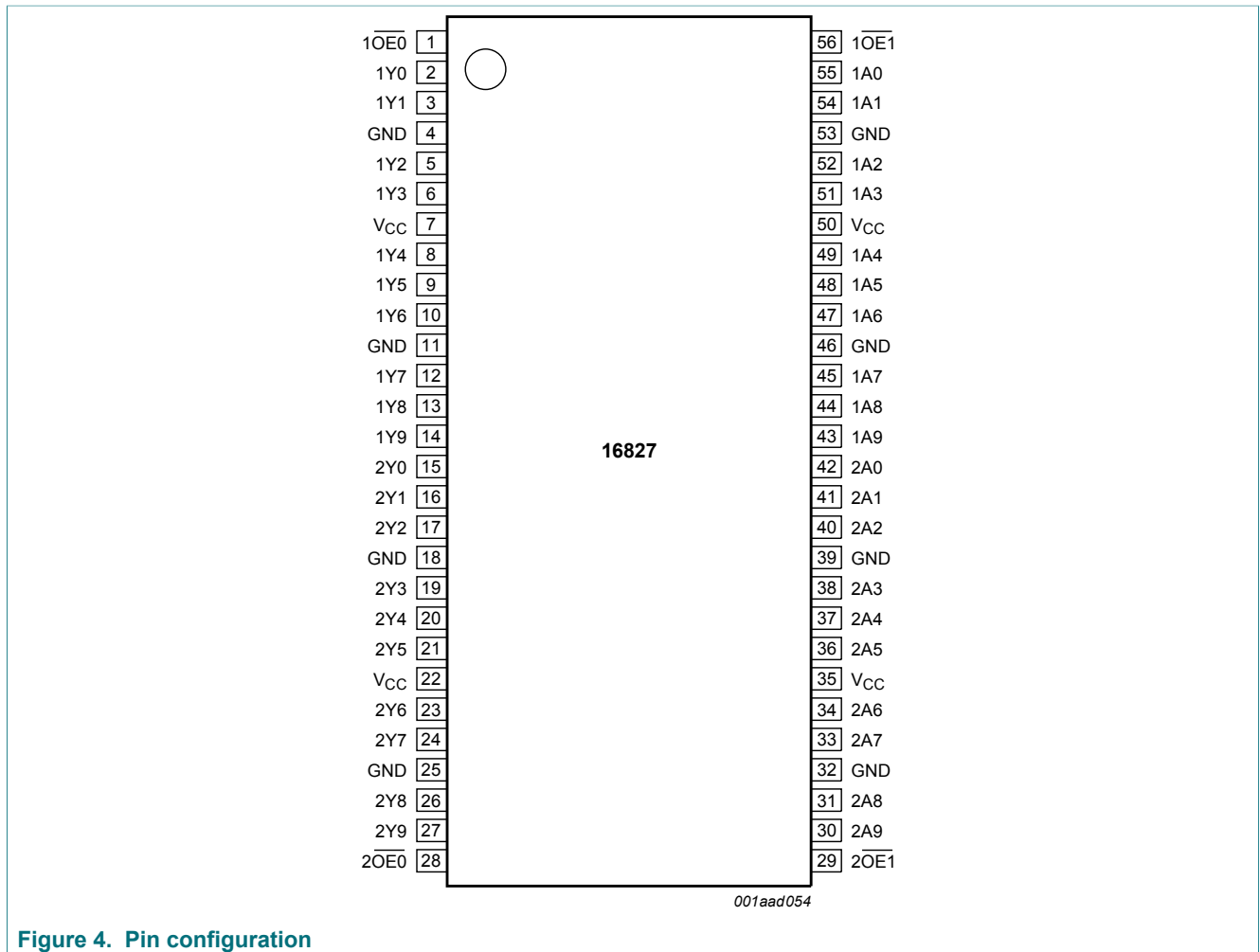


Figure 4. Pin configuration

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|--|-----------------------------------|
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8, 1A9 | 55, 54, 52, 51, 49, 48, 47, 45, 44, 43 | data input |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8, 2A9 | 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | data input |
| 1Y0, 1Y1, 1Y2, 1Y3, 1Y4, 1Y5, 1Y6, 1Y7, 1Y8, 1Y9 | 2, 3, 5, 6, 8, 9, 10, 12, 13, 14 | data output |
| 2Y0, 2Y1, 2Y2, 2Y3, 2Y4, 2Y5, 2Y6, 2Y7, 2Y8, 2Y9 | 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | data output |
| $1\overline{OE}0$, $1\overline{OE}1$, $2\overline{OE}0$, $2\overline{OE}1$ | 1, 56, 28, 29 | output enable inputs (active-LOW) |
| GND | 4, 11, 18, 25, 32, 39, 46, 53 | ground (0 V) |
| V _{CC} | 7, 22, 35, 50 | positive voltage supply |

6 Functional description

Table 3. Function table ^[1]

| Input | | Output | Operating mode |
|-------|-----|--------|----------------|
| nOEn | nAn | nYn | |
| L | L | L | transparent |
| L | H | H | transparent |
| H | X | Z | High-impedance |

[1] X = don't care; Z = High-impedance OFF-state; H = HIGH voltage level; L = LOW voltage level.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-----------------------------|---------------------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| V _I | input voltage | | ^[1] -1.2 | +7.0 | V |
| V _O | output voltage | output in OFF or HIGH-state | ^[1] -0.5 | +5.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -18 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| T _j | junction temperature | | ^[2] - | 150 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8 Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | Unit |
|------------------|-------------------------------------|---|---------------------------------|-----|---------------------------------|-----|------|
| | | | Min | Max | Min | Max | |
| V _{CC} | supply voltage | | 2.3 | 2.7 | 3.0 | 3.6 | V |
| V _I | input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| I _{OH} | HIGH-level output current | | - | -8 | - | -32 | mA |
| I _{OL} | LOW-level output current | none | - | 8 | - | 32 | mA |
| | | current duty cycle ≤ 50 %; f ≥ 1 kHz | - | 24 | - | 64 | mA |
| Δt/ΔV | input transition rise and fall rate | outputs enabled | - | 10 | - | 10 | ns/V |
| T _{amb} | ambient temperature | | -40 | +85 | -40 | +85 | °C |

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; T_{amb} = -40 °C to +85 °C; voltages are referred to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---------------------------------------|---------------------------|--|-----------------------|--------------------|------|------|
| V_{CC} = 2.5 V ± 0.2 V | | | | | | |
| V _{IK} | input clamping voltage | V _{CC} = 2.3 V; I _{IK} = -18 mA | - | -0.85 | -1.2 | V |
| V _{IH} | HIGH-level input voltage | | 1.7 | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.7 | V |
| V _{OH} | HIGH-level output voltage | V _{CC} = 2.3 V to 2.7 V; I _O = -100 μA | V _{CC} - 0.2 | V _{CC} | - | V |
| | | V _{CC} = 2.3 V; I _O = -8 mA | 1.8 | 2.1 | - | V |
| V _{OL} | LOW-level output voltage | V _{CC} = 2.3 V; I _O = 100 μA | - | 0.07 | 0.2 | V |
| | | V _{CC} = 2.3 V; I _O = 24 mA | - | 0.3 | 0.5 | V |
| I _I | input leakage current | all pins | | | | |
| | | V _{CC} = 0 V or 2.7 V; V _I = 5.5 V | - | 0.1 | 10 | μA |
| | | control pins | | | | |
| | | V _{CC} = 2.7 V; V _I = V _{CC} or GND | - | 0.1 | ±1 | μA |
| | | data pins ^[2] | | | | |
| | | V _{CC} = 2.7 V; V _I = V _{CC} | - | 0.1 | 1 | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 2.7 V; V _I = 0 V | - | 0.1 | -5 | μA |
| | | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 0.1 | ±100 | μA |
| I _{BHL} | bus hold LOW current | V _{CC} = 2.5 V; V _I = 0.8 V | - | 115 | - | μA |
| I _{BHH} | bus hold HIGH current | V _{CC} = 2.5 V; V _I = 2.0 V | - | -10 | - | μA |

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|------------------------------------|--|----------------|--------------------|-----------|---------------|
| I_{EX} | external current | output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 2.3\text{ V}$ | - | 10 | 125 | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V to } V_{CC}$; $V_I = \text{GND or } V_{CC}$; $n\overline{OE}n = \text{don't care}$ ^[3] | - | 1 | 100 | μA |
| I_{OZ} | OFF-state output current | $V_{CC} = 2.7\text{ V}$; $V_I = V_{IL}$ or V_{IH} | | | | |
| | | output HIGH; $V_O = 2.3\text{ V}$ | - | 0.5 | 5 | μA |
| | | output LOW; $V_O = 0.5\text{ V}$ | - | 0.5 | -5 | μA |
| I_{CC} | supply current | $V_{CC} = 2.7\text{ V}$; $V_I = \text{GND or } V_{CC}$; $I_O = 0\text{ A}$ | | | | |
| | | outputs HIGH | - | 0.04 | 0.1 | mA |
| | | outputs LOW | - | 3.6 | 5.0 | mA |
| | | outputs disabled ^[4] | - | 0.04 | 0.1 | mA |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 2.3\text{ V to } 2.7\text{ V}$; one input at $V_{CC} - 0.6\text{ V}$; other inputs at V_{CC} or GND ^[5] | - | 0.04 | 0.4 | mA |
| C_I | input capacitance | $V_I = 0\text{ V or } V_{CC}$ | - | 3 | - | pF |
| C_O | output capacitance | $V_O = 0\text{ V or } V_{CC}$ | - | 9 | - | pF |
| $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | |
| V_{IK} | input clamping voltage | $V_{CC} = 3.0\text{ V}$; $I_{IK} = -18\text{ mA}$ | - | -0.85 | -1.2 | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_{CC} = 3.0\text{ V to } 3.6\text{ V}$; $I_O = -100\text{ }\mu\text{A}$ | $V_{CC} - 0.2$ | V_{CC} | - | V |
| | | $V_{CC} = 3.0\text{ V}$; $I_O = -32\text{ mA}$ | 2.0 | 2.3 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 3.0\text{ V}$ | | | | |
| | | $I_O = 100\text{ }\mu\text{A}$ | - | 0.07 | 0.2 | V |
| | | $I_O = 16\text{ mA}$ | - | 0.25 | 0.4 | V |
| | | $I_O = 32\text{ mA}$ | - | 0.3 | 0.5 | V |
| | | $I_O = 64\text{ mA}$ | - | 0.4 | 0.55 | V |
| I_I | input leakage current | control pins | | | | |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND | - | 0.1 | ± 1 | μA |
| | | $V_{CC} = 0\text{ V or } 3.6\text{ V}$; $V_I = 5.5\text{ V}$ | - | 0.1 | 10 | μA |
| | | data pins ^[2] | | | | |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ | - | 0.5 | 1 | μA |
| | | $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V}$ | - | 0.1 | -5 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V to } 4.5\text{ V}$ | - | 0.1 | ± 100 | μA |
| I_{BHL} | bus hold LOW current | data inputs; $V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$ | 75 | 130 | - | μA |
| I_{BHH} | bus hold HIGH current | data inputs; $V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$ | -75 | -140 | - | μA |
| I_{BHLO} | bus hold LOW overdrive current | data inputs; $V_{CC} = 3.6\text{ V}$; $V_I = 0\text{ V to } 3.6\text{ V}$ ^[6] | 500 | - | - | μA |

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------------------|------------------------------------|--|------|--------------------|------|------|
| I _{BHHO} | bus hold HIGH overdrive current | data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V ^[6] | -500 | - | - | μA |
| I _{EX} | external current | output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V | - | 10 | 125 | μA |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n \overline{OE} n = don't care ^[7] | - | 1 | ±100 | μA |
| I _{OZ} | OFF-state output current | V _{CC} = 3.6 V; V _I = V _{IL} or V _{IH} | | | | |
| | | output HIGH; V _O = 3.0 V | - | 0.5 | 5 | μA |
| | | output LOW; V _O = 0.5 V | - | 0.5 | -5 | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | |
| | | outputs HIGH | - | 0.07 | 0.1 | mA |
| | | outputs LOW | - | 4.2 | 6 | mA |
| | | outputs disabled ^[4] | - | 0.07 | 0.1 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V; other inputs at V _{CC} or GND ^[5] | - | 0.04 | 0.4 | mA |
| C _I | input capacitance | V _I = 0 V or V _{CC} | - | 3 | - | pF |
| C _O | output capacitance | V _O = 0 V or V _{CC} | - | 9 | - | pF |

- [1] All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
- [2] Unused pins at V_{CC} or GND.
- [3] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 2.5 V ± 0.2 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
- [4] I_{CC} with outputs disabled is measured with outputs pulled up to V_{CC} or pulled down to ground.
- [5] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- [6] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [7] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

10 Dynamic characteristics

Table 7. Dynamic characteristics

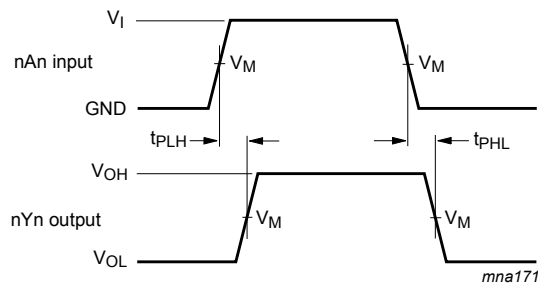
At recommended operating conditions; T_{amb} = -40 °C to +85 °C; Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---------------------------------------|-------------------------------------|--|-----|--------------------|-----|------|
| V_{CC} = 2.5 V ± 0.2 V | | | | | | |
| t _{PLH} | LOW to HIGH propagation delay | nAn to nYn; see Figure 5 | 1.0 | 2.0 | 2.9 | ns |
| t _{PHL} | HIGH to LOW propagation delay | nAn to nYn; see Figure 5 | 1.0 | 2.0 | 3.0 | ns |
| t _{PZH} | OFF-state to HIGH propagation delay | n \overline{OE} n to nYn; see Figure 6 | 2.0 | 3.2 | 5.5 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | n \overline{OE} n to nYn; see Figure 6 | 1.7 | 2.9 | 4.3 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | n \overline{OE} n to nYn; see Figure 6 | 1.8 | 2.8 | 5.1 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | n \overline{OE} n to nYn; see Figure 6 | 1.4 | 2.3 | 3.9 | ns |
| V_{CC} = 3.3 V ± 0.3 V | | | | | | |
| t _{PLH} | LOW to HIGH propagation delay | nAn to nYn; see Figure 5 | 0.7 | 1.5 | 2.2 | ns |
| t _{PHL} | HIGH to LOW propagation delay | nAn to nYn; see Figure 5 | 0.8 | 1.6 | 2.3 | ns |

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|------------------|-------------------------------------|---|-----|--------------------|-----|------|
| t _{PZH} | OFF-state to HIGH propagation delay | n \overline{OEn} to nYn; see Figure 6 | 1.6 | 2.6 | 3.8 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | n \overline{OEn} to nYn; see Figure 6 | 1.4 | 2.3 | 3.2 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | n \overline{OEn} to nYn; see Figure 6 | 2.3 | 3.2 | 4.8 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | n \overline{OEn} to nYn; see Figure 6 | 1.5 | 2.5 | 3.8 | ns |

[1] All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
 All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

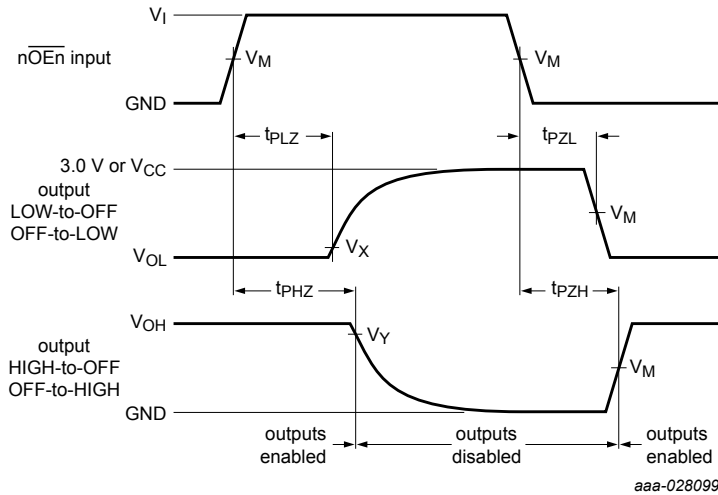
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Input (nAn) to output (nYn) propagation delays



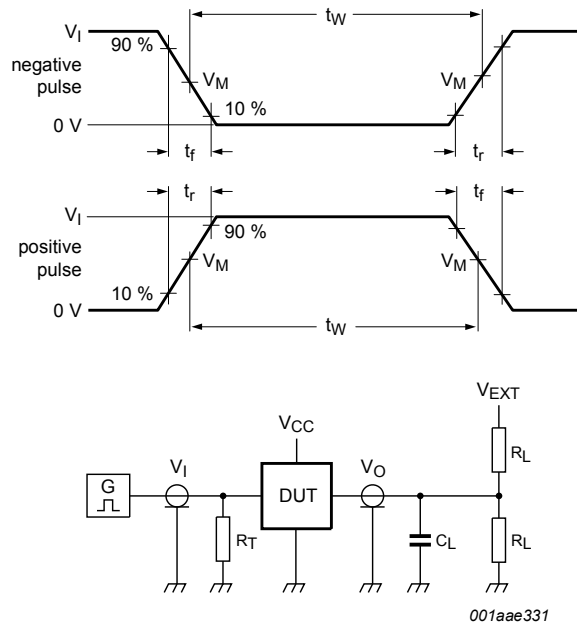
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. The 3-state output enable and disable times

Table 8. Measurement points

| V _{CC} | Input | | Output | | |
|-------------------------|-----------------|-----------------------|-----------------------|--------------------------|--------------------------|
| | V _I | V _M | V _M | V _X | V _Y |
| V _{CC} ≤ 2.7 V | V _{CC} | 0.5 x V _{CC} | 0.5 x V _{CC} | V _{OL} + 0.15 V | V _{OH} - 0.15 V |
| V _{CC} ≥ 3.0 V | 3.0 V | 1.5 V | 1.5 V | V _{OL} + 0.3 V | V _{OH} - 0.3 V |



Test data is given in [Table 9](#).

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Figure 7. Test circuit for measuring switching times

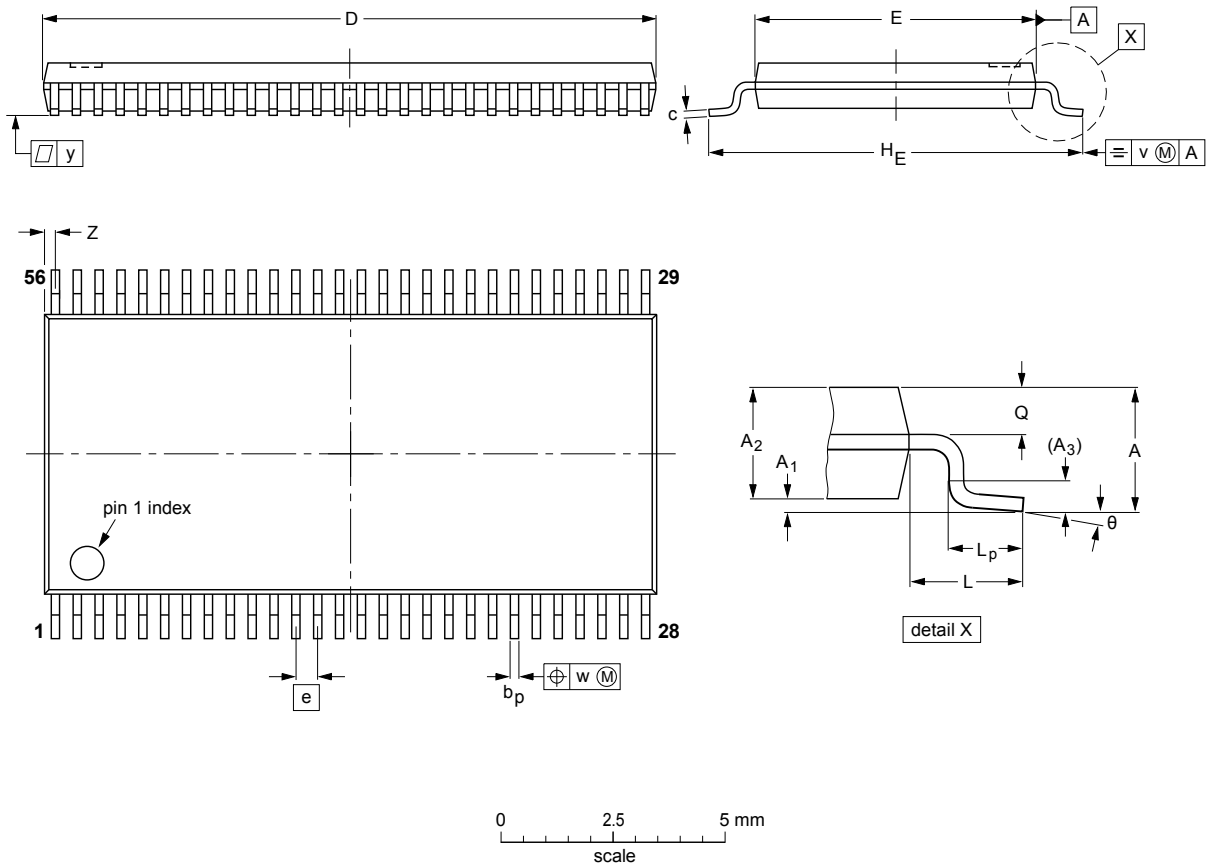
Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------------------------------------|---------------|--------|---------------|-------|--------------|--------------------|--------------------------|--------------------|
| V_I | f_i | t_W | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 3.0 V or V_{CC} whichever is less | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V or $V_{CC} \times 2$ | open |

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|-----|----------------|---|----------------|--------------|------|------|-----|------------|----------|
| mm | 1.2 | 0.15 0.05 | 1.05 0.85 | 0.25 | 0.28 0.17 | 0.2 0.1 | 14.1 13.9 | 6.2 6.0 | 0.5 | 8.3 7.9 | 1 | 0.8 0.4 | 0.50 0.35 | 0.25 | 0.08 | 0.1 | 0.5 0.1 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|-------|---------------------|----------------------|
| | IEC | JEDEC | JEITA | | |
| SOT364-1 | | MO-153 | | | 99-12-27 03-02-19 |

Figure 8. Package outline SOT364-1 (TSSOP56)

12 Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| BICMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| MIL | Military |
| MM | Machine Model |

13 Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--|-----------------------|---------------|-----------------|
| 74ALVT16827 v.4 | 20180124 | Product data sheet | - | 74ALVT16827 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74ALVT16827DL (SOT371-1 / SSOP56) removed. | | | |
| 74ALVT16827 v.3 | 20050602 | Product data sheet | - | 74ALVT16827 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 2: modified 'JEDEC Std 17' into 'JESD78'. Section 10: changed values in column 'min' | | | |
| 74ALVT16827 v.2 | 19980213 | Product specification | - | 74ALVT16827 v.1 |
| 74ALVT16827 v.1 | 19960619 | Product specification | - | - |

14 Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com

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