ACPL-C797

Optically Isolated Sigma-Delta Modulator

Preliminary Data Sheet

Description

The ACPL-C797 is a 1-bit, second-order sigma-delta (Σ-Δ) modulator converts an analog input signal into a high-speed data stream with galvanic isolation based on optical coupling technology. The ACPL-C797 operates from a 5 V power supply with dynamic range of 80 dB with an appropriate digital filter. The differential inputs of ±200 mV (full scale ±320 mV) are ideal for direct connection to shunt resistors or other low-level signal sources in applications such as motor phase current measurement.

The analog input is continuously sampled by a means of sigma-delta over-sampling using an on-board clock. The signal information is contained in the modulator data, as a density of ones with data rate of 10 MHz, and the data are encoded and transmitted across the isolation boundary where they are recovered and decoded into high-speed data stream of digital ones and zeros. The original signal information can be reconstructed with a digital filter. The serial interface for data and clock has a wide supply range of 3 V to 5.5 V.

Combined with superior optical coupling technology, the modulator delivers high noise margins and excellent immunity against isolation-mode transients. With 0.5 mm minimum distance through insulation (DTI), the ACPL-C797 provides reliable reinforced insulation and high working insulation voltage, which is suitable for fail-safe designs. This outstanding isolation performance is superior to alternatives including devices based on capacitive- or magnetic-coupling with DTI in micro-meter range. Offered in a Stretched SO-8 (SSO-8) package, the isolated ADC delivers the reliability, small size, superior isolation and over-temperature performance motor drive designers need to accurately measure current at much lower price compared to traditional current transducers.

The external clock version modulator ACPL-796J (SO-16 package) is also available.

Features

- 10 MHz internal clock
- 1-bit, second-order sigma-delta modulator
- 16 bits resolution no missing codes (12 bits ENOB)
- 78 dB SNR
- 4.5 μV/°C maximum offset drift
- ±1% gain error
- Internal reference voltage
- ±200 mV linear range with single 5 V supply (±320 mV full scale)
- 3 V to 5.5 V wide supply range for digital interface
- -40°C to +105°C operating temperature range
- SSO-8 package
- 25 kV/μs common-mode transient immunity
- Safety and regulatory approval (pending):
  - IEC/EN/DIN EN 60747-5-5: 1140 Vpeak working insulation voltage
  - UL 1577: 5000 Vrms/1min isolation voltage
  - CSA: Component Acceptance Notice #5

Applications

- Motor phase and rail current sensing
- Power inverter current and voltage sensing
- Industrial process control
- Data acquisition systems
- General purpose current and voltage sensing
- Traditional current transducer replacements

This preliminary data is provided to assist you in the evaluation of product(s) currently under development. Until Avago Technologies releases this product for general sales, Avago Technologies reserves the right to alter prices, specifications, features, capabilities, functions, release dates, and remove availability of the product(s) at anytime.

***CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Functional Block Diagram

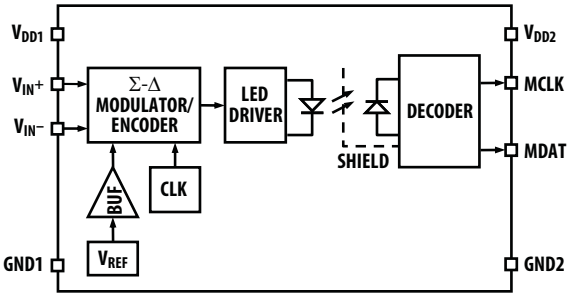


Figure 1.

Pin Configuration and Descriptions

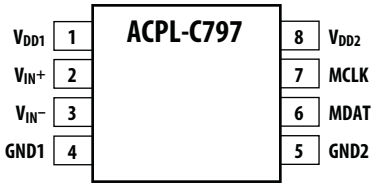


Figure 2. Pin configuration.

Table 1. Pin descriptions.

Pin No.	Symbol	Description
1	V_{DD1}	Supply voltage for signal input side (analog side), relative to GND1
2	V_{IN+}	Positive analog input, recommended input range ±200 mV
3	V_{IN-}	Negative analog input, recommended input range ±200 mV (normally connected to GND1)
4	GND1	Supply ground for signal input side
5	GND2	Supply ground for data/clock output side (digital side)
6	MDAT	Modulator data output
7	MCLK	Modulator clock output
8	V_{DD2}	Supply voltage for data output side, relative to GND2

Ordering Information

ACPL-C797 is UL recognized with 5000 Vrms/1 minute rating per UL 1577 (pending).

Table 2.

Part number	Option (RoHS Compliant)	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-C797	-000E	Stretched SO-8	X		X	80 per tube
	-500E		X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

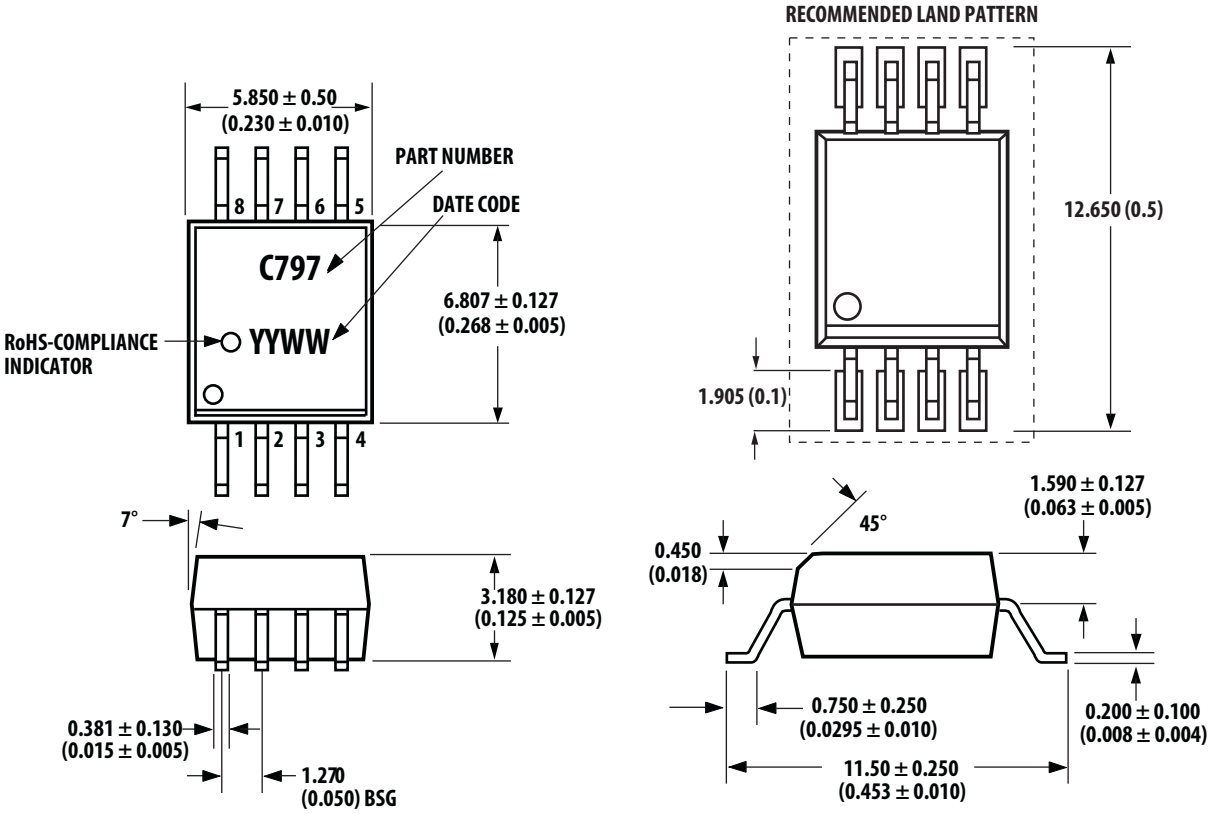
Example:

ACPL-C797-500E to order product of Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval and RoHS compliance.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Drawings

Stretched SO-8 Package (SSO-8)



Dimensions in millimeters and (inches).
Lead coplanarity = 0.1 mm (0.004 inches).

Figure 3.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non- Halide Flux should be used.

Regulatory Information

The ACPL-C797 is pending for approvals by the following organizations:

IEC/EN/DIN EN 60747-5-5

Approved with Maximum Working Insulation Voltage V_{IORM} = 1140 Vpeak.

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 5000 Vrms/1min. File E55361.

CSA

Approval under CSA Component Acceptance Notice #5, File CA 88324.

Table 3. IEC/EN/DIN EN 60747-5-5 Insulation Characteristics[1]

Description	Symbol	Value	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – IV	
for rated mains voltage ≤ 450 V_{rms}		I – III	
for rated mains voltage ≤ 600 V_{rms}		I – III	
for rated mains voltage ≤ 1000 V_{rms}		I – II	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	1140	Vpeak
Input to Output Test Voltage, Method b V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	2137	Vpeak
Input to Output Test Voltage, Method a V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	1824	Vpeak
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	8000	Vpeak
Safety-limiting values (Maximum values allowed in the event of a failure)			
Case Temperature	T_S	175	°C
Input Current[2]	$I_{S, INPUT}$	230	mA
Output Power[2]	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

Notes:
1. Insulation characteristics are guaranteed only within the safety maximum ratings, which must be ensured by protective circuits within the application.
2. Safety-limiting parameters are dependent on ambient temperature. The Input Current, $I_{S,INPUT}$, derates linearly above 25°C free-air temperature at a rate of 2.53 mA/°C; the Output Power, $P_{S,OUTPUT}$, derates linearly above 25°C free-air temperature at a rate of 4 mW/°C.

Table 4. Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-55	+125	°C
Ambient Operating Temperature	T_A	-40	+105	°C
Supply Voltage	V_{DD1}, V_{DD2}	-0.5	6.0	V
Steady-State Input Voltage[1,3]	V_{IN}+, V_{IN}–	-2	V_{DD1} + 0.5	V
Two-Second Transient Input Voltage[2]	V_{IN}+, V_{IN}–	-6	V_{DD1} + 0.5	V
Digital Output Voltages	MCLK, MDAT	-0.5	V_{DD2} +0.5	V
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane			

Notes:
1. DC voltage of up to -2 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
2. Transient voltage of 2 seconds up to -6 V on the inputs does not cause latch-up or damage to the device; tested at typical operating conditions.
3. Absolute maximum DC current on the inputs = 100 mA, no latch-up or device damage occurs.

Table 6. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Ambient Operating Temperature	T_A	-40	+105	°C
V_{DD1} Supply Voltage	V_{DD1}	4.5	5.5	V
V_{DD2} Supply Voltage	V_{DD2}	3	5.5	V
Analog Input Voltage[1]	V_{IN}+, V_{IN}–	-200	+200	mV

Notes:
1. Full scale signal input range ±320 mV.

Table 7. Electrical Specifications

Unless otherwise noted, T_A = -40°C to +105°C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V, V_{IN}+ = -200 mV to +200 mV, and V_{IN}– = 0 V (single-ended connection); tested with Sinc^3 filter, 256 decimation ratio.

Parameter	Symbol	Min.	Typ.[1]	Max.	Units	Test Conditions/Notes	Fig.
STATIC CHARACTERISTICS							
Resolution		16			Bits	Decimation filter output set to 16 bits	
Integral Nonlinearity	INL	-15	3	15	LSB	T_A = –40°C to +85°C; see Definitions section	
		-25	3	25	LSB	T_A = 85°C to 105°C	
Differential Nonlinearity	DNL	-0.9		0.9	LSB	No missing codes, guaranteed by design; see Definitions section	
Offset Error	V_{OS}	-1	0.3	2	mV	T_A = –40°C to +105°C; see Definitions section	
Offset Drift vs. Temperature	TCV_{OS}		1.5	4.5	µV/°C	V_{DD1} = 5 V	
Offset Drift vs. V_{DD1}			250		µV/V		
Internal Reference Voltage	V_{REF}		320		mV		
Reference Voltage Tolerance	G_E	-1		1	%	T_A = 25°C, V_{IN}+ = –320 to +320 mV; see Definitions section	
		-2		2	%	T_A = –40°C to +105°C, V_{IN}+ = –320 to +320 mV	
V_{REF} Drift vs. Temperature	TCG_E		60		ppm/°C		
V_{REF} Drift vs. V_{DD1}			110		µV/V		
ANALOG INPUTS							
Full-Scale Differential Voltage Input Range	FSR		±320		mV	$V_{IN} = V_{IN}+ - V_{IN}–$; Note 2	
Average Input Bias Current	I_{INA}		-0.3		µA	V_{DD1} = 5V, V_{DD2} = 5V, V_{IN}+ = 0 V; Note 3	
Average Input Resistance	R_{IN}		24		kΩ	Across V_{IN}+ or V_{IN}– to GND1; Note 3	
Input Capacitance	C_{INA}		8		pF	Across V_{IN}+ or V_{IN}– to GND1	
DYNAMIC CHARACTERISTICS						V_{IN}+ = 400 mVpp, 1 kHz sine wave	
Signal-to-Noise Ratio	SNR	68	78		dB	T_A = –40°C to +105°C; see Definitions section	
Signal-to-(Noise + Distortion) Ratio	SNDR	65	75		dB	T_A = –40°C to +105°C; see Definitions section	
Effective Number of Bits	ENOB		12		Bits	see Definitions section	
Isolation Transient Immunity	CMR		25		kV/µV	V_{CM} = 1 kV; See Definitions section	
Common-Mode Rejection Ratio	CMRR		74		dB		
DIGITAL OUTPUTS							
Output High Voltage	V_{OH}	V_{DD2} – 0.2	V_{DD2} – 0.1		V	I_{OUT} = –200 µA	
Output Low Voltage	V_{OL}			0.6	V	I_{OUT} = +1.6 mA	
POWER SUPPLY							
V_{DD1} Supply Current	I_{DD1}		9	14	mA	V_{IN}+ = –320 mV to +320 mV	
V_{DD2} Supply Current	I_{DD2}		5.2	8	mA	V_{DD2} = 5 V supply	
			4.6	7	mA	V_{DD2} = 3.3 V supply	

Notes:
1. All Typical values are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 5 V.
2. Beyond the full-scale input range the data output is either all zeroes or all ones.
3. Because of the switched-capacitor nature of the isolated modulator, time averaged values are shown.

Table 8. Timing Specifications

Unless otherwise noted, T_A = -40°C to +105°C, V_{DD1} = 4.5 V to 5.5 V, V_{DD2} = 3 V to 5.5 V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions/Notes	Fig.
Modulator Clock Output Frequency	f_{MCLK}	9	10	11	MHz	Clock duty cycle 40% to 60%	
Data Delay After Rising Edge of MCLK	t_D	14	25	35	ns	C_L = 15 pF	4

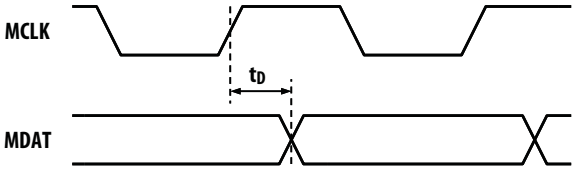


Figure 4. Data timing.

Table 9. Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	5000			Vrms	RH < 50%, t = 1 min, T_A = 25°C	1, 2
Input-Output Resistance	R_{I-O}		$>10^{12}$		Ω	V_{I-O} = 500 Vdc	3
Input-Output Capacitance	C_{I-O}		0.5		pF	f =1 MHz	3

Notes:

1. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA). This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
2. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 insulation characteristics table and your equipment level safety specification.
3. This is a two-terminal measurement: pins 1–4 are shorted together and pins 5–8 are shorted together.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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