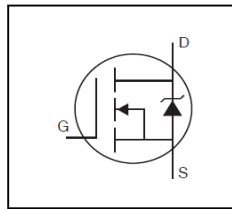


**Features**

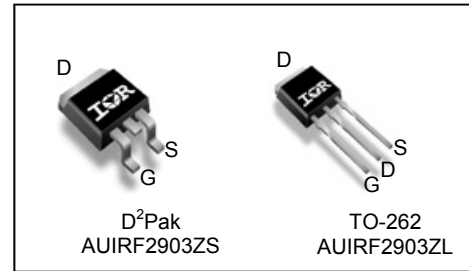
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*



$V_{DSS}$	<b>30V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>1.9mΩ</b>
	<b>max.</b>
$I_D$ (Silicon Limited)	<b>235A<sup>Ⓞ</sup></b>
$I_D$ (Package Limited)	<b>160A</b>

**Description**

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF2903ZL	TO-262	Tube	50	AUIRF2903ZL
AUIRF2903ZS	D²-Pak	Tube	50	AUIRF2903ZS
		Tape and Reel Left	800	AUIRF2903ZSTRL

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	235 <sup>Ⓞ</sup>	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	166 <sup>Ⓞ</sup>	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	160	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	1020	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	231	W
	Linear Derating Factor	1.54	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) <sup>②</sup>	231	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value <sup>⑥</sup>	820	
$I_{AR}$	Avalanche Current <sup>①</sup>	See Fig.15,16, 12a, 12b	A
$E_{AR}$	Repetitive Avalanche Energy <sup>⑤</sup>		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>⑧</sup>	—	0.65	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—	62	
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mount, steady state) <sup>⑦</sup>		40	

HEXFET® is a registered trademark of Infineon.

\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.021	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	1.9	2.4	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A ③ ⑩
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
g <sub>fs</sub>	Forward Trans conductance	120	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 75A⑩
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
		—	—	250	μA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200	nA	V <sub>GS</sub> = -20V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

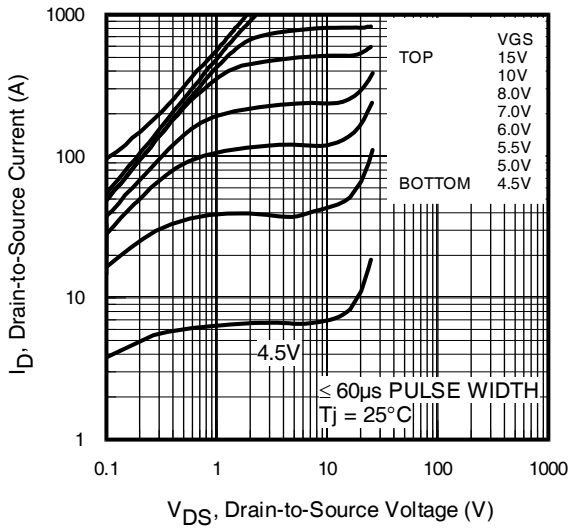
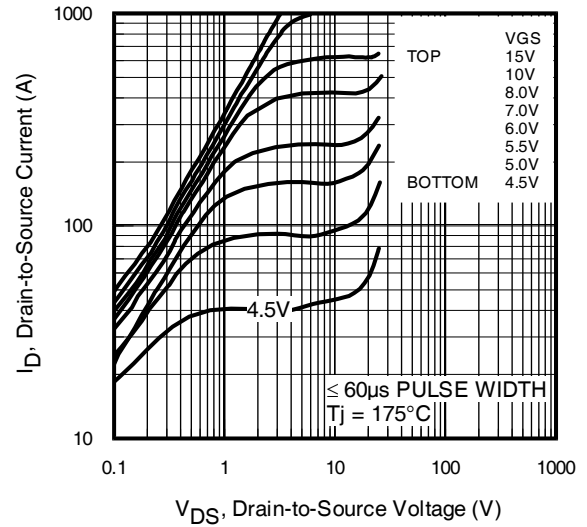
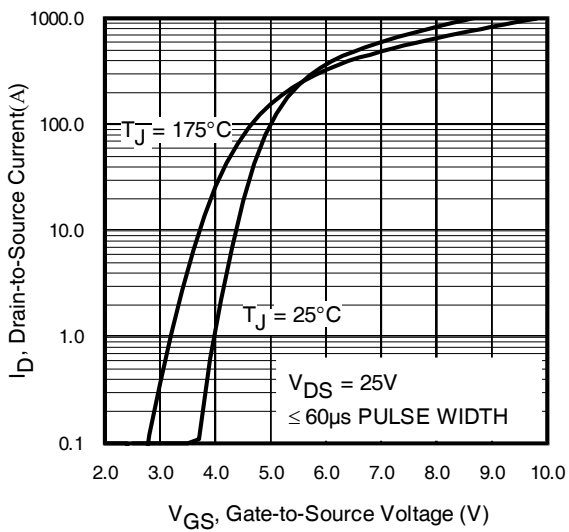
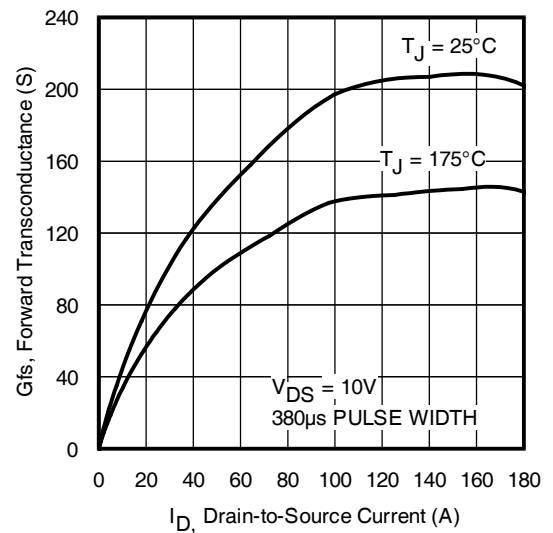
Q <sub>g</sub>	Total Gate Charge	—	160	240	nC	I <sub>D</sub> = 75A⑩
Q <sub>gs</sub>	Gate-to-Source Charge	—	51	—		V <sub>DS</sub> = 24V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	58	—		V <sub>GS</sub> = 10V③
t <sub>d(on)</sub>	Turn-On Delay Time	—	24	—	ns	V <sub>DD</sub> = 15V
t <sub>r</sub>	Rise Time	—	100	—		I <sub>D</sub> = 75A⑩
t <sub>d(off)</sub>	Turn-Off Delay Time	—	48	—		R <sub>G</sub> = 3.2Ω
t <sub>f</sub>	Fall Time	—	37	—		V <sub>GS</sub> = 10V ③
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact.
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	6320	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1980	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	1100	—		f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance	—	5930	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	2010	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 24V f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	3050	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 24V ④

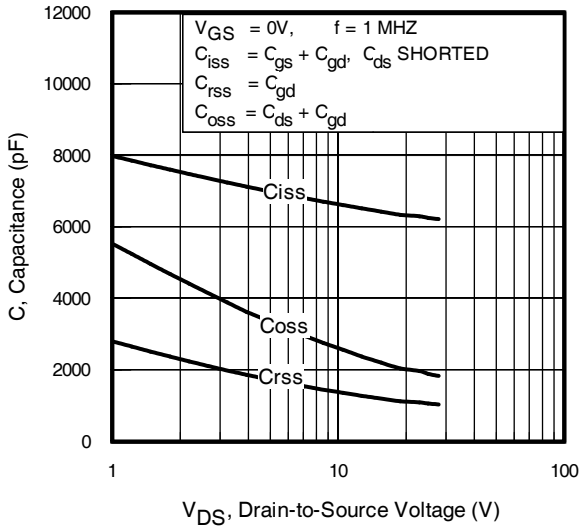
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	160⑨	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	1020		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A⑩, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	34	51	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 75A⑩, V <sub>DD</sub> = 15V
Q <sub>rr</sub>	Reverse Recovery Charge	—	29	44	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

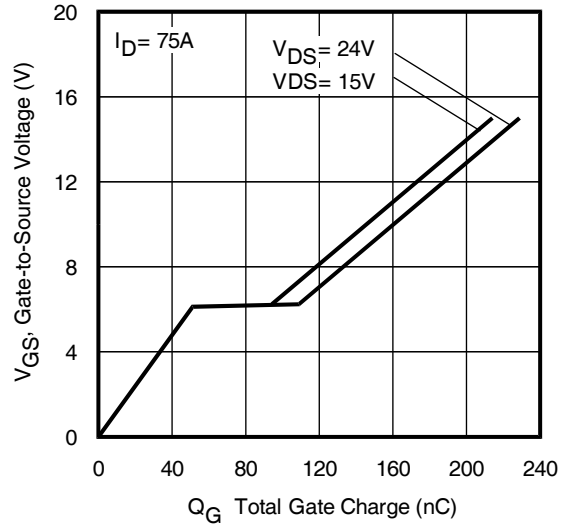
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.10mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 75A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ④ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑤ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population, 100% tested to this value in production.
- ⑦ This is applied to D<sup>2</sup>Pak When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C
- ⑨ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 160A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)
- ⑩ All AC and DC test condition based on old Package limitation current = 75A.

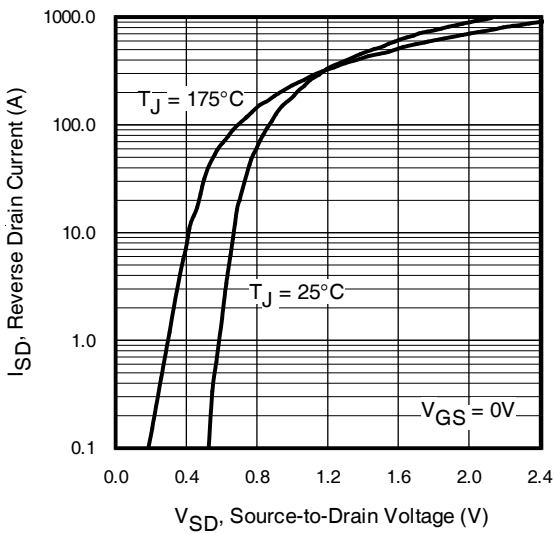

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Typical Forward Transconductance vs. Drain Current



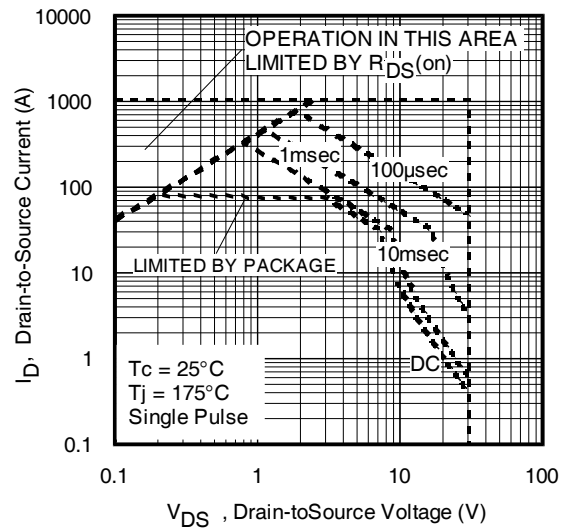
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



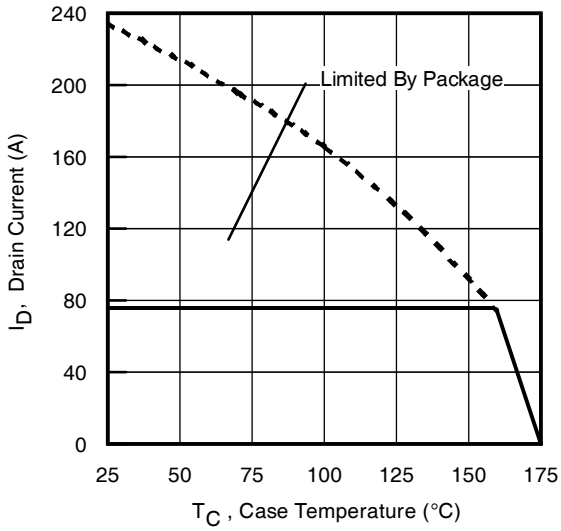
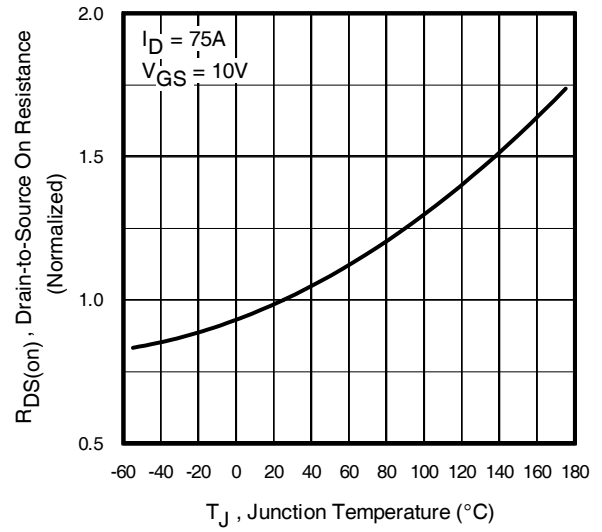
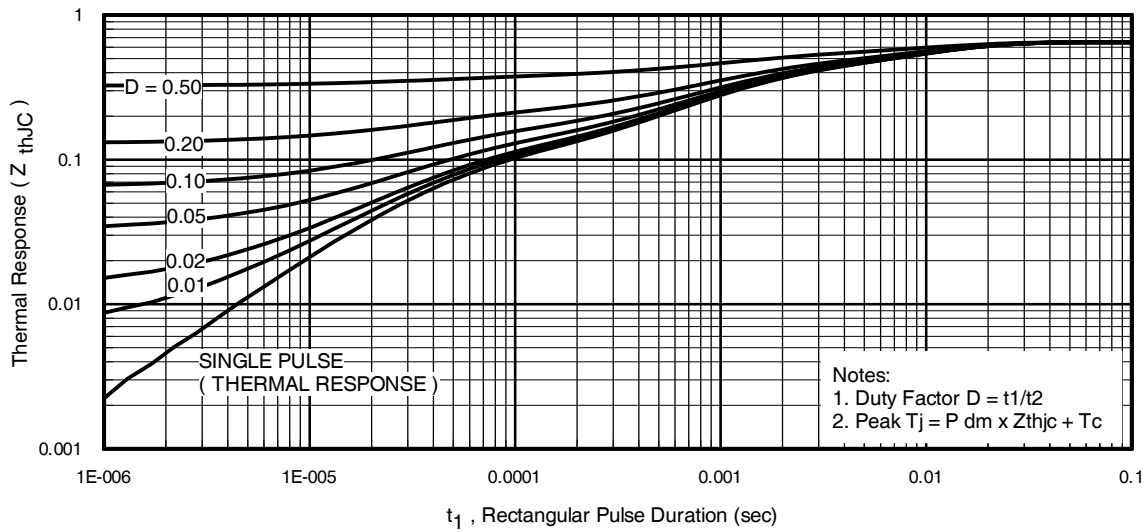
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

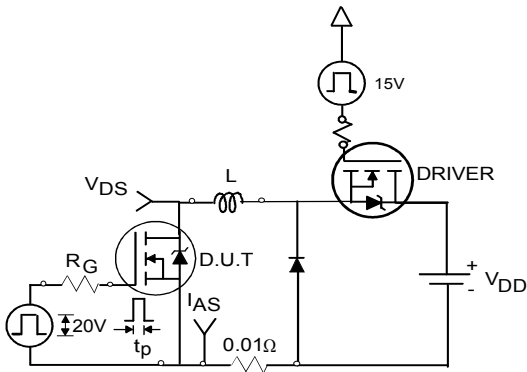
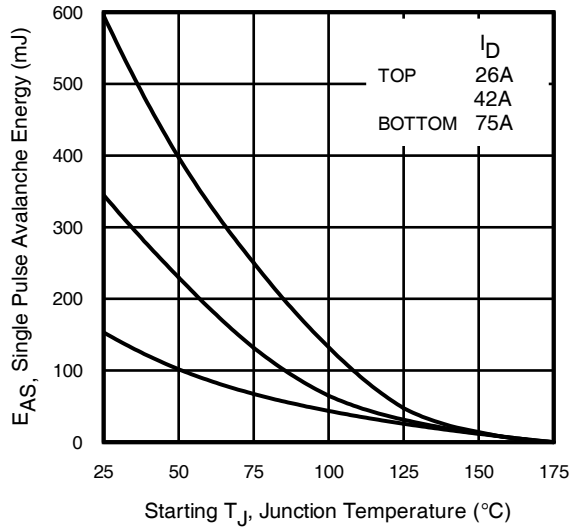
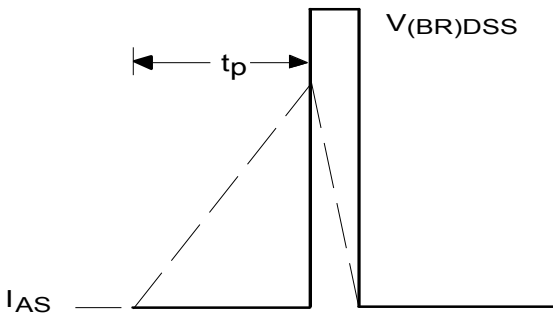
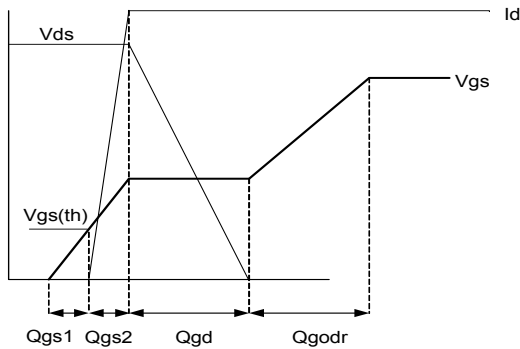
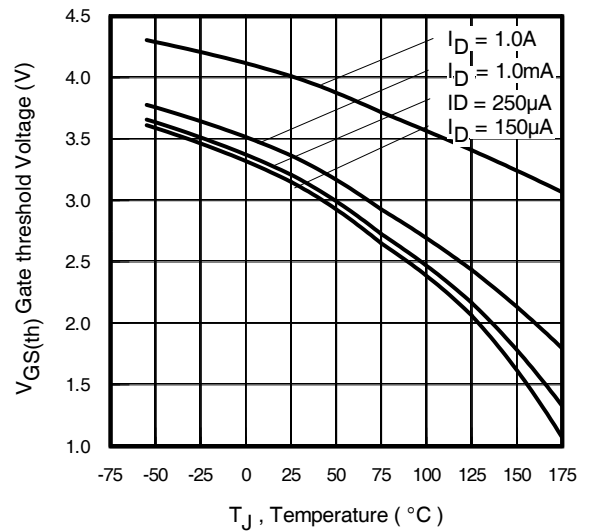
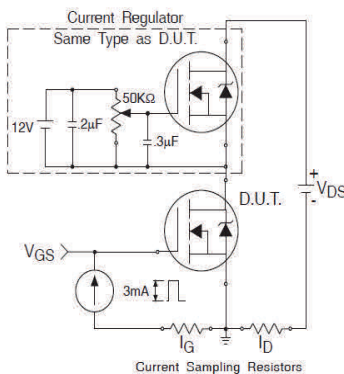


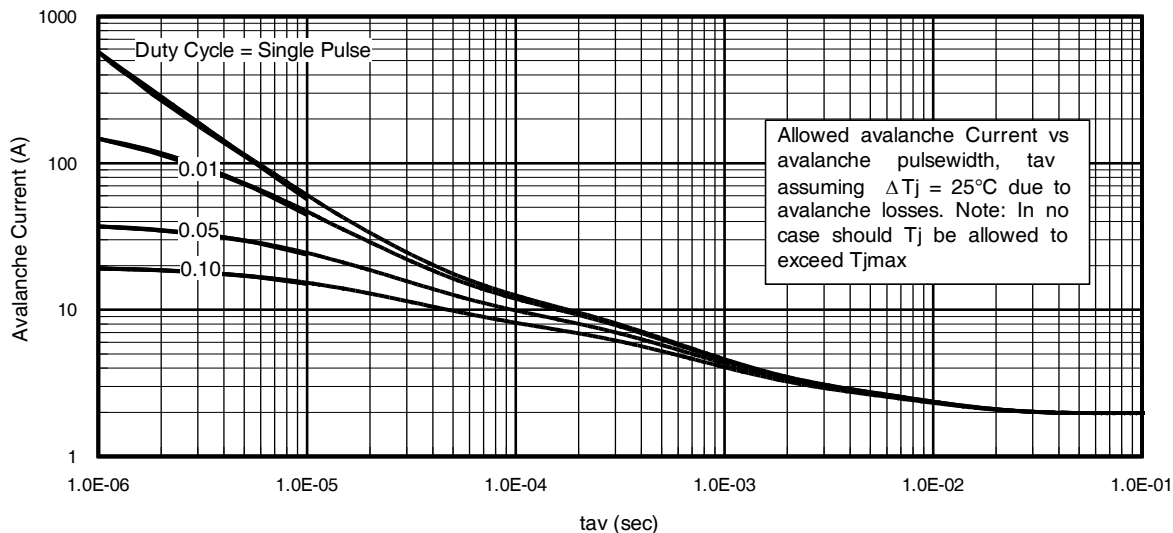
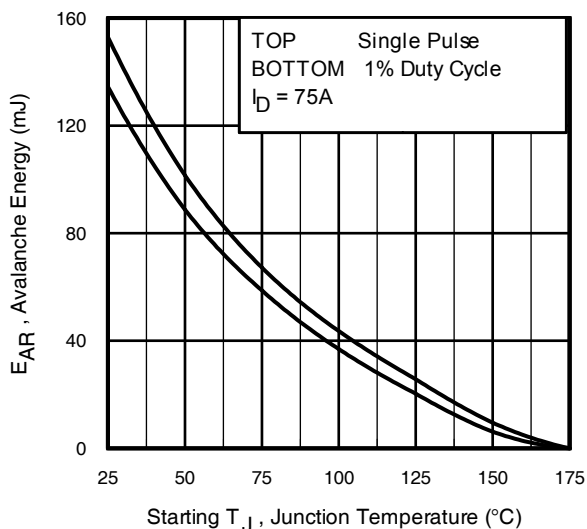
**Fig 7.** Typical Source-to-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area


**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Normalized On-Resistance vs. Temperature

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12c. Maximum Avalanche Energy vs. Drain Current**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 13a. Gate Charge Waveform**

**Fig 14. Threshold Voltage vs. Temperature**

**Fig 13b. Gate Charge Test Circuit**


**Fig 15.** Typical Avalanche Current vs. Pulse width

**Fig 16.** Maximum Avalanche Energy vs. Temperature

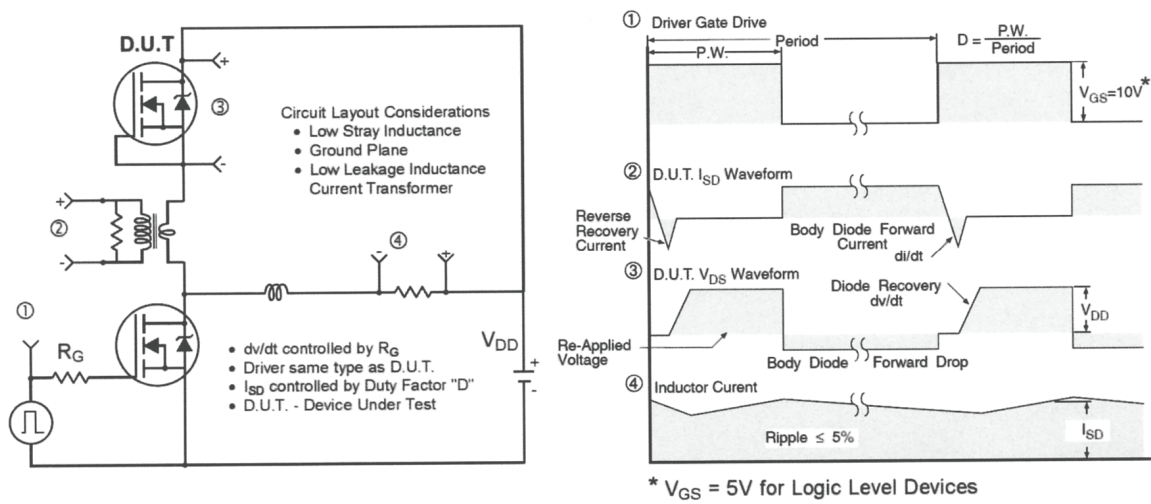
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

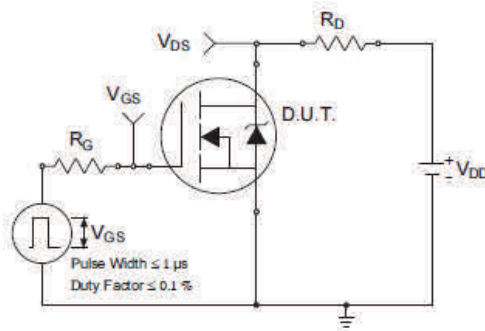
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{thJC} ]$$

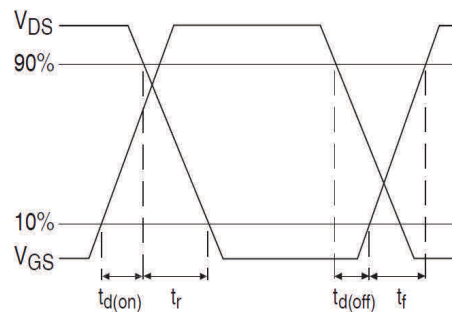
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs



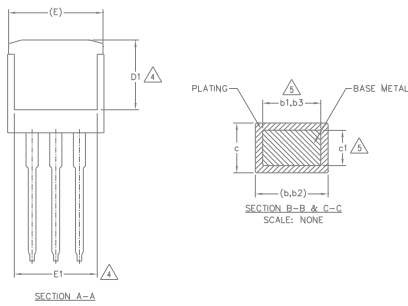
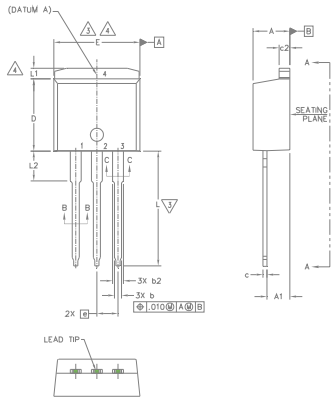
**Fig 18a.** Switching Time Test Circuit



**Fig 18b.** Switching Time Waveforms



## TO-262 Package Outline (Dimensions are shown in millimeters (inches))



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

### LEAD ASSIGNMENTS

#### IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

#### HEXFET

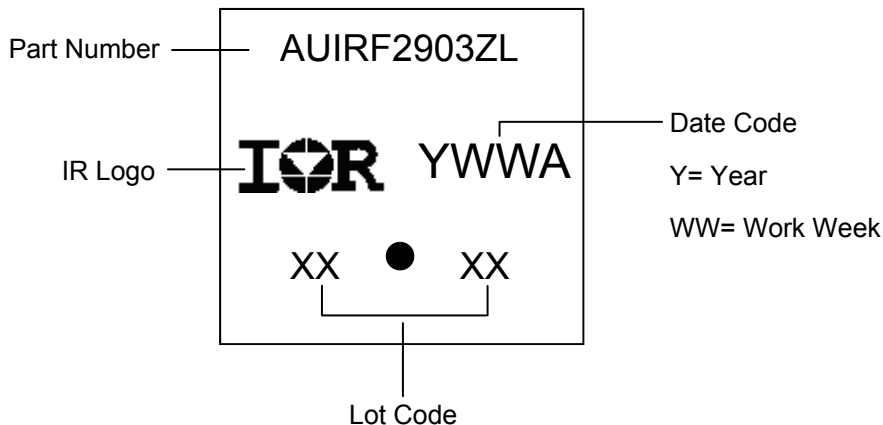
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

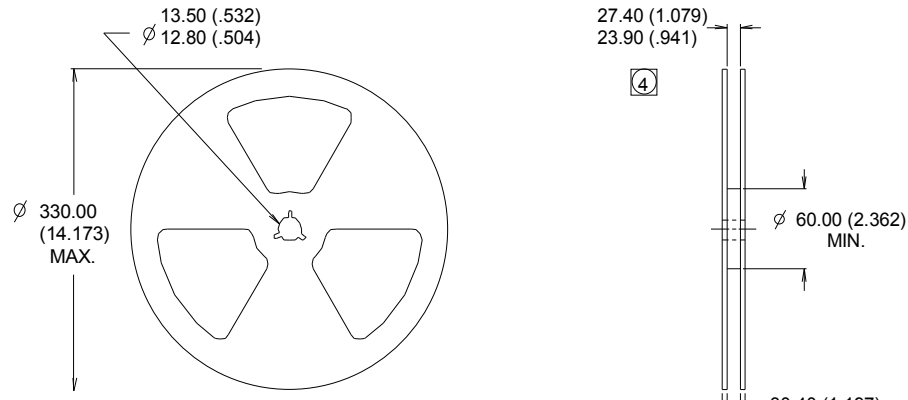
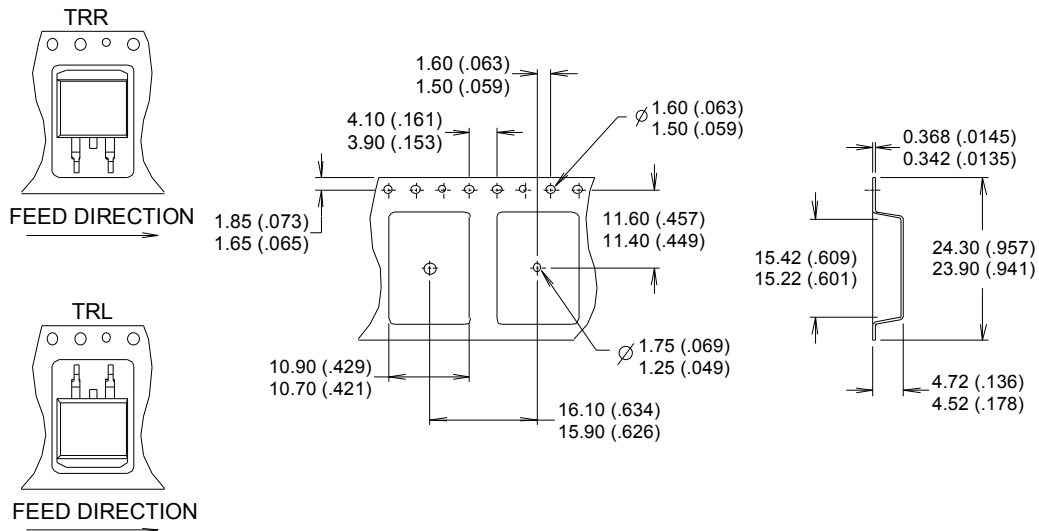
#### DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

## TO-262 Part Marking Information



**D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))**


- NOTES :
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		TO-262	MSL1
		D <sup>2</sup> -Pak	
<b>ESD</b>	Machine Model	Class M4(+/- 800V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H2(+/- 4000V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5(+/- 2000V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
9/30/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>
8/22/2017	<ul style="list-style-type: none"> <li>Corrected part marking on pages 9,10.</li> </ul>

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