MOSFET

OptiMOS^{TM} Power-Transistor, 60 V

Features

- Ideal for high-frequency switching
- Optimized for chargers
- 100% avalanche tested
- Superior thermal resistance
- N-channel, Logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
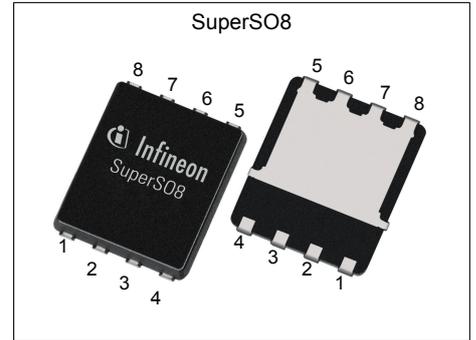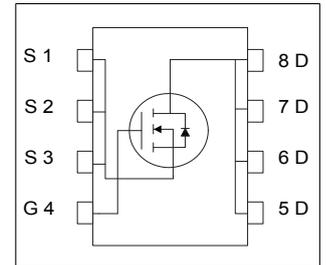- Qualified for Standard Grade applications

SuperSO8

Table 1   Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	2.7	mΩ
I_D	100	A
Q_{oss}	43	nC
$Q_G(0..4.5V)$	24	nC

S 1		8 D
S 2		7 D
S 3		6 D
G 4		5 D

Type / Ordering Code	Package	Marking	Related Links
BSC0702LS	PG-TDSON-8	0702LS	-

Table of Contents

1   Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2   Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	100 84 23	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA} =50K/W[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	400	A	T_C=25 °C
Avalanche energy, single pulse[3]	E_{AS}	-	-	100	mJ	I_D=50 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	83 2.5	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2   Thermal characteristics

Table 3   Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.9	1.5	K/W	-
Device on PCB, 6 cm² cooling area[1]	R_{thJA}	-	-	50	K/W	-

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information

3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	$V_{DS}=V_{GS}$, I_D=49 µA
Zero gate voltage drain current	I_{DSS}	- -	0.5 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.3 3.1	2.7 3.9	mΩ	V_{GS}=10 V, I_D=50 A V_{GS}=4.5 V, I_D=25 A
Gate resistance[1]	R_G	-	1.3	1.95	Ω	-
Transconductance	g_{fs}	60	120	-	S	$|V_{DS}|$>2$|I_D|R_{DS(on)max}$, I_D=50 A

Table 5 Dynamic characteristics[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3300	4400	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}	-	670	890	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	33	58	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	7.7	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	4.8	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	25	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	5.4	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=50 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	10	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	6	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1]	Q_{gd}	-	8	11	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	12	-	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total[1]	Q_g	-	24	30	nC	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	V_{DD}=30 V, I_D=50 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	43	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1]	Q_{oss}	-	43	58	nC	V_{DD}=30 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test
[2] See ″Gate charge waveforms″ for parameter definition

Table 7   Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	69	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	276	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.8	1.2	V	V_{GS}=0 V, I_F=50 A, T_j=25 °C
Reverse recovery time[1]	t_{rr}	-	40	80	ns	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge[1]	Q_{rr}	-	36	72	nC	V_R=30 V, I_F=50 A, di_F/dt=100 A/µs

[1] Defined by design. Not subject to production test

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4 Electrical characteristics diagrams

Diagram 1: Power dissipation

P_{tot} [W] vs T_C [°C]

P_{tot}=f(T_C)

Diagram 2: Drain current

I_D [A] vs T_C [°C]

I_D=f(T_C); $V_{GS} \geq$ 10 V

Diagram 3: Safe operating area

I_D [A] vs V_{DS} [V]

1 µs
10 µs
100 µs
1 ms
10 ms
DC

I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance

Z_{thJC} [K/W] vs t_p [s]

0.5
0.2
0.1
0.05
0.02
0.01
single pulse

Z_{thJC}=f(t_p); parameter: D=t_p/T
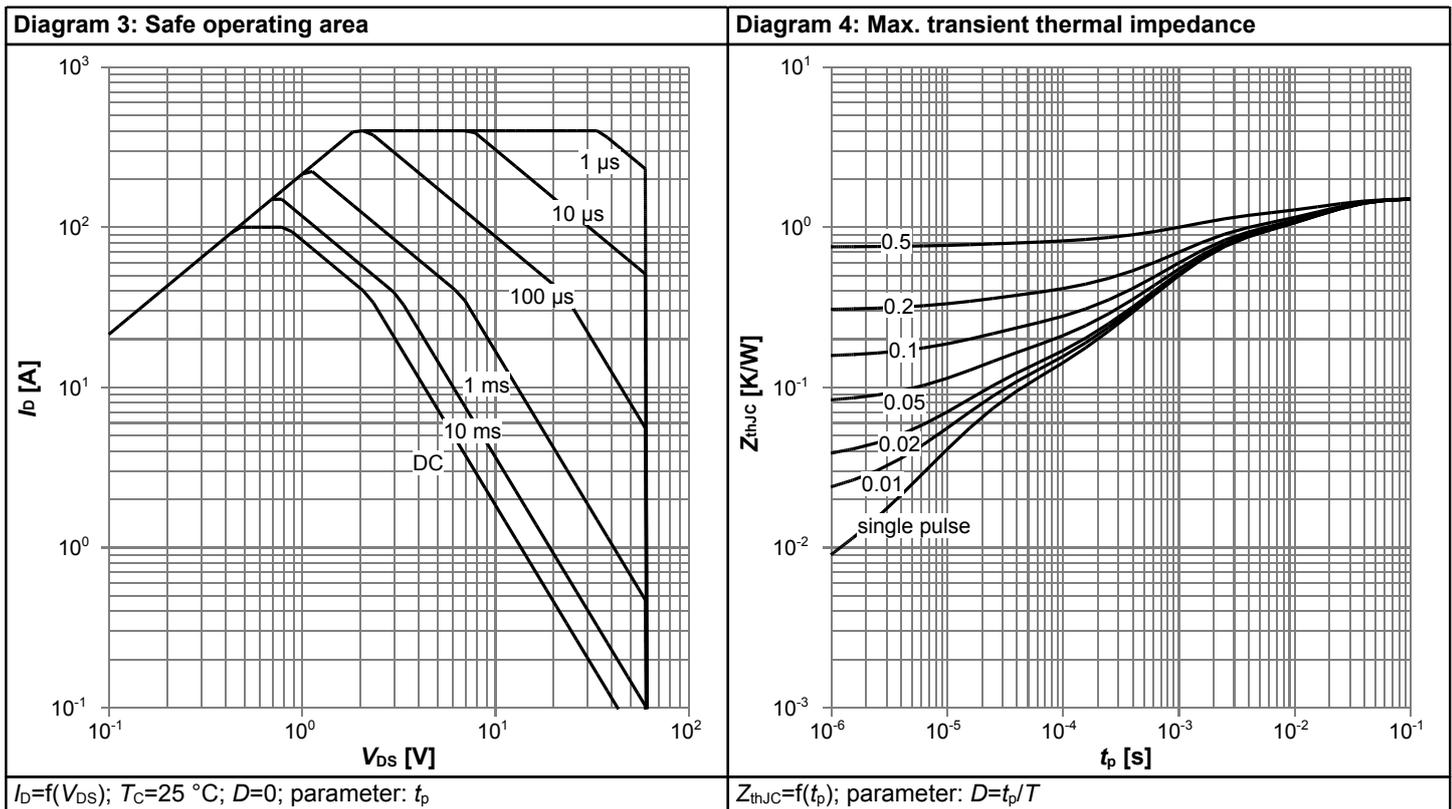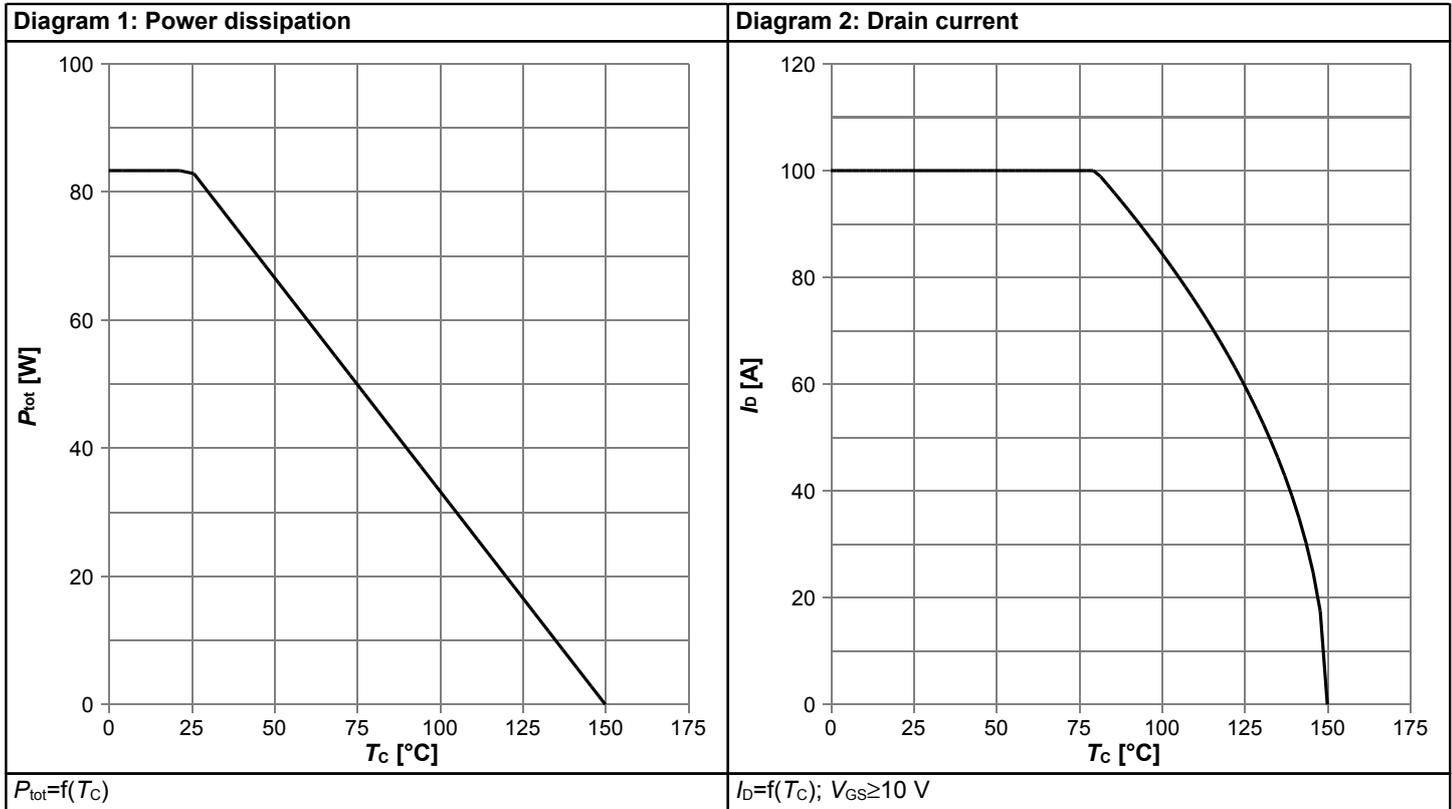
Diagram 5: Typ. output characteristics
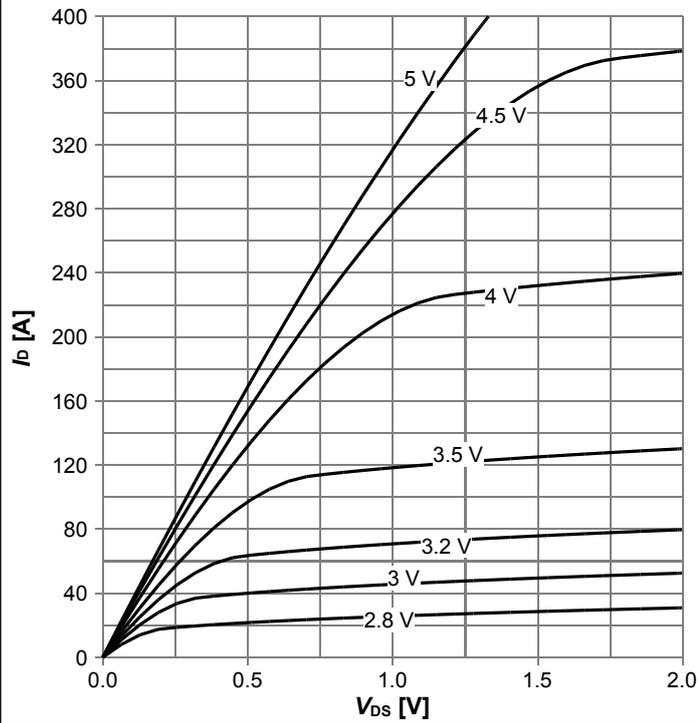
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}
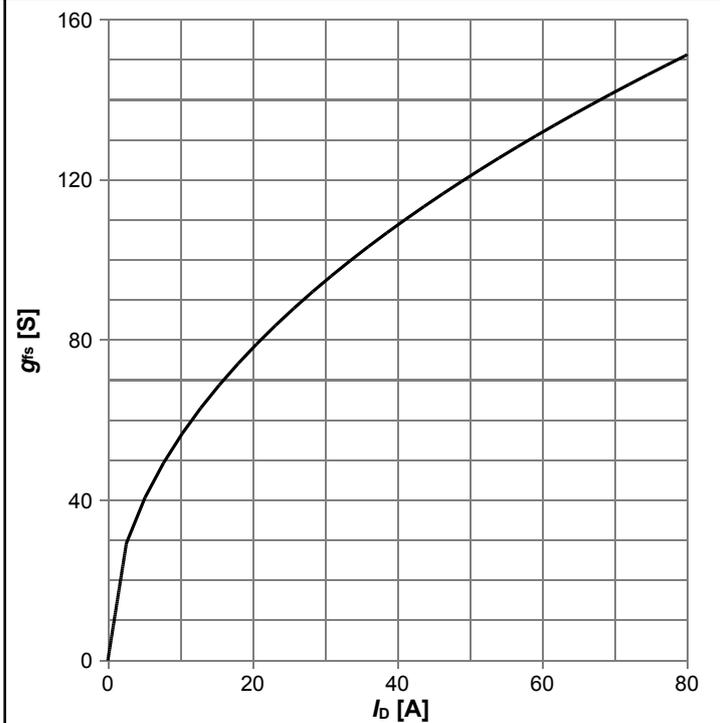
Diagram 6: Typ. drain-source on resistance
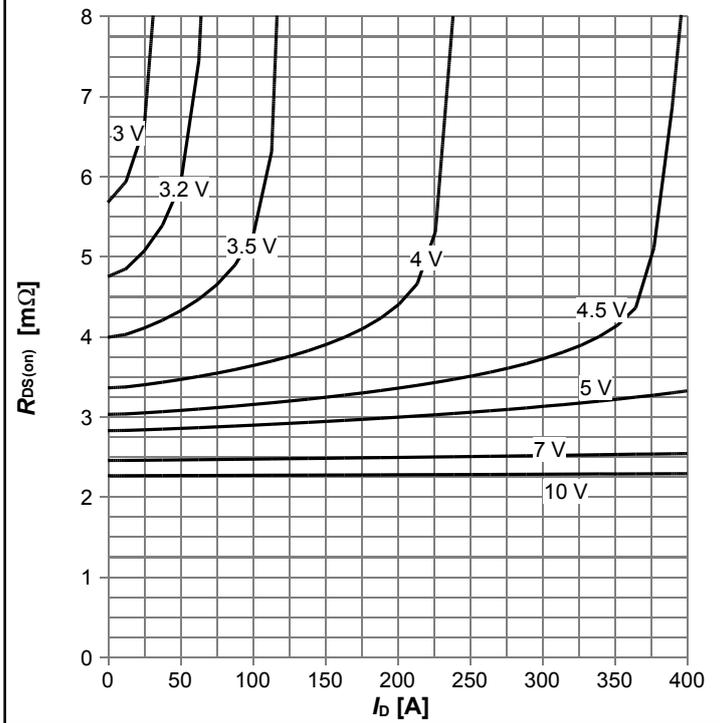
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}
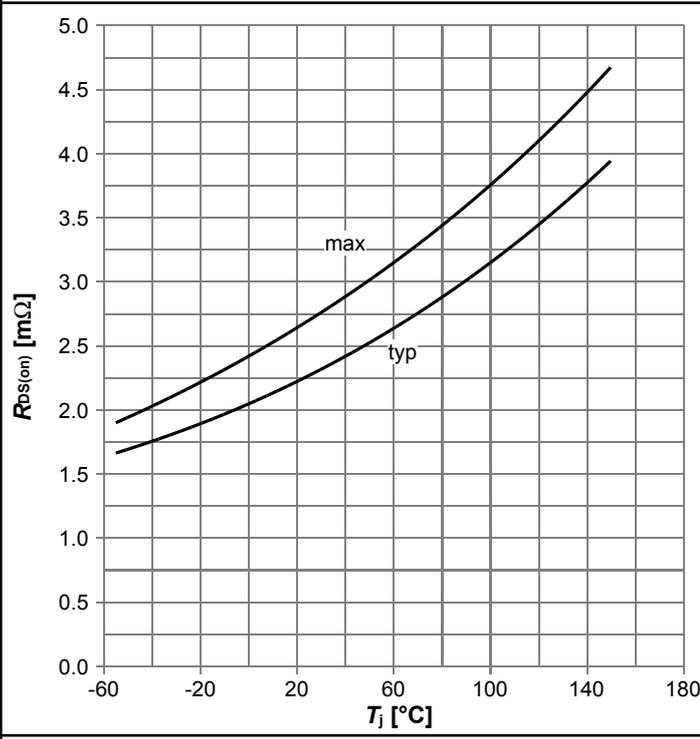
Diagram 7: Typ. transfer characteristics
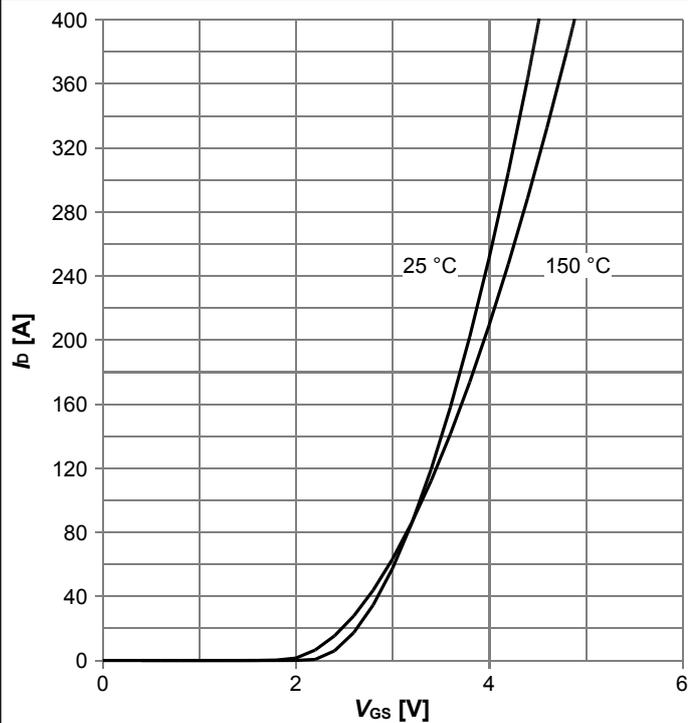
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j
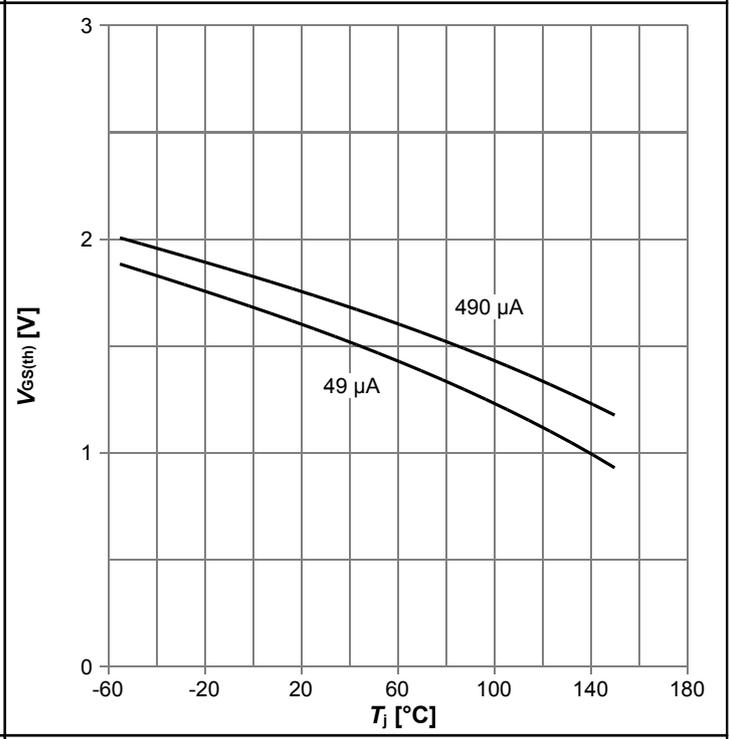
Diagram 8: Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C

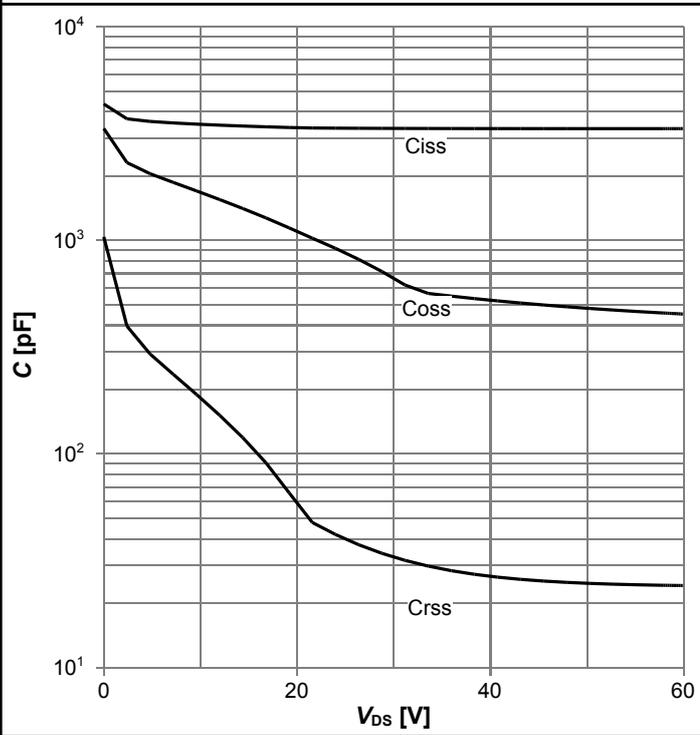## Diagram 9: Drain-source on-state resistance

$R_{DS(on)}=f(T_j)$; I_D=50 A; V_{GS}=10 V
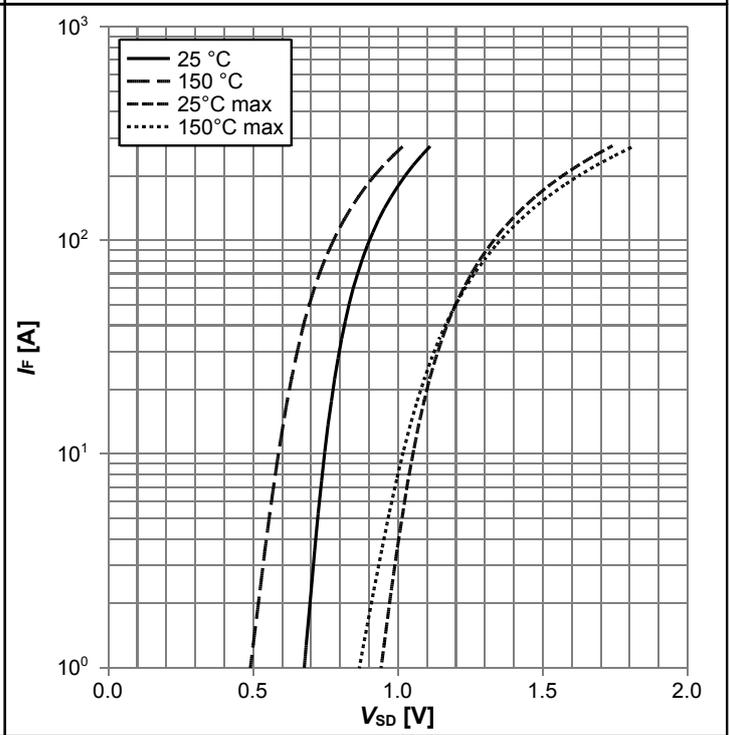
Diagram 10: Typ. gate threshold voltage

490 µA

49 µA

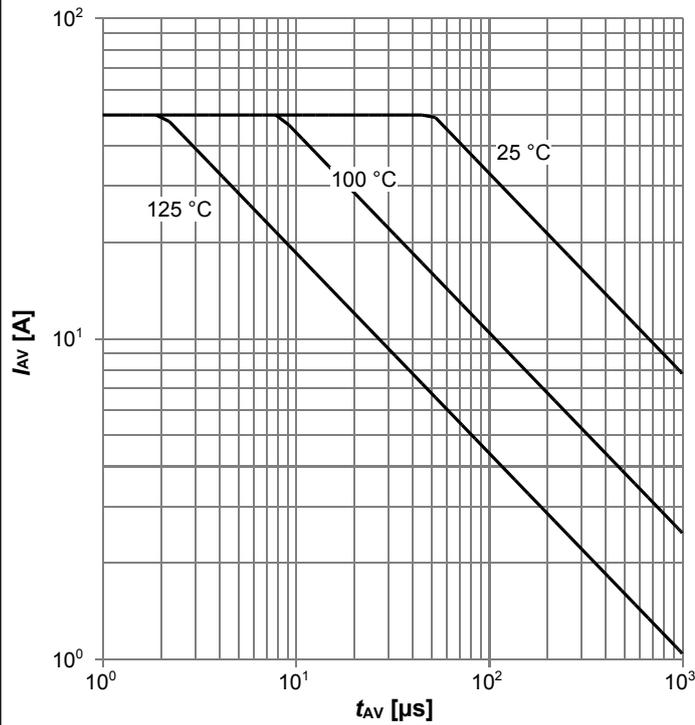$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances

Ciss

Coss

Crss

$C=f(V_{DS})$; V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode

- 25 °C
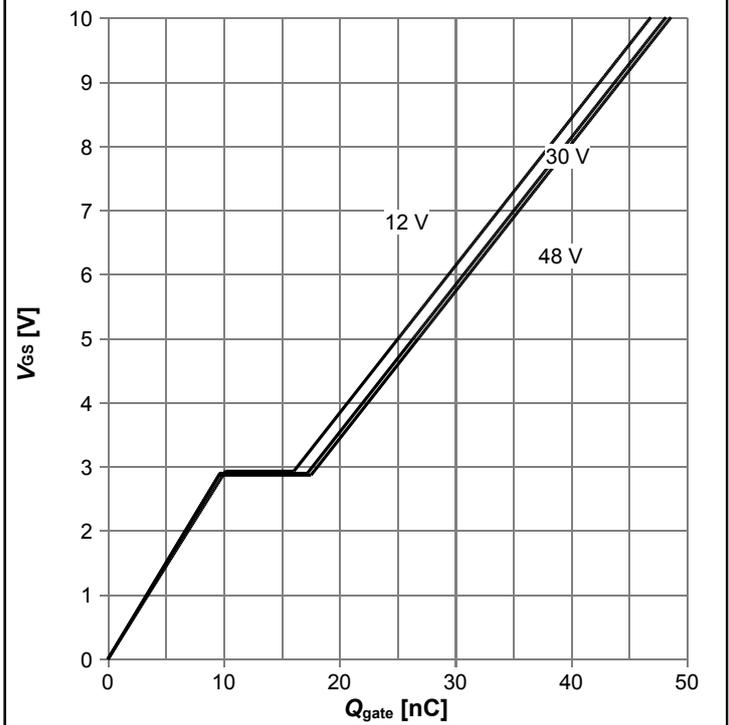- 150 °C
- 25°C max
- 150°C max

$I_F=f(V_{SD})$; parameter: T_j
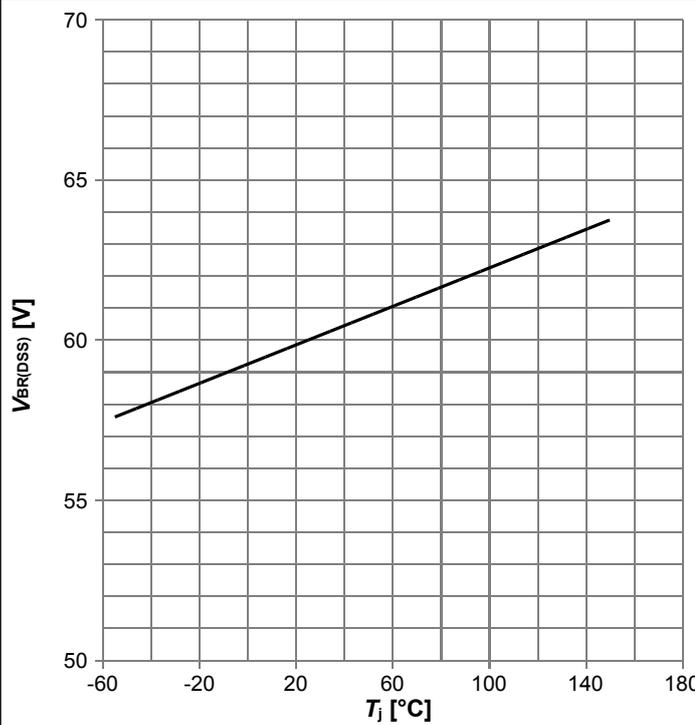
Diagram 13: Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$
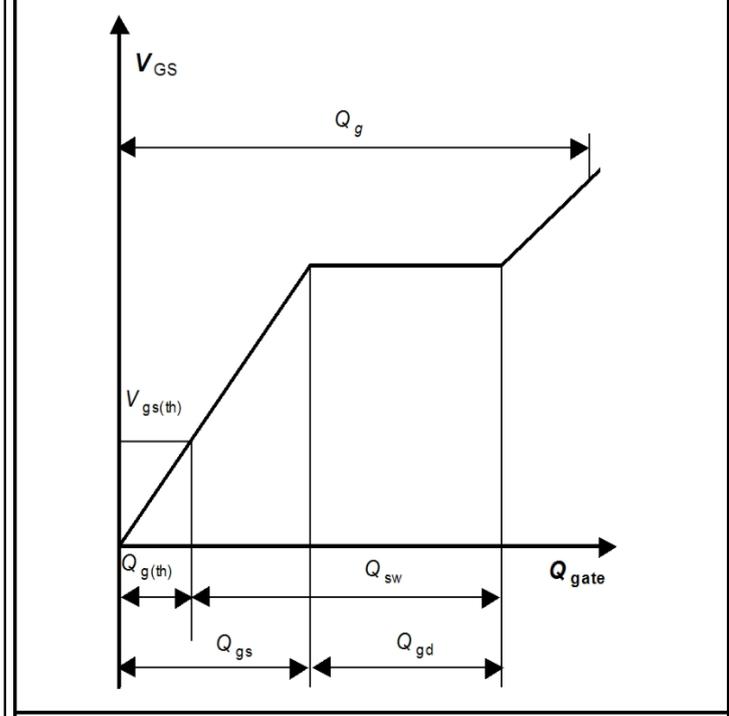
Diagram 14: Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=50 A pulsed; parameter: V_{DD}

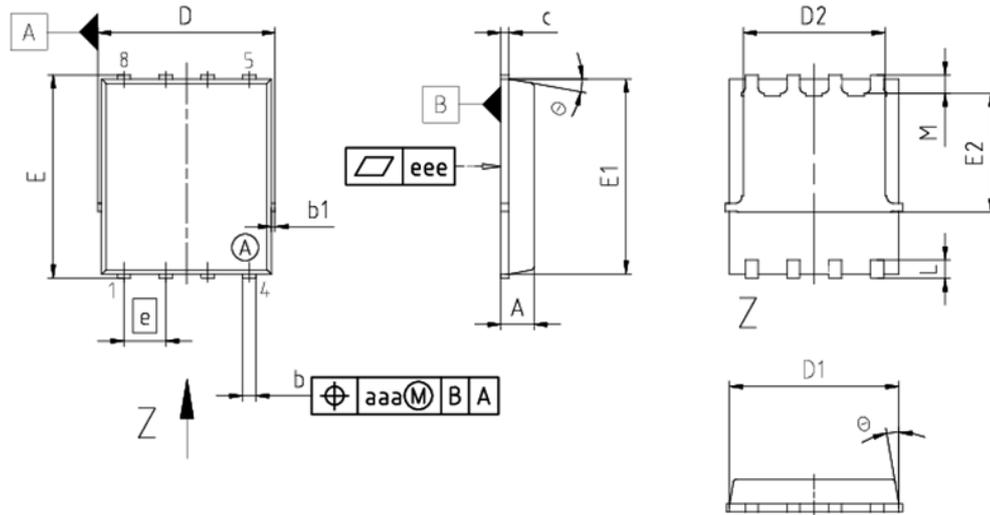**Diagram 15: Drain-source breakdown voltage**

$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms

5 Package Outlines

DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
b	0.31	0.54
b1	0.02	0.22
c	0.15	0.35
D	5.15	5.49
D1	4.95	5.35
D2	3.70	4.40
E	5.95	6.35
E1	5.70	6.10
E2	3.40	3.80
e	1.27	
N	8	
L	0.45	0.71
M	0.45	0.75
Θ	8.5°	12°
aaa	0.25	
eee	0.08	

DOCUMENT NO.
Z8B00003332

SCALE

EUROPEAN PROJECTION

ISSUE DATE
10-04-2013

REVISION
04

Figure 1   Outline PG-TDSON-8, dimensions in mm
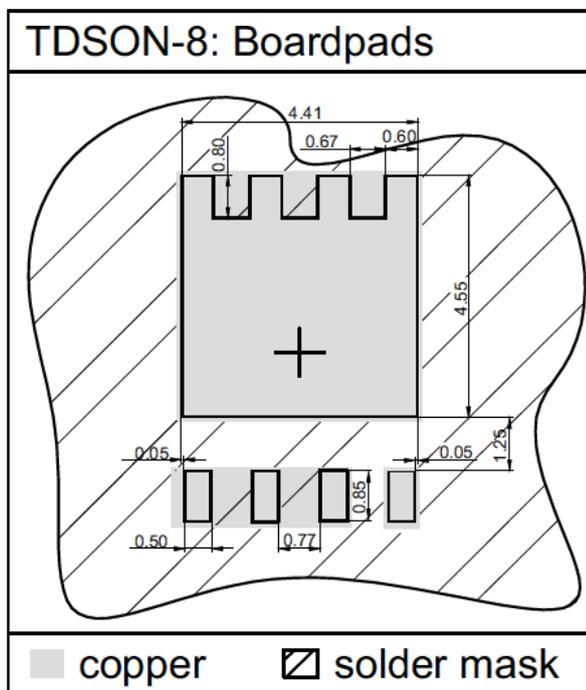
Figure 2   Outline Footprint (TDSON-8)

Revision History

BSC0702LS

Revision: 2016-10-25, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-06-09	Release of final version
2.1	2016-06-13	Insert Rds(on) max at Vgs 4.5
2.2	2016-06-21	Delete heading on first page
2.3	2016-10-25	Update " Features "

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