



BUK7M6R7-40H

N-channel 40 V, 6.7 mΩ standard level MOSFET in LPAK33

5 February 2019

Product data sheet

1. General description

Automotive qualified standard level N-channel MOSFET in an LPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
 - Low power losses, high power density
- LPAK copper clip package technology:
 - High robustness and reliability
 - Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Medium/Low power motor drive
- DC-DC systems
- LED lighting

4. Quick reference data

Table 1. Quick reference data

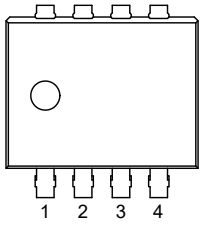
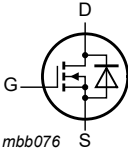
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	50	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	65	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		4	5.7	6.7	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 13 ; Fig. 14		-	3.2	6.4	nC
Source-drain diode							
Q_r	recovered charge	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$		-	17	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S	softness factor	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 17	-	0.62	-	

[1] 50A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK33 (SOT1210)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7M6R7-40H	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7M6R7-40H	76H740

8. Limiting values

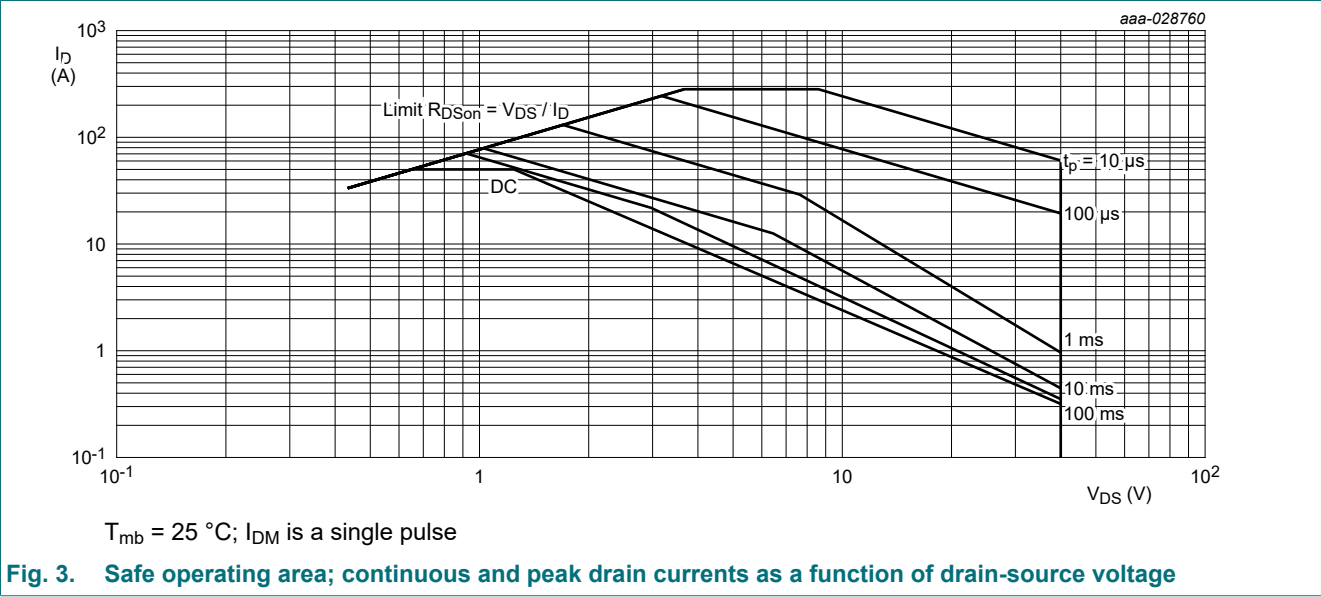
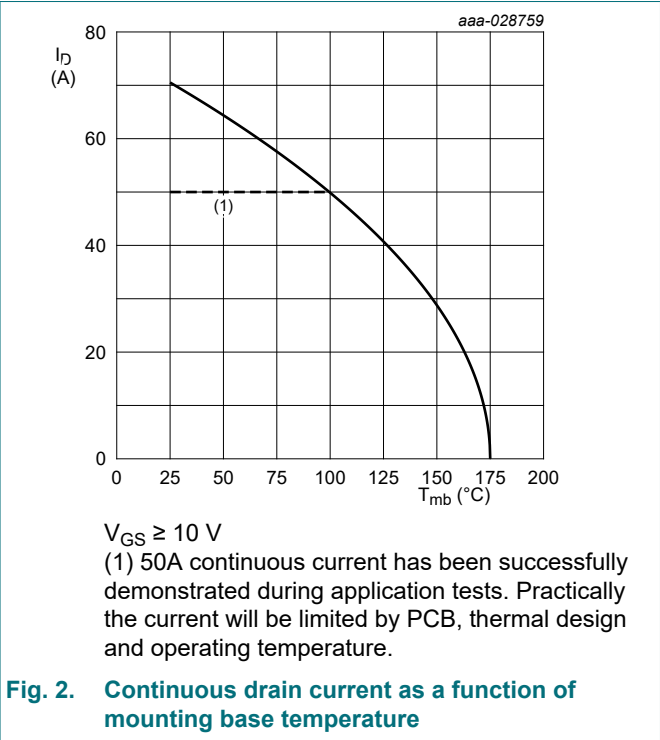
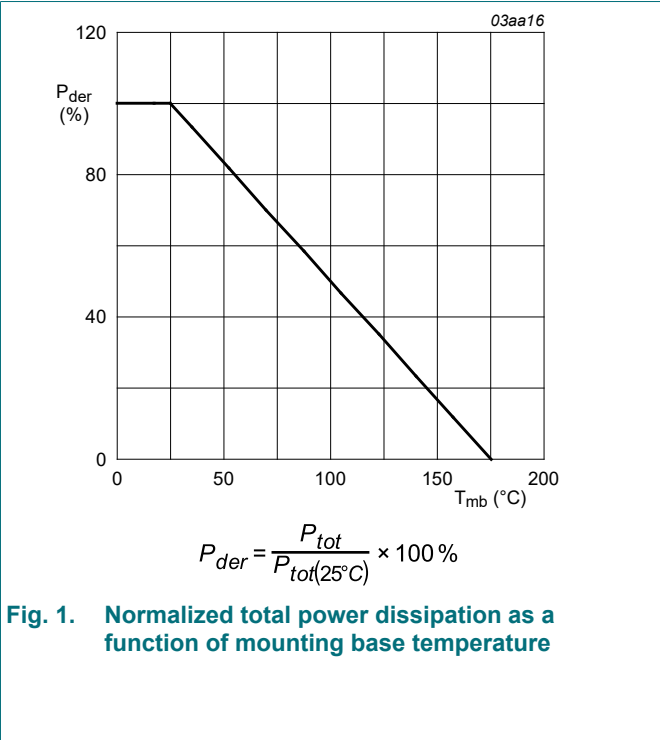
Table 5. Limiting values

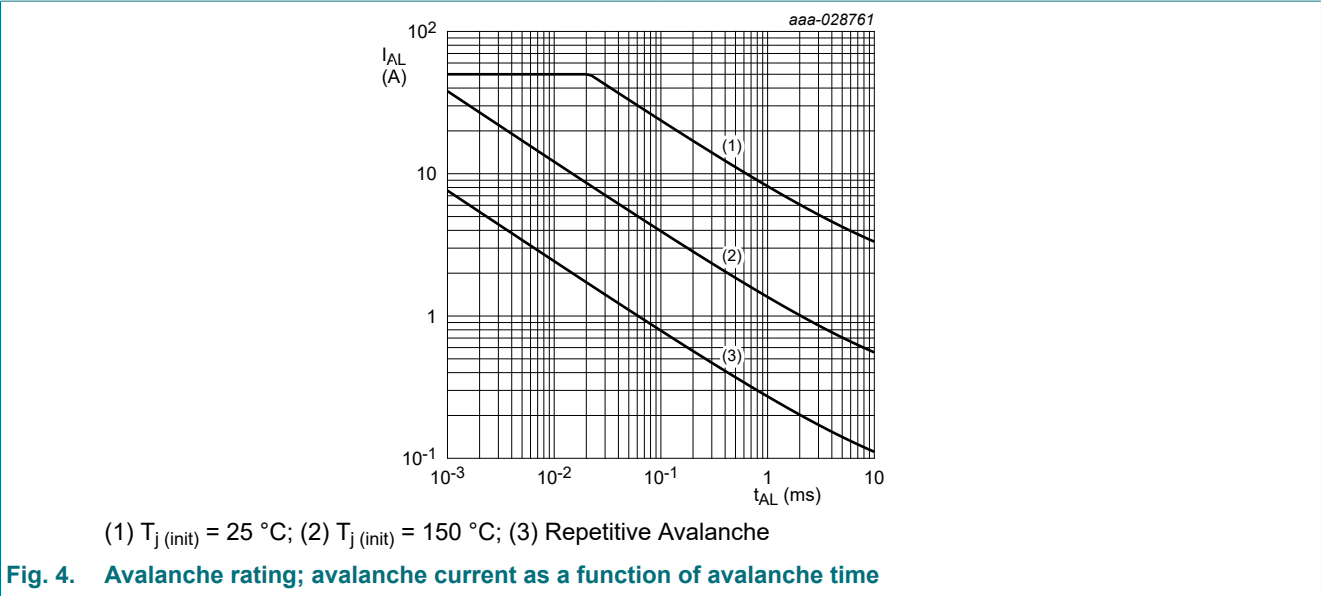
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	40	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ }^\circ\text{C}$	-10	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	65	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	[1]	50	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2	-	50	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3	-	282	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$
Source-drain diode					

Symbol	Parameter	Conditions		Min	Max	Unit
I _S	source current	T _{mb} = 25 °C		-	50	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	282	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 50 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[2] [3]	-	28	mJ

- [1] 50A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.

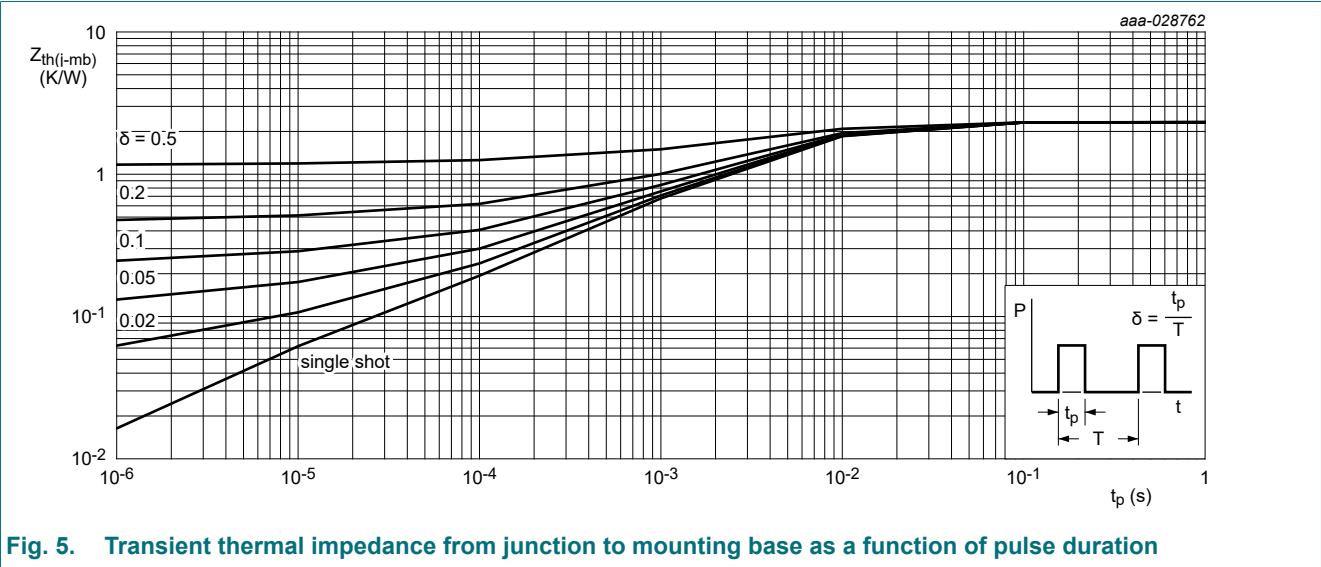




9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.09	2.32	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	40	43	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -40\text{ °C}$	-	40.5	-	V

N-channel 40 V, 6.7 mΩ standard level MOSFET in LPAK33

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = 25 ^\circ C$; Fig. 9 ; Fig. 10		2.4	3	3.6	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = -55 ^\circ C$; Fig. 10		-	-	4.3	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = 175 ^\circ C$; Fig. 10		1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$		-	0.02	1	μA
		$V_{DS} = 16 V$; $V_{GS} = 0 V$; $T_j = 125 ^\circ C$		-	0.51	10	μA
		$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_j = 175 ^\circ C$		-	25	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	2	100	nA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 25 ^\circ C$; Fig. 11		4	5.7	6.7	m Ω
		$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 105 ^\circ C$; Fig. 12		5.4	8.1	10	m Ω
		$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 125 ^\circ C$; Fig. 12		6	8.8	10.8	m Ω
		$V_{GS} = 10 V$; $I_D = 20 A$; $T_j = 175 ^\circ C$; Fig. 12		7.3	10.6	13	m Ω
R_G	gate resistance	$f = 1 MHz$; $T_j = 25 ^\circ C$		0.3	0.8	1.9	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 20 A$; $V_{DS} = 32 V$; $V_{GS} = 10 V$; Fig. 13 ; Fig. 14		-	17	24	nC
Q_{GS}	gate-source charge			-	5.4	8	nC
Q_{GD}	gate-drain charge			-	3.2	6.4	nC
C_{iss}	input capacitance	$V_{DS} = 25 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$; Fig. 15		-	1161	1625	pF
C_{oss}	output capacitance			-	433	606	pF
C_{rss}	reverse transfer capacitance			-	55	121	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V$; $R_L = 1.5 \Omega$; $V_{GS} = 10 V$; $R_{G(ext)} = 5 \Omega$		-	5.8	-	ns
t_r	rise time			-	4.3	-	ns
$t_{d(off)}$	turn-off delay time			-	11	-	ns
t_f	fall time			-	4.5	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 20 A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$; Fig. 16		-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20 A$; $dI_S/dt = -100 A/\mu s$; $V_{GS} = 0 V$; $V_{DS} = 20 V$; Fig. 17		-	23	-	ns
Q_r	recovered charge	$I_S = 20 A$; $dI_S/dt = -100 A/\mu s$; $V_{GS} = 0 V$; $V_{DS} = 20 V$		-	17	-	nC
S	softness factor	$I_S = 20 A$; $dI_S/dt = -100 A/\mu s$; $V_{GS} = 0 V$; $V_{DS} = 20 V$; $T_j = 25 ^\circ C$; Fig. 17		-	0.62	-	
		$I_S = 20 A$; $dI_S/dt = -500 A/\mu s$; $V_{GS} = 0 V$; $V_{DS} = 20 V$; $T_j = 25 ^\circ C$; Fig. 17		-	0.46	-	

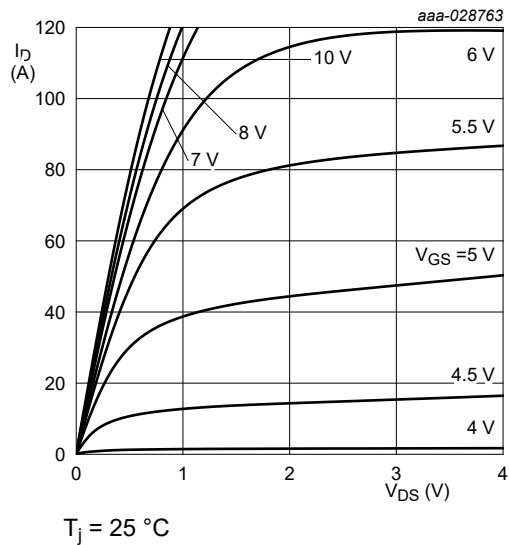


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

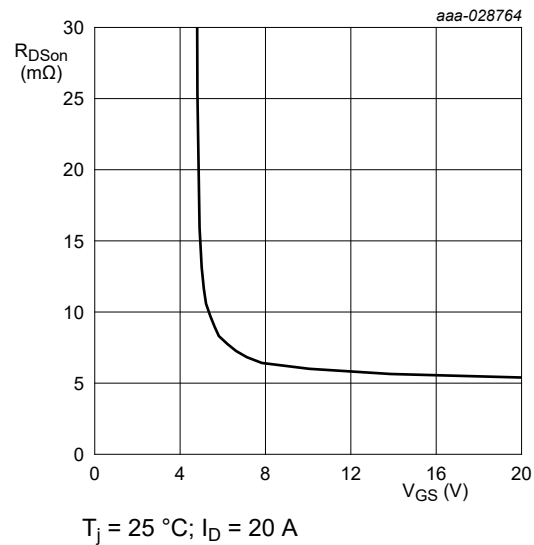


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

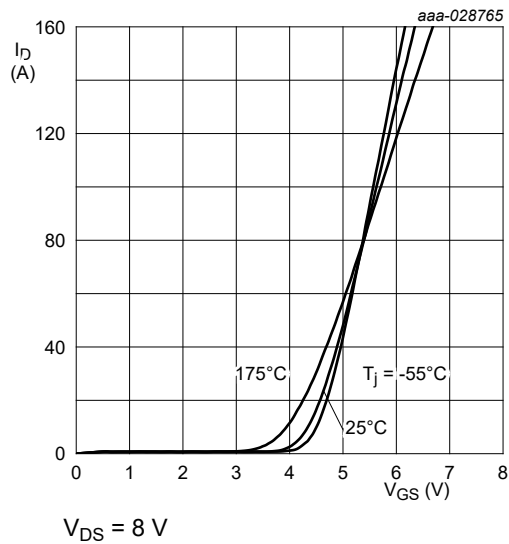


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

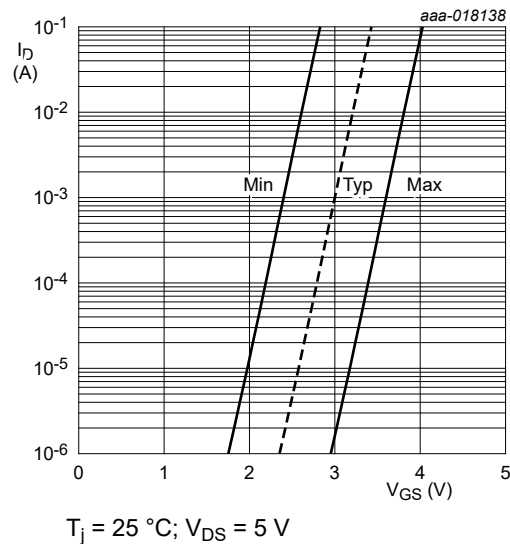


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

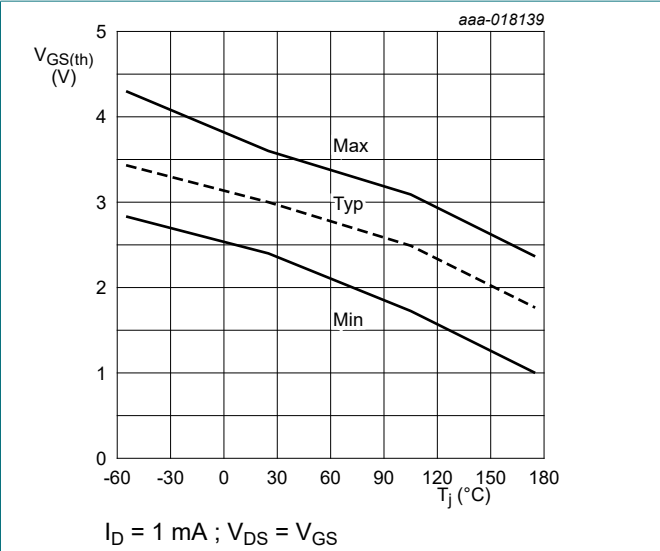


Fig. 10. Gate-source threshold voltage as a function of junction temperature

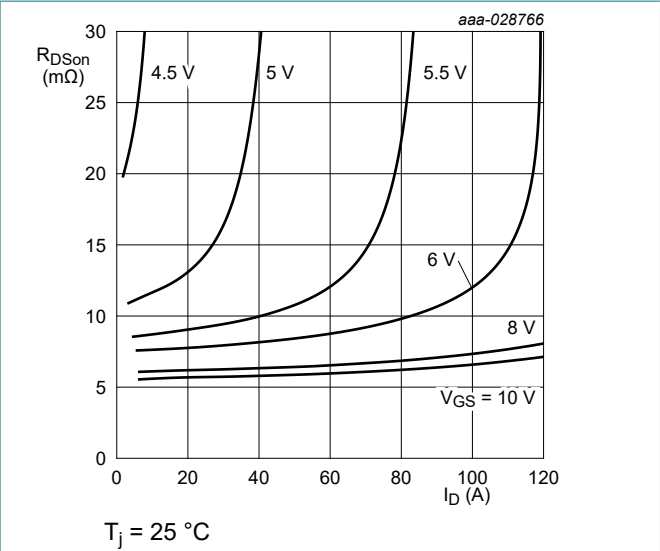


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

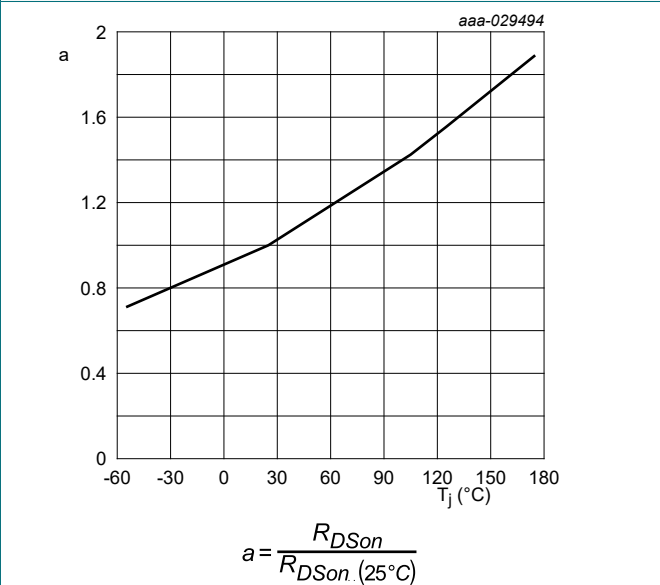


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

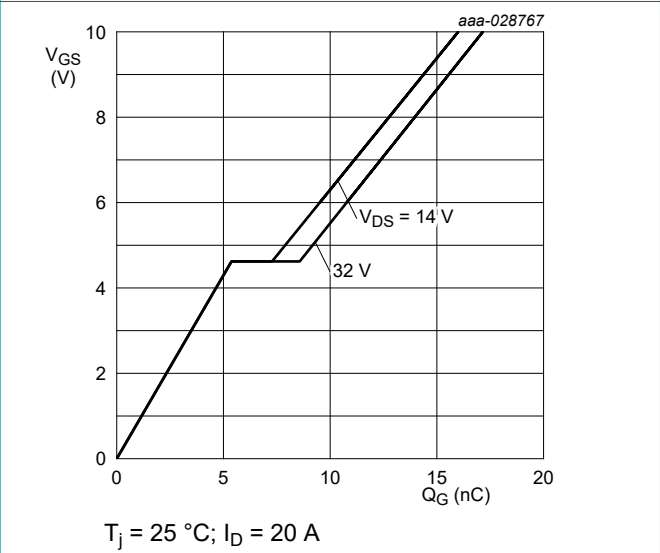


Fig. 13. Gate-source voltage as a function of gate charge; typical values

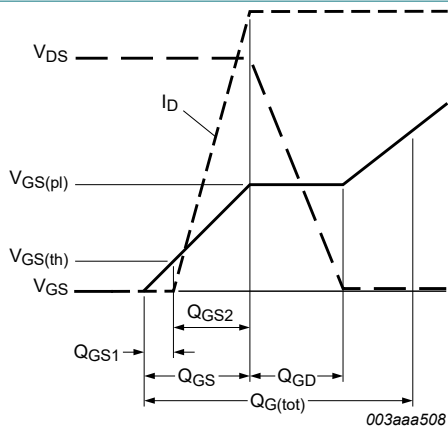
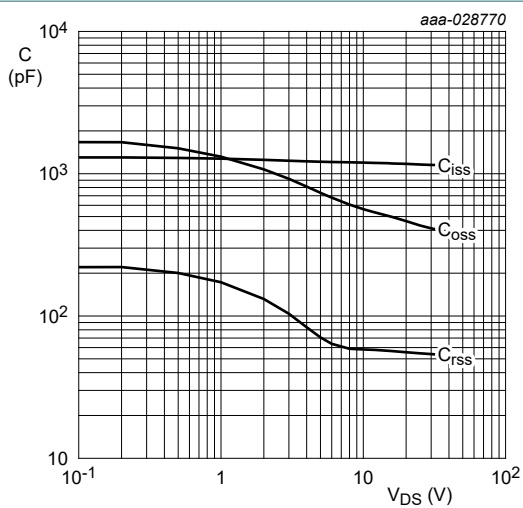
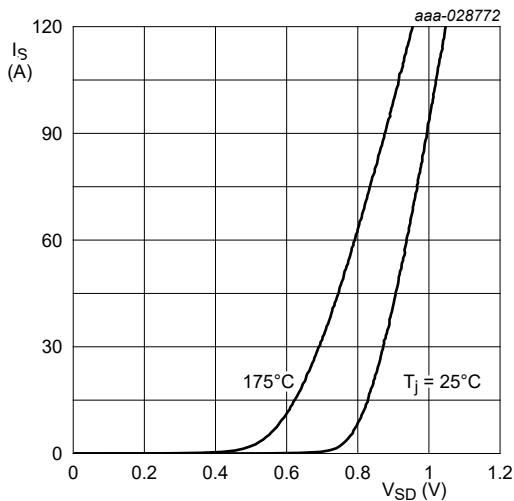


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

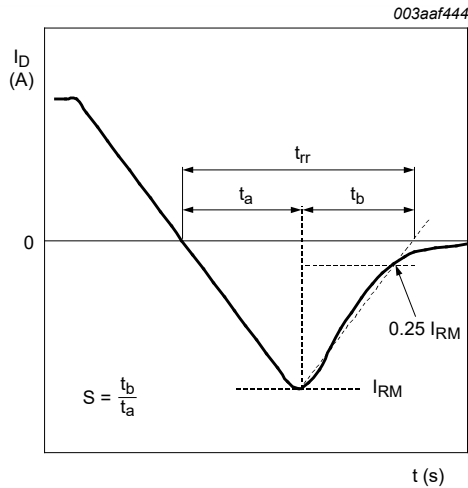


Fig. 17. Reverse recovery timing definition

11. Package outline

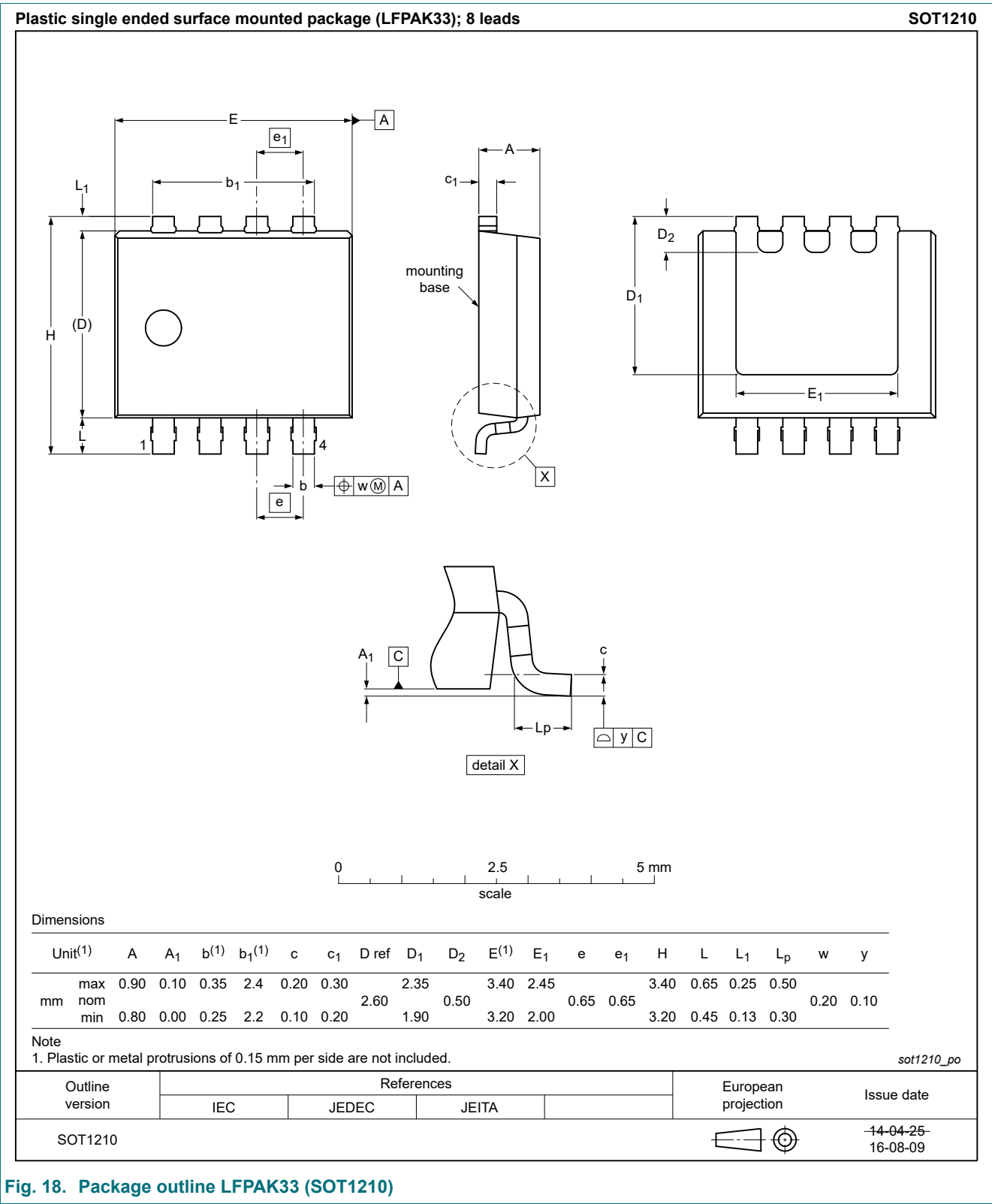


Fig. 18. Package outline LPAK33 (SOT1210)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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