



# BUK9M5R0-40H

N-channel 40 V, 5.0 mΩ logic level MOSFET in LFPAK33

13 March 2020

Product data sheet

## 1. General description

Automotive qualified logic level N-channel MOSFET in an LFPAK33 package using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
  - Low power losses, high power density
- LFPAK copper clip package technology:
  - High robustness and reliability
  - Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

## 3. Applications

- 12 V automotive systems
- Powertrain, chassis, body and infotainment applications
- Medium/Low power motor drive
- DC-DC systems
- LED lighting

## 4. Quick reference data

Table 1. Quick reference data

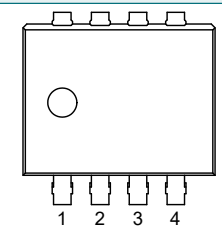
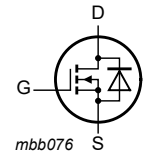
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	[1]	-	-	85	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>		-	-	83	W
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>		2.7	3.9	5	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$I_D = 20\text{ A}; V_{DS} = 20\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 13; Fig. 14</a>		-	2.9	5.9	nC
<b>Source-drain diode</b>							
$Q_r$	recovered charge	$I_S = 20\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}$		-	18	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S	softness factor	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 17</a>	-	0.66	-	

[1] 85A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFPAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

## 6. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BUK9M5R0-40H	LFPAK33	Plastic, single ended surface mounted package (LFPAK33); 8 leads; 0.65 mm pitch	SOT1210

## 7. Marking

**Table 4. Marking codes**

Type number	Marking code
BUK9M5R0-40H	95H040

## 8. Limiting values

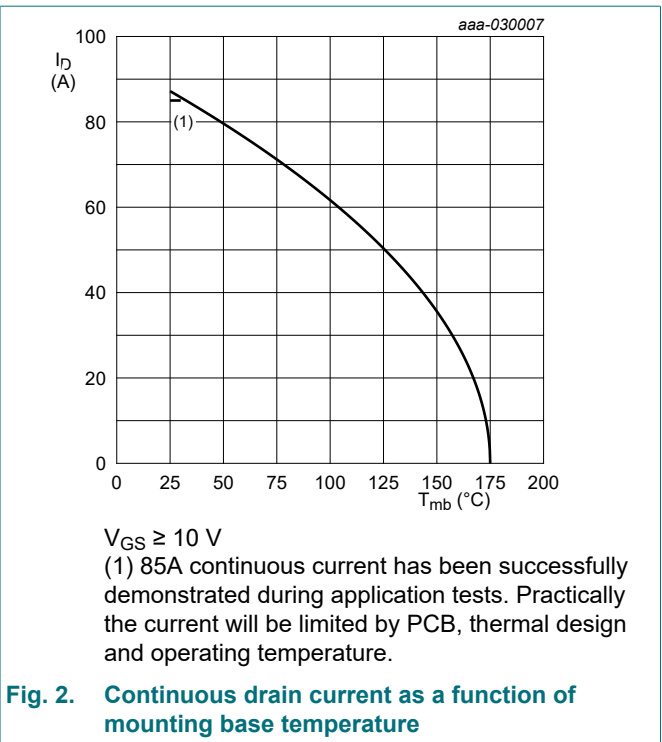
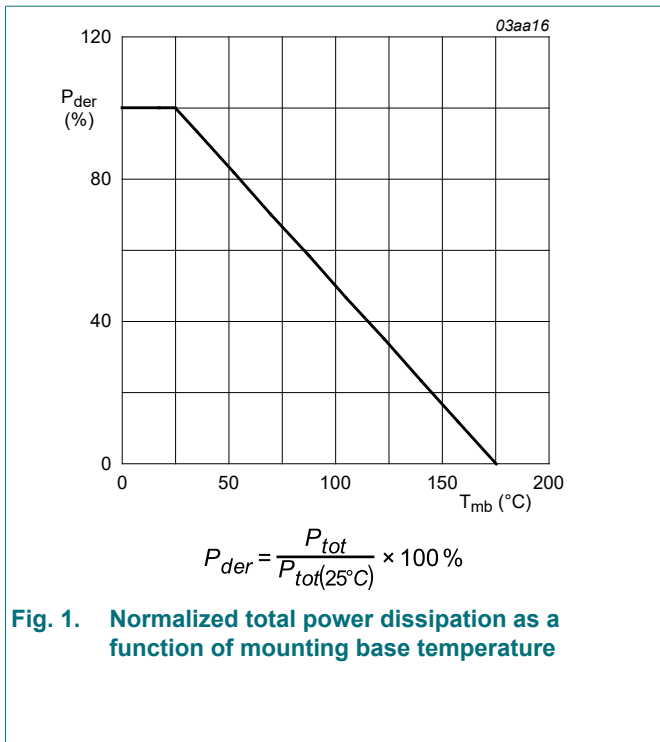
**Table 5. Limiting values**

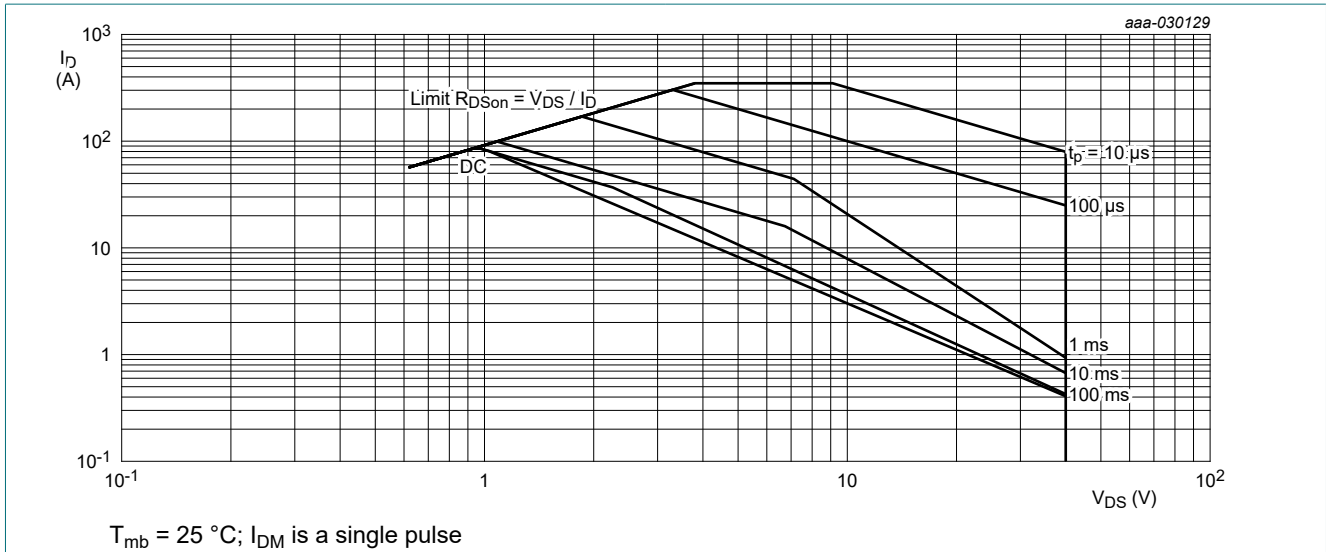
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	40	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ }^\circ\text{C}$	-10	16	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	83	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	[1]	85	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	61.7	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 3</a>	-	349	A
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$

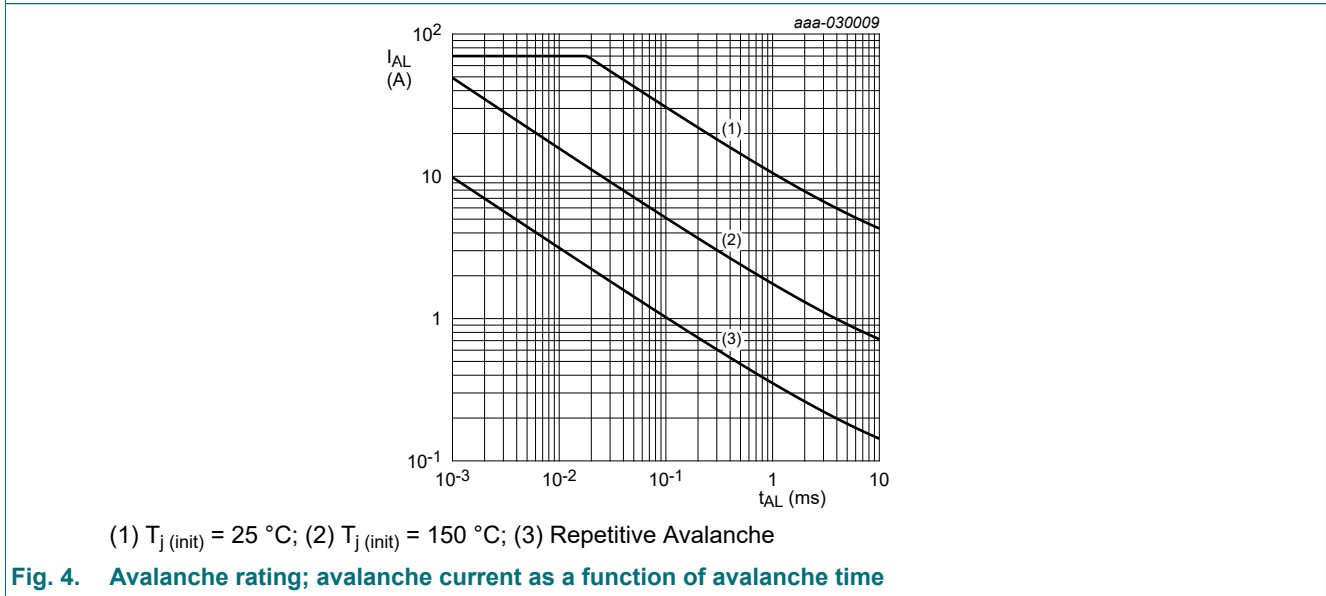
Symbol	Parameter	Conditions	Min	Max	Unit
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	85	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	349	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 70\text{ A}$ ; $V_{sup} \leq 40\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; unclamped; Fig. 4	[2] [3] [4]	33	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $R_{GS} = 50\text{ }\Omega$	[4]	70	A

- [1] 85A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test.





**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	1.61	1.81	K/W

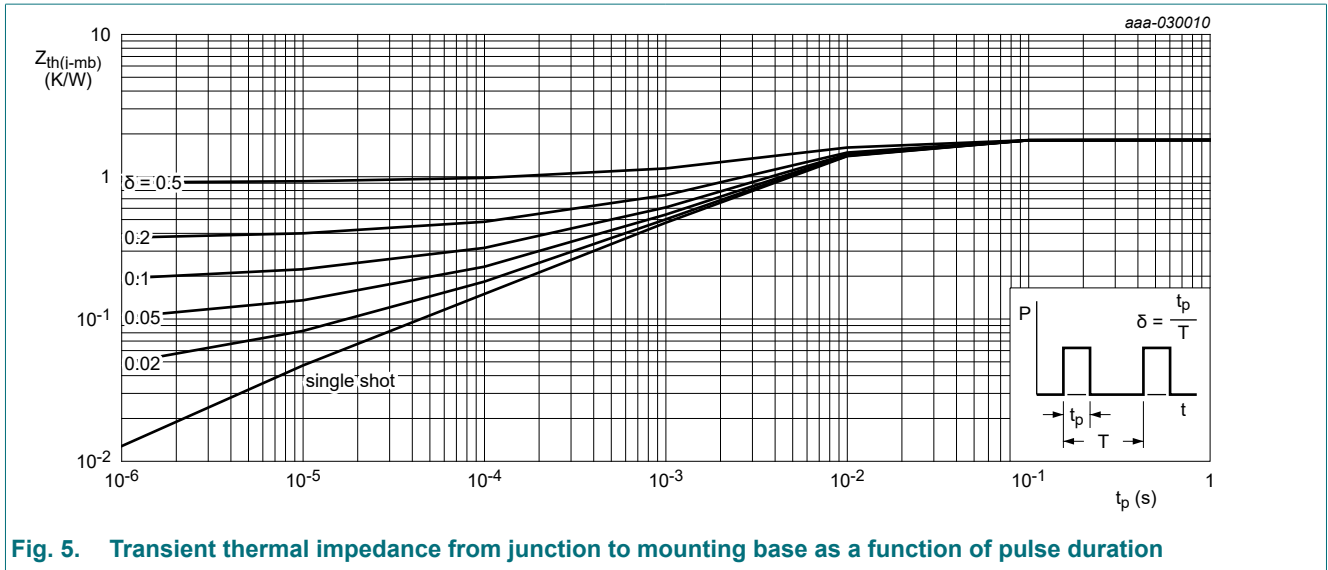


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

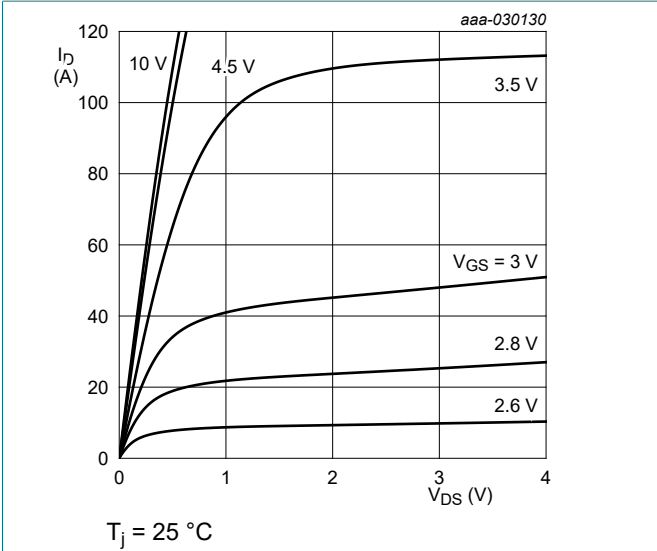
## 10. Characteristics

Table 7. Characteristics

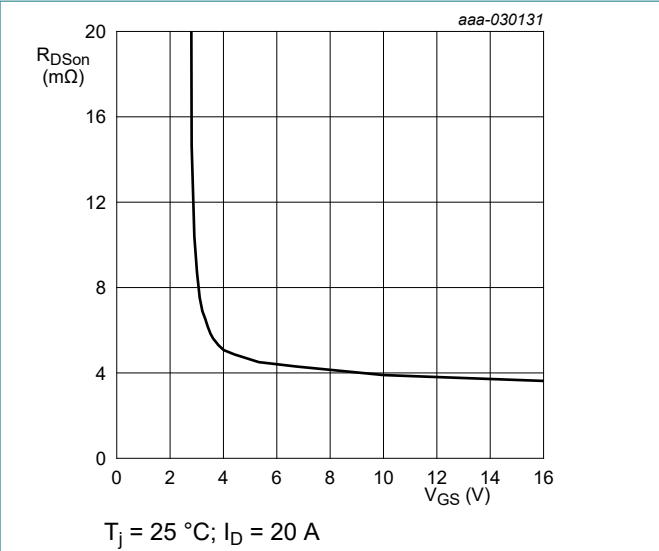
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}$	1.45	1.77	2.15	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	2.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	0.7	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.07	5	$\mu A$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	0.66	10	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	50	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

## N-channel 40 V, 5.0 mΩ logic level MOSFET in LPAK33

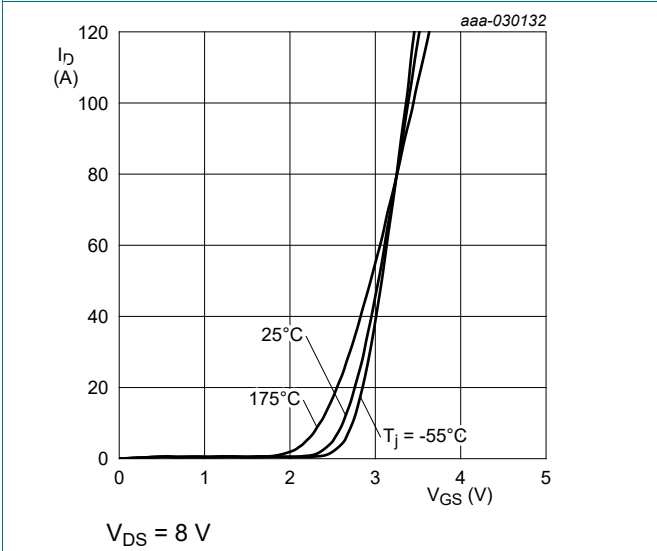
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	2.7	3.9	5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 105 °C; <a href="#">Fig. 12</a>	4	6	7.9	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 12</a>	4.4	6.6	8.7	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>	5.6	8.1	10.9	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>	3.4	4.9	6.4	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 105 °C; <a href="#">Fig. 12</a>	5.1	7.4	10.1	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 125 °C; <a href="#">Fig. 12</a>	5.6	8.2	11.1	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 12</a>	7.1	10	14	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.3	0.8	2	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	28	39	nC
		I <sub>D</sub> = 20 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	13	18	nC
Q <sub>GS</sub>	gate-source charge		-	4.9	7.4	nC
Q <sub>GD</sub>	gate-drain charge		-	2.9	5.9	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>	-	1879	2631	pF
C <sub>oss</sub>	output capacitance		-	442	619	pF
C <sub>rss</sub>	reverse transfer capacitance		-	68	150	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 20 V; R <sub>L</sub> = 1 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 5 Ω	-	18	-	ns
t <sub>r</sub>	rise time		-	22	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	17	-	ns
t <sub>f</sub>	fall time		-	12	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 20 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>	-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; <a href="#">Fig. 17</a>	-	24	-	ns
Q <sub>r</sub>	recovered charge	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V	-	18	-	nC
S	softness factor	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.66	-	
		I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -500 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 17</a>	-	0.45	-	



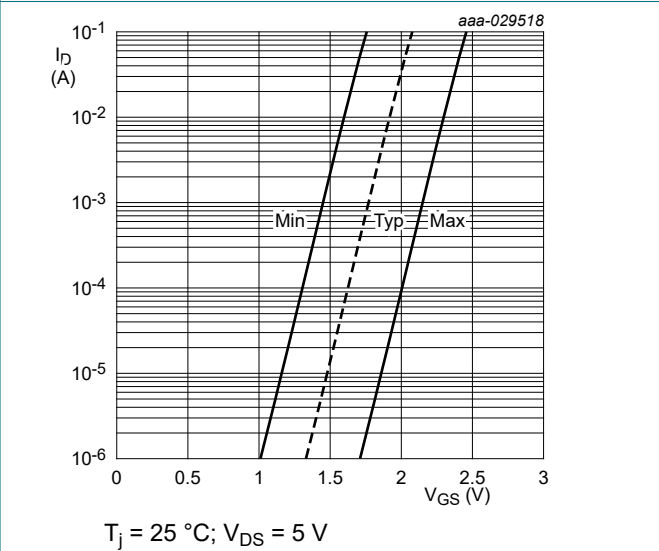
**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



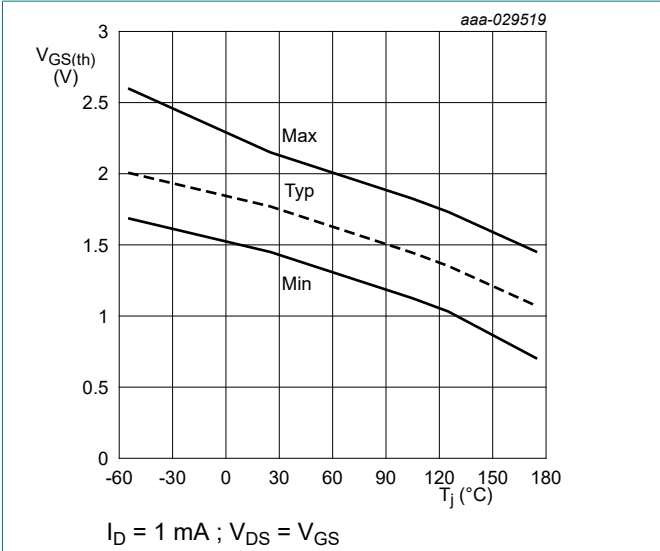
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**



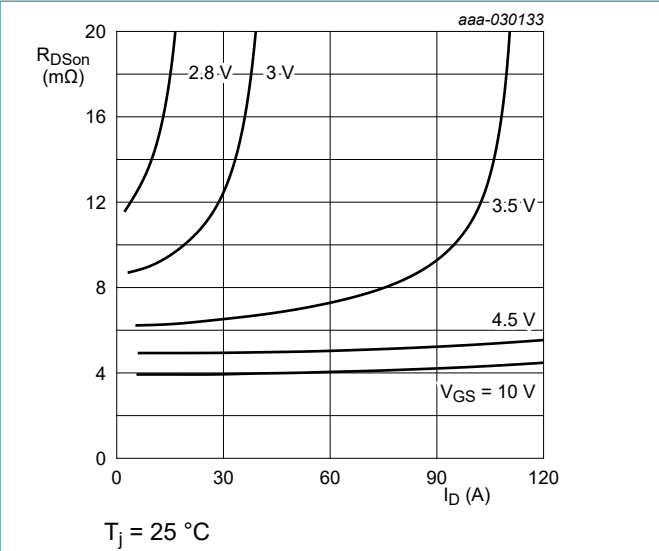
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



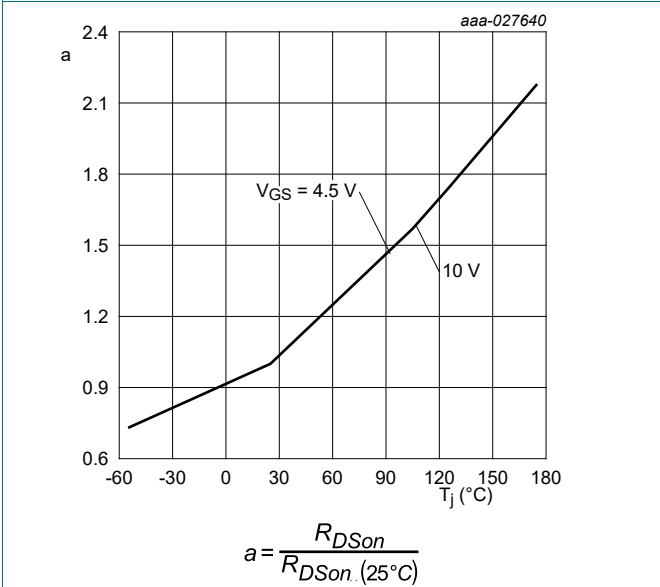
**Fig. 9. Sub-threshold drain current as a function of gate-source voltage**



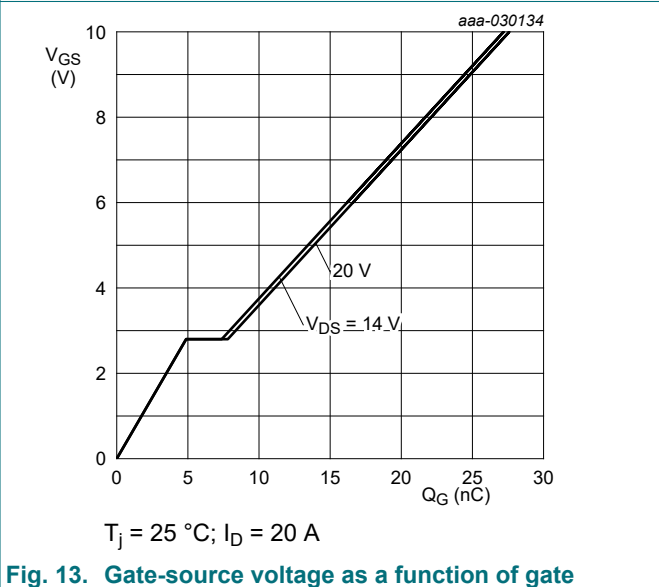
**Fig. 10. Gate-source threshold voltage as a function of junction temperature**



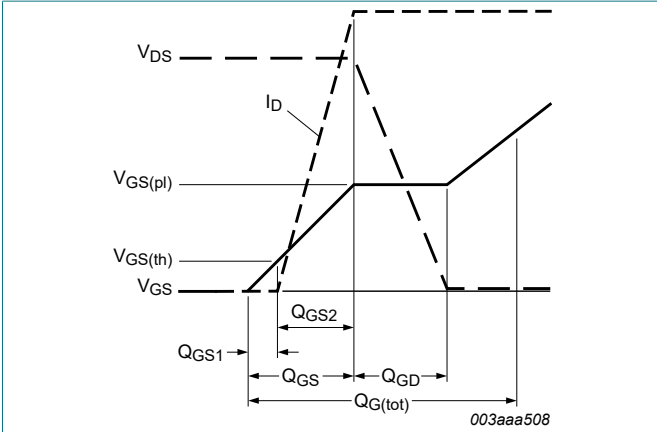
**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**



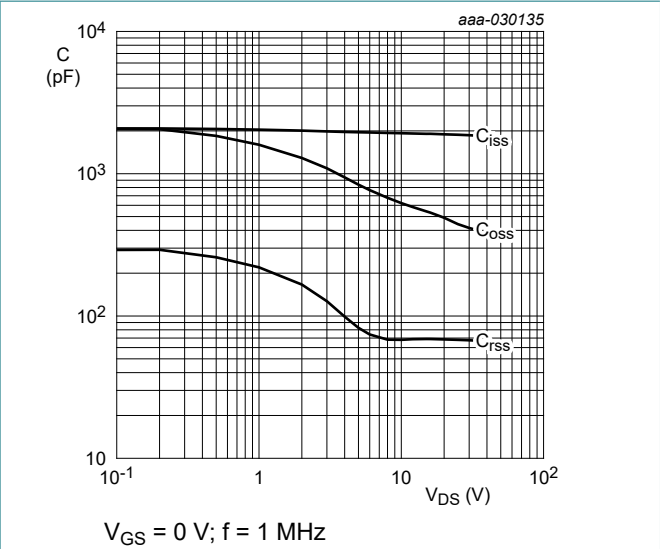
**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**



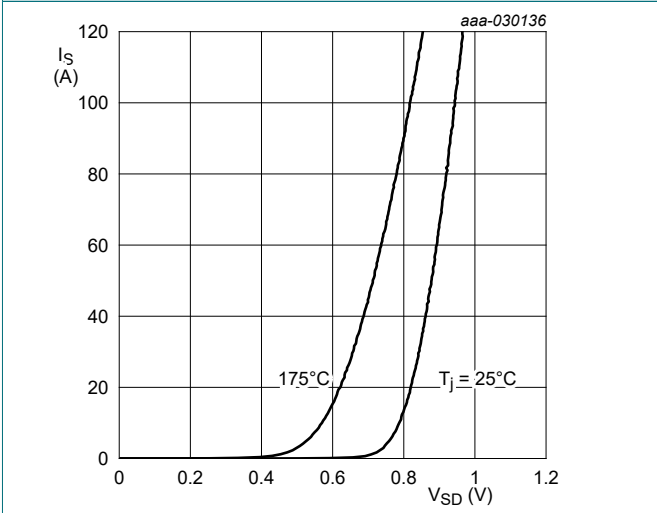
**Fig. 13. Gate-source voltage as a function of gate charge; typical values**



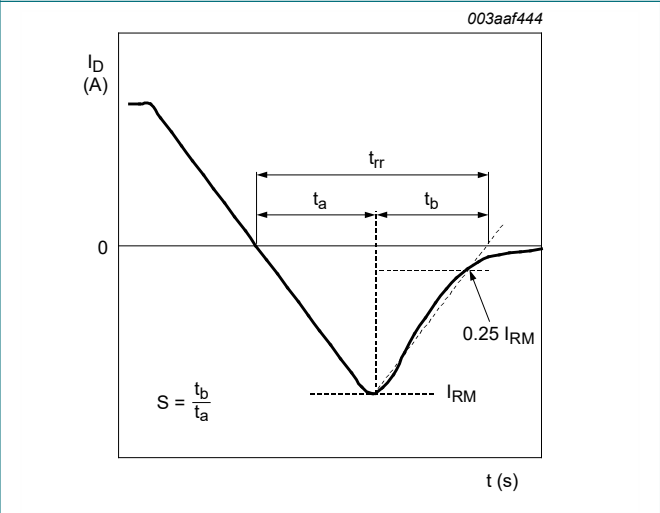
**Fig. 14. Gate charge waveform definitions**



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

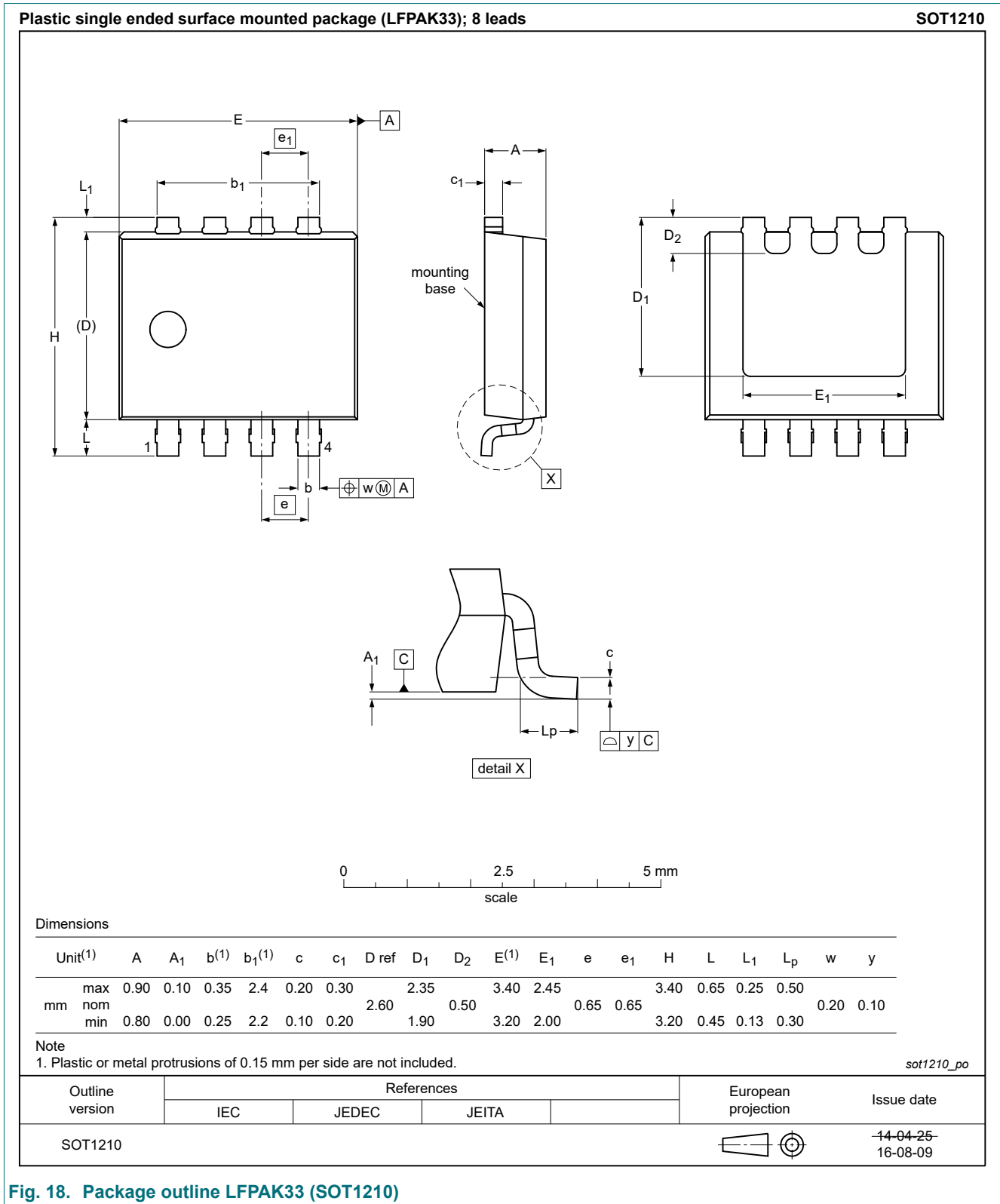


**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



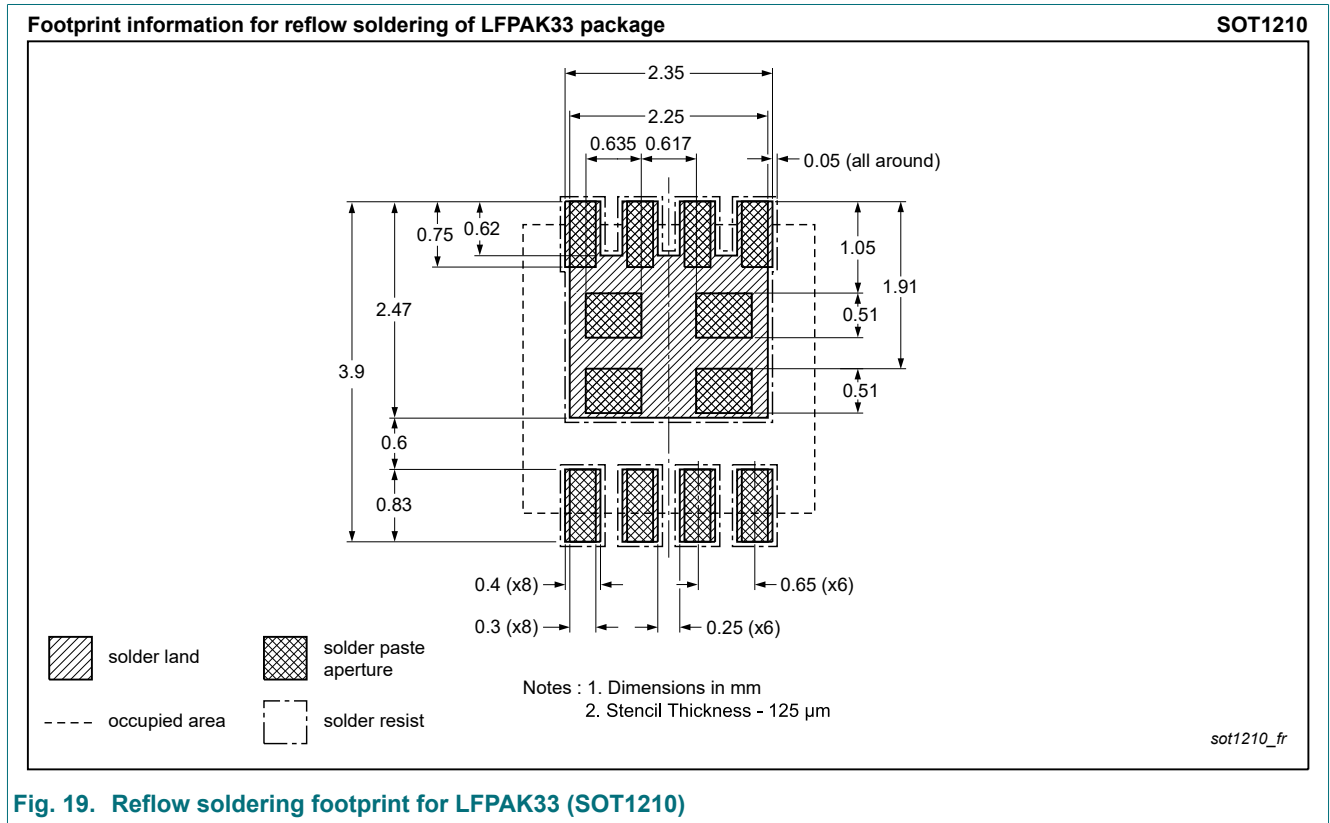
**Fig. 17. Reverse recovery timing definition**

### 11. Package outline



**Fig. 18. Package outline LPAK33 (SOT1210)**

## 12. Soldering



**Fig. 19. Reflow soldering footprint for LFPAK33 (SOT1210)**

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 13 March 2020

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