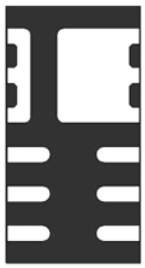
ECMF2-0730V12M12

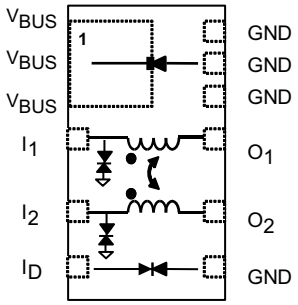
Common mode filter with ESD protection for USB2.0 interface

Datasheet - production data



µQFN-12L
1.35 mm x 2.6 mm

Figure 1. Pin configuration (top view)



V_{BUS} pin 1,2 and 3 must be connected together on the PCB.

Features

- High common mode attenuation from 0.65 GHz to 3 GHz:
  - -18 dB at 0.7 GHz
  - -30 dB at 0.9 GHz
  - -25 dB at 1.5 GHz
  - -20 dB at 2.4 GHz
  - -17 dB at 3 GHz
- V_{BUS} high power TVS diode:
  - V_{RM} = 13.2 V
  - I_{PP} (8/20 µs): 70 A
- Very low PCB space consumption
- Thin package: 0.55 mm max
- Lead free package
- High reduction of parasitic elements through integration

Complies with following standards

- IEC61000-4-2 level 4:
  - +/-15 kV (air discharge)
  - +/-8 kV (contact discharge)

Applications

- Mobile phone, smartphone
- Phablet
- Tablet
- Portable devices

Description

The ECMF2-0730V12M12 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on LTE, GSM and GPS band. The device integrates a high power TVS to protect the V_{BUS} line against surge.

1 Characteristics

Table 1. Absolute maximum rating (T_{amb} = 25 °C)

Symbol	Parameter			Value	Unit
V_{PP}	Peak pulse voltage	I_1, I_2, O_1, O_2, I_D	IEC61000-4-2 contact discharge IEC61000-4-2 air discharge	8 15	kV
		V_{BUS}	IEC61000-4-2 contact discharge IEC61000-4-2 air discharge	30 30	kV
I_{PP}	Peak pulse current (8/20 µs)			70	A
P_{PP}	Peak pulse power (8/20 µs)			1500	W
I_{RMS}	Maximum RMS current			100	mA
T_{OP}	Operating temperature			-40 to +85	°C
T_j	Maximum junction temperature			125	°C
T_{stg}	Storage temperature range			-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s			260	°C

Figure 2. V_{BUS} pins electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_{RM}	=	Leakage current
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage
I_{PP}	=	Peak pulse current
I_F	=	Forward current
V_F	=	Forward voltage
R_D	=	Dynamic impedance

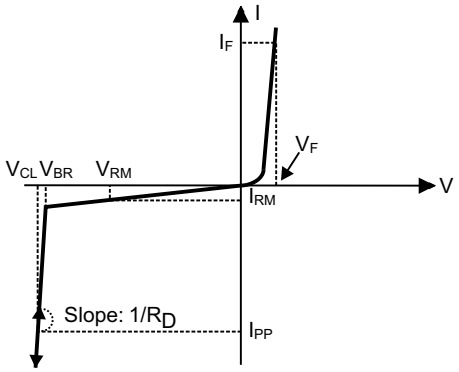


Figure 3. I_1, I_2 and I_D pins electrical characteristics (definitions)

Symbol Parameter

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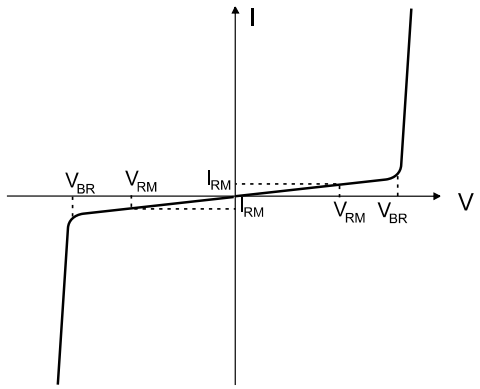


Table 2. Electrical characteristics (T_{amb} = 25°C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data Lines					
V_{BR}	I_R = 1 mA	5			V
I_{RM}	V_{RM} = 3 V per line			100	nA
R_{DC}	DC serial resistance		5.5		Ω
F_c	Differential mode cut-off frequency at -3 dB		1.2		GHz
I_D					
V_{BR}	I_R = 1 mA	5			V
I_{RM}	V_{RM} = 3 V			100	nA
V_{BUS}					
V_{BR}	I_R = 1 mA	13.5			V
I_{RM}	V_{RM} = 13.2 V		0.1	1	µA
V_{CL}	I_{PP} = 60 A - 8/20 µs		21	23	V
R_D	8/20 µs		0.1		Ω

Figure 4. Differential mode attenuation versus frequency ($Z_{0\ diff}$ = 100 Ω)

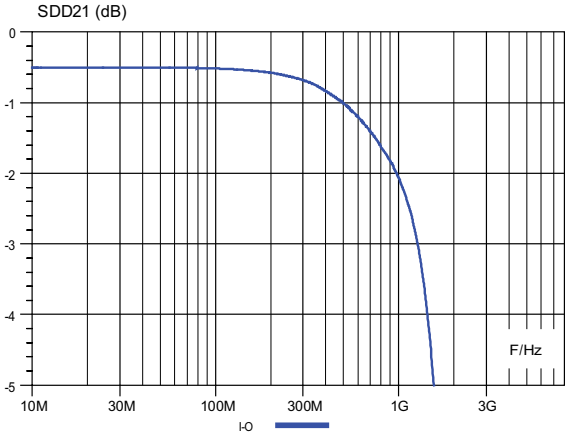


Figure 5. Common mode attenuation versus frequency ($Z_{0\ com}$ = 50 Ω)

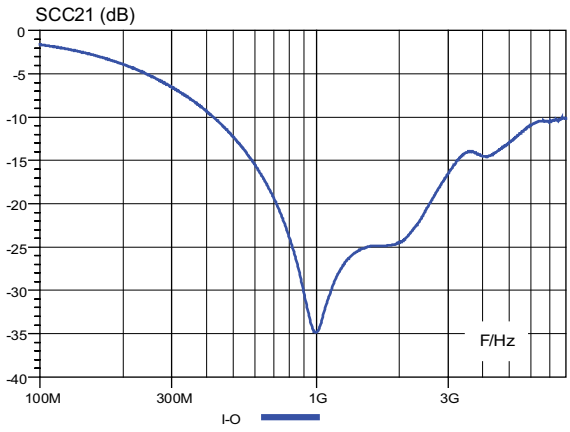


Figure 6. Return loss versus frequency ($Z_{0\ com}$ = 50 Ω)

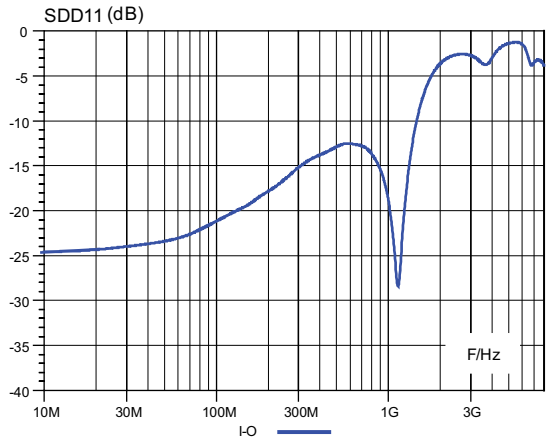


Figure 7. Return loss versus frequency ($Z_{0\ com}$ = 50 Ω)

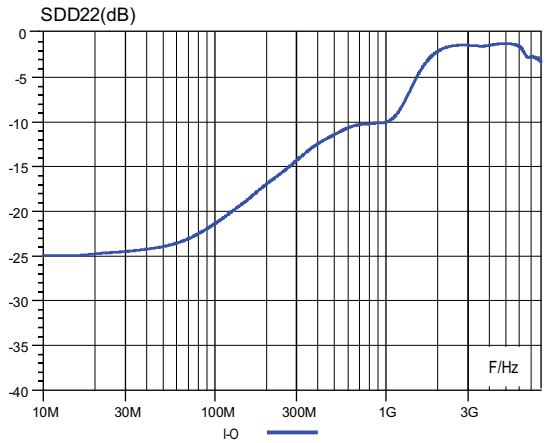


Figure 8. USB2.0 (480 Mbps) eye diagram without device

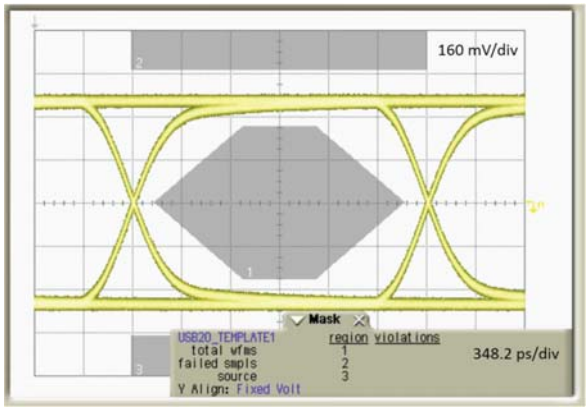


Figure 9. USB2.0 (480 Mbps) eye diagram with device

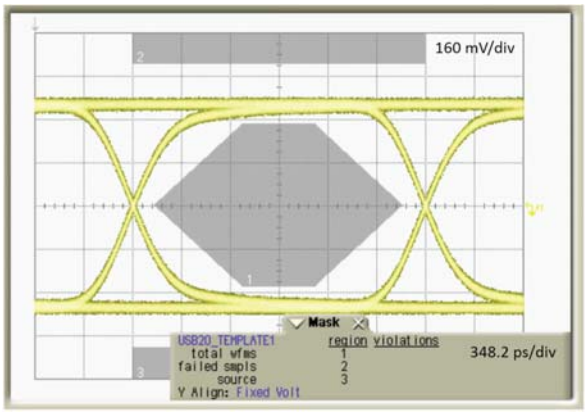


Figure 10. Data lines ESD response to IEC 61000-4-2 (+8 kV contact discharge)

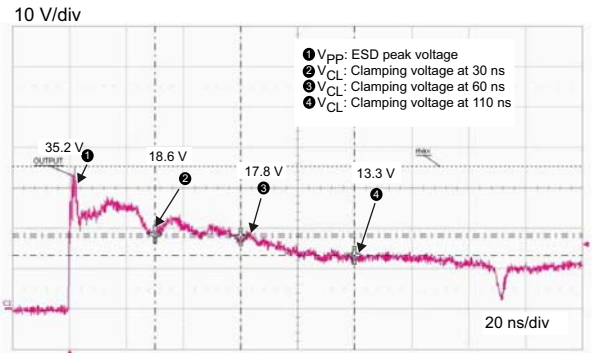


Figure 11. Data lines ESD response to IEC 61000-4-2 (-8 kV contact discharge)

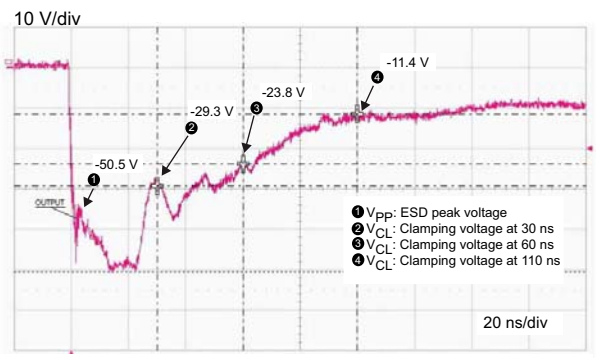


Figure 12. I_D ESD response to IEC 61000-4-2 (+8kV contact discharge)

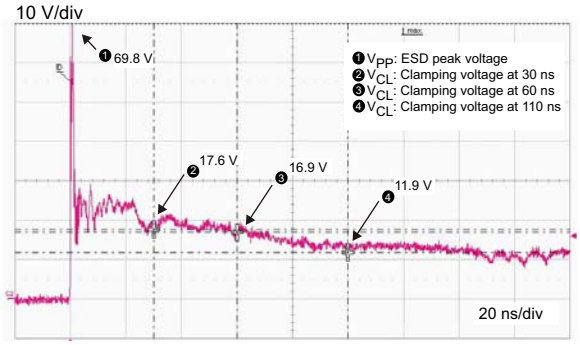


Figure 13. I_D ESD response to IEC 61000-4-2 (-8kV contact discharge)

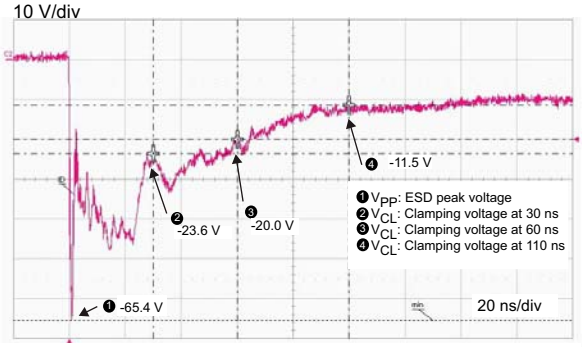


Figure 14. V_{BUS} ESD response to IEC 61000-4-2 (+30kV contact discharge)

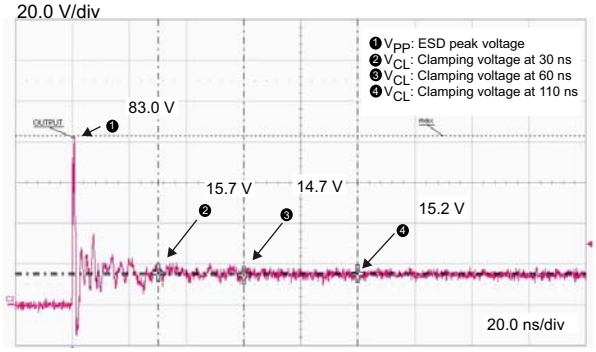


Figure 15. V_{BUS} ESD response to IEC 61000-4-2 (-30kV contact discharge)

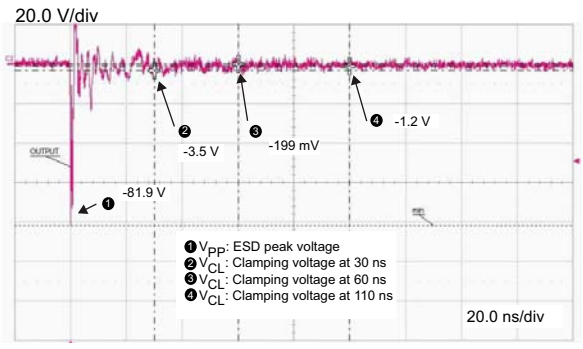


Figure 16. V_{BUS} peak pulse power dissipation versus initial junction temperature (maximum value)

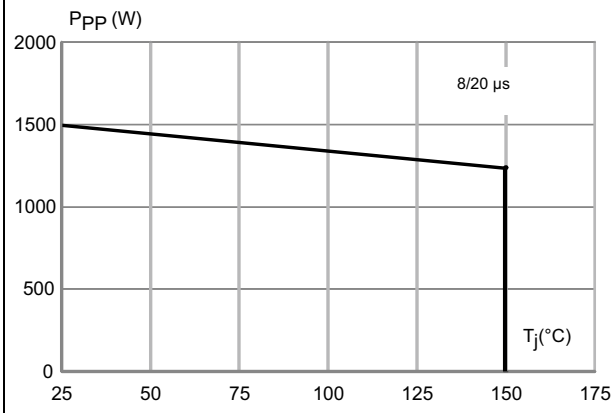


Figure 17. V_{BUS} peak pulse power versus exponential pulse duration (maximum value)

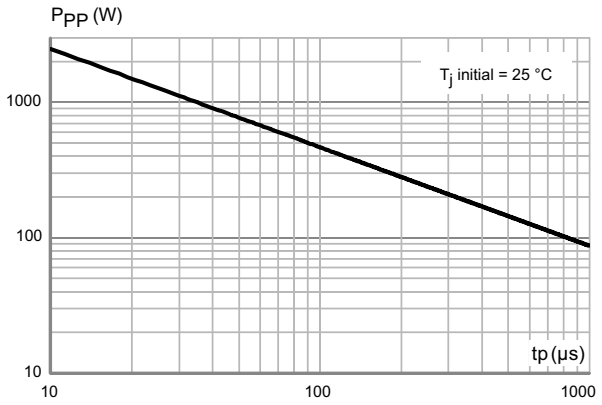


Figure 18. V_{BUS} peak pulse current versus clamping voltage (maximum value)

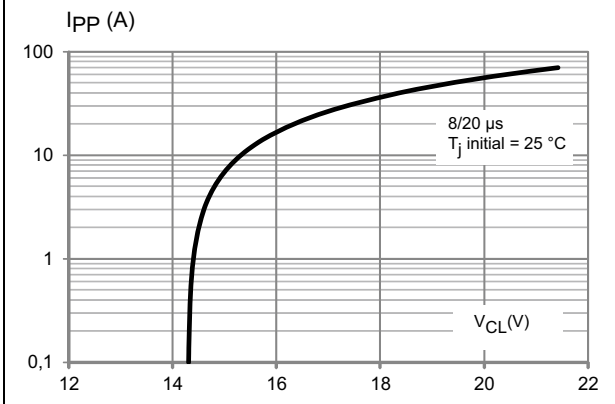
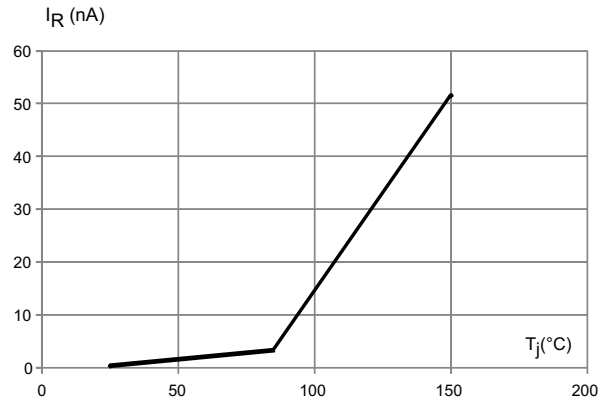


Figure 19. V_{BUS} leakage current versus junction temperature (typical value)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

2.1 µQFN-12L package information

Figure 20. µQFN-12L package outline

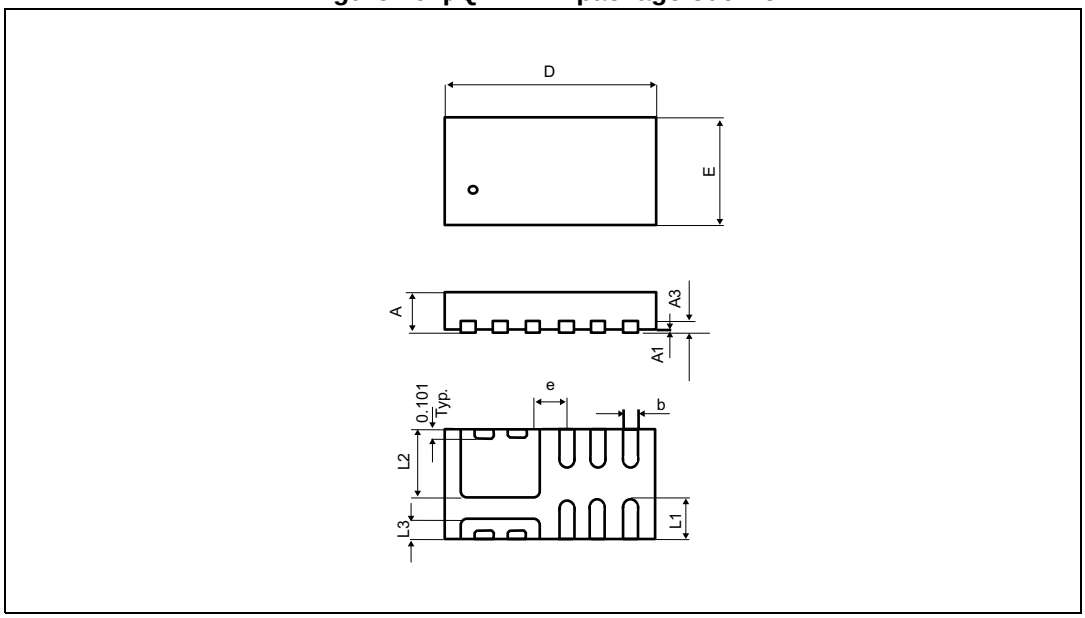


Table 3. µQFN-12L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.50	0.45	0.55	0.0197	0.0177	0.0217
A1	0.02	0.00	0.05	0.0008	0.0000	0.0020
A3	0.127			0.0050		
b	0.20	0.15	0.25	0.0079	0.0060	0.0099
D	2.60	2.55	2.65	0.0102	0.0100	0.1043
E	1.35	1.30	1.40	0.0531	0.0512	0.0551
e	0.40			0.0157		
L1	0.45	0.35	0.55	0.0177	0.0138	0.0217
L2	0.842	0.742	0.942	0.0331	0.0292	0.0371
L3	0.253	0.153	0.353	0.0099	0.0060	0.0139

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 21. Footprint

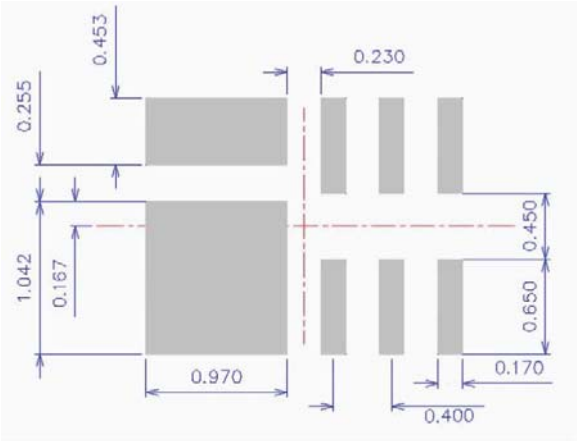
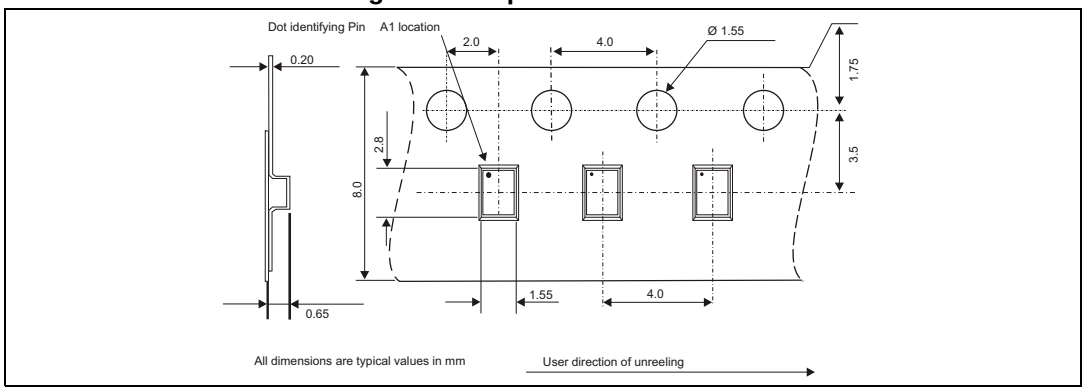


Figure 22. Marking

Note: The marking codes can be rotated by 90 ° or 180 ° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose

Figure 23. Tape and reel outline



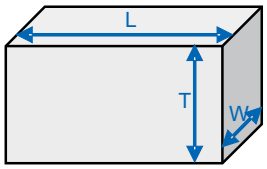
3 Recommendation on PCN assembly

3.1 Stencil opening design

3.1.1 General recommendation on stencil opening design

1. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 24. Stencil opening recommendation



2. General design rule

Stencil thickness (T) = 75 ~ 125 µm

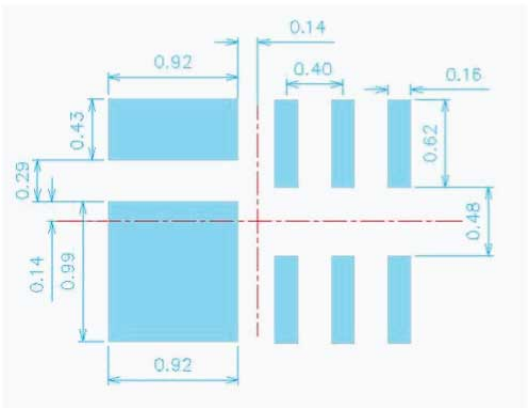
$$\text{Aspect ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect area} = \frac{LxW}{2T(L+W)} \geq 0.66$$

3.1.2 Reference design

1. Stencil opening thickness: 100 µm
2. Stencil opening for leads: opening to footprint ratio is 90%.

Figure 25. Recommended stencil window position



3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

3.3 Placement

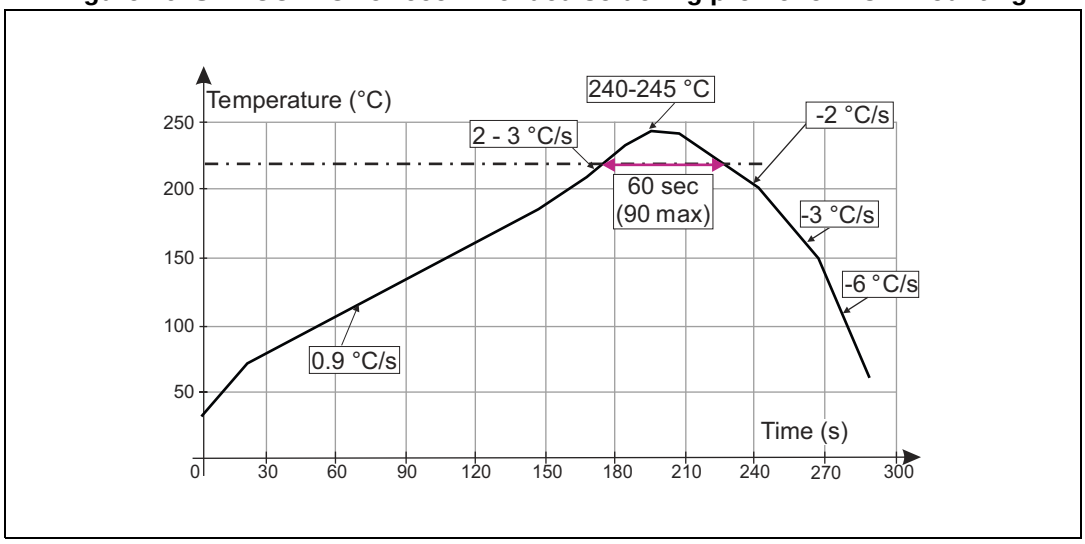
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away

3.5 Reflow profile

Figure 26. ST ECOPACK® recommended soldering profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

3.5.1 General advice about reflow conditions:

For each individual board, the appropriate heat profile has to be adjusted experimentally. The proposed profiles are just starting points. In every case, the following precautions have to be considered:

- Always preheat the device. The purpose of this step is to minimize the rate of temperature rise to less than 2 °C per second in order to minimize thermal shock on the component.

- Dry out sections ensure that the solder paste is fully dried before starting reflow step. Also, this step allows the temperature gradient on the board to be evened out.

- Peak temperature should be at least 30 °C higher than the melting point of the chosen solder alloy to ensure the reflow quality. In any case the peak temperature should not exceed 260 °C.

4 Ordering information

Figure 27. Ordering information scheme

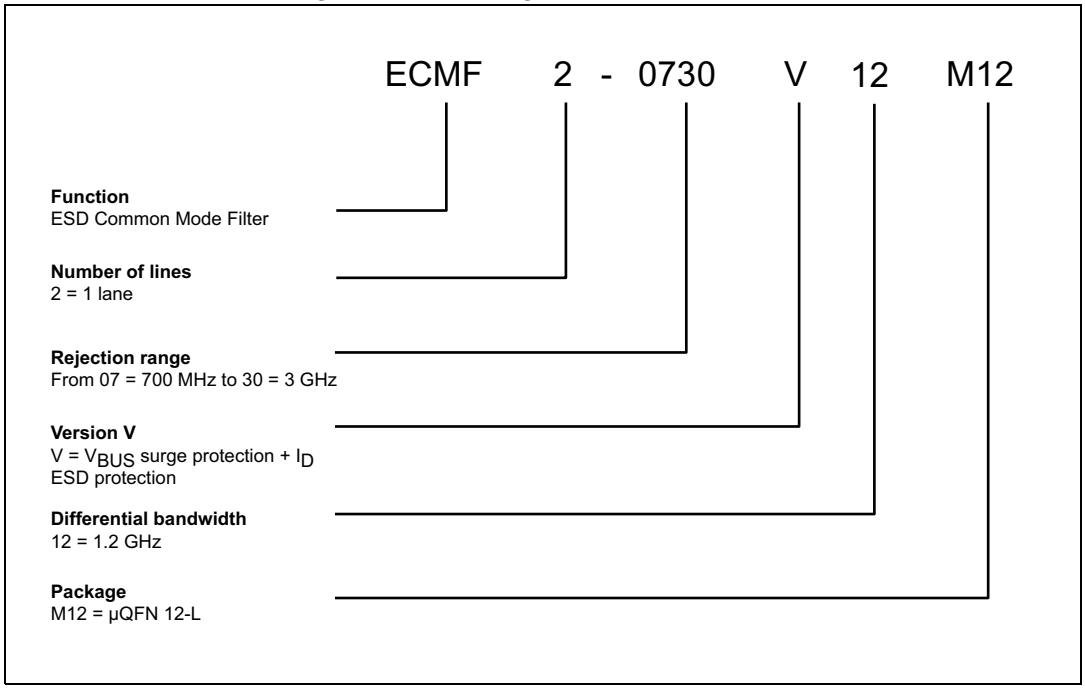


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ECMF2-0730V12M12	M4	µQFN-12L	5.3 mg	3000	Tape and reel

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
01-Mar-2016	1	Initial release.