

OptiMOS™ -5 Power-Transistor



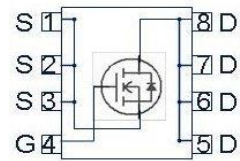
Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	42	mΩ
I_D	18	A

PG-TSDSON-8



Type	Package	Marking
IAUZ18N10S5L420	PG-TSDSON-8	5N1L420

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	18	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	13	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	72	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=7\text{ A}$	11	mJ
Avalanche current, single pulse	I_{AS}	-	7	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$ $T_J=175\text{ °C}$	30	W
Operating and storage temperature	T_J , T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	-

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	5.0	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm ² cooling area ²⁾	-	-	62	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=8\mu A$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	-	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125^\circ\text{C}^{1)}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=9A$	-	46	55	m Ω
		$V_{GS}=10V, I_D=9A$	-	34.5	42	
Gate resistance ¹⁾	R_G		-	1.8	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=50V,$ $f=1MHz$	-	356	470	pF
Output capacitance	C_{oss}		-	68	88	
Reverse transfer capacitance	C_{rss}		-	6	9	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V,$ $I_D=18A, R_G=3.5\Omega$	-	1	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	3	-	
Fall time	t_f		-	3	-	

Gate Charge Characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=50V, I_D=9A,$ $V_{GS}=0 \text{ to } 10V$	-	1.2	1.7	nC
Gate to drain charge	Q_{gd}		-	1.2	2.0	
Gate charge total	Q_g		-	5.4	8	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	V

Reverse Diode

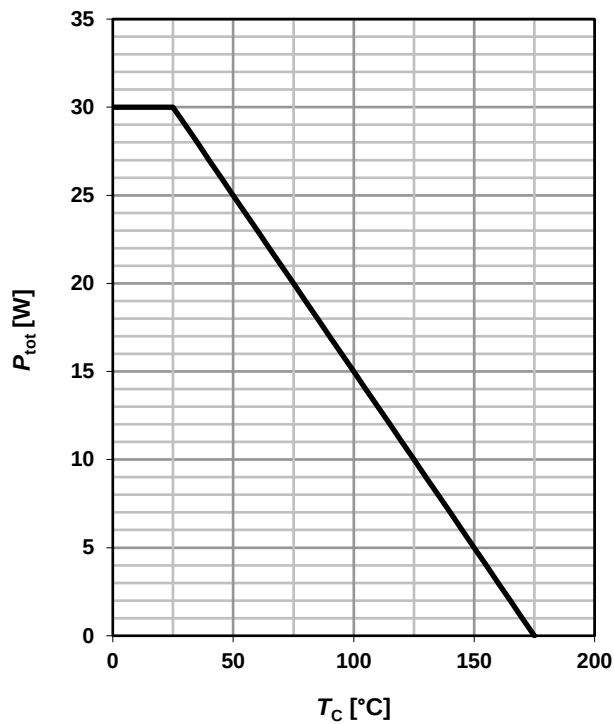
Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ C$	-	-	18	A
Diode pulse current	$I_{S,pulse}$		-	-	72	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=9A,$ $T_J=25^\circ C$	-	0.9	1.1	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50V, I_F=18A,$ $di_F/dt=100A/\mu s$	-	36	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	33	-	nC

¹⁾ Specified by design. Not subject to production test.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

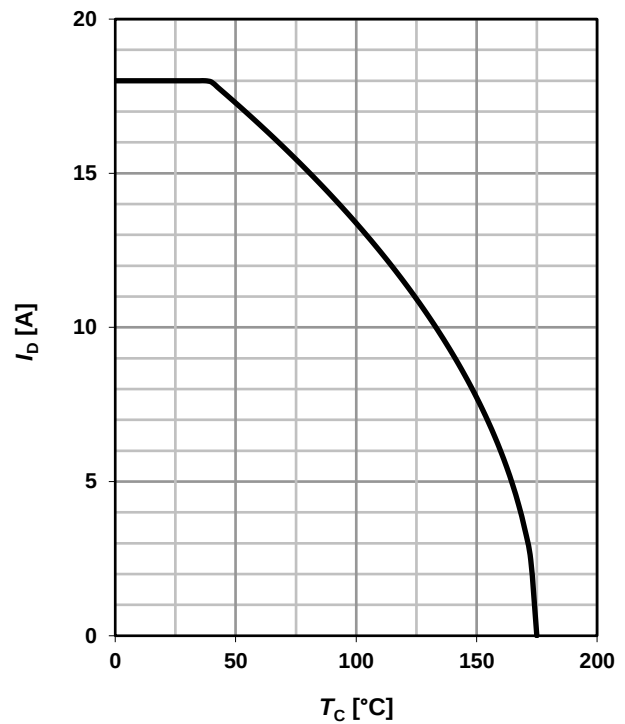
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

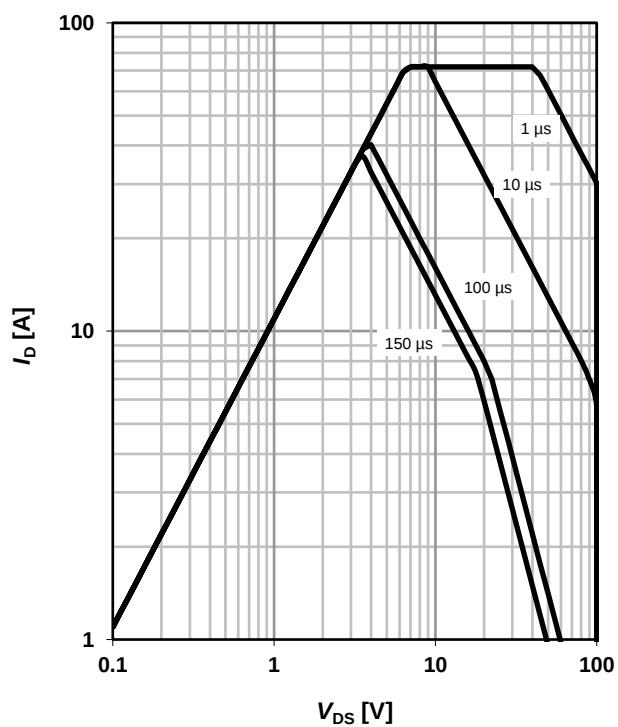
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

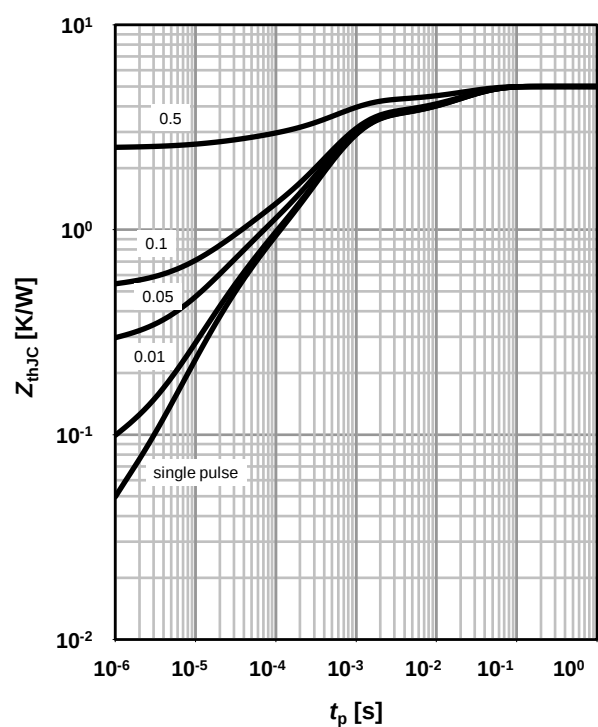
parameter: t_p



4 Max. transient thermal impedance

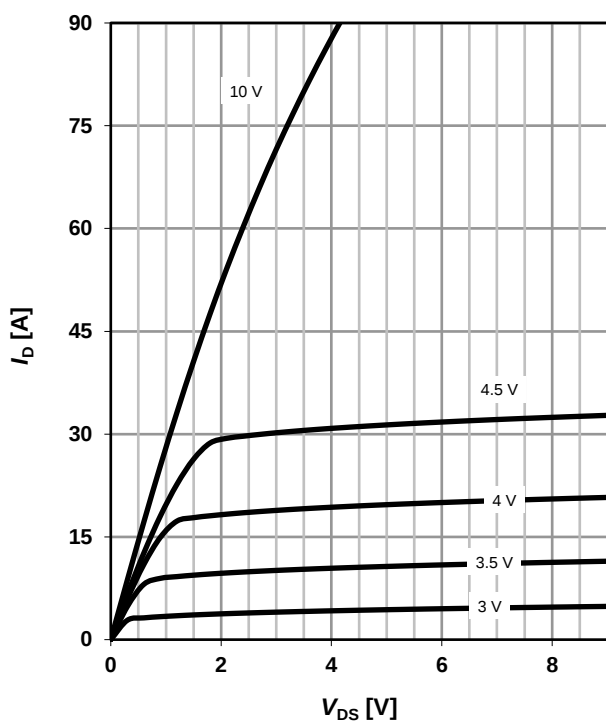
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



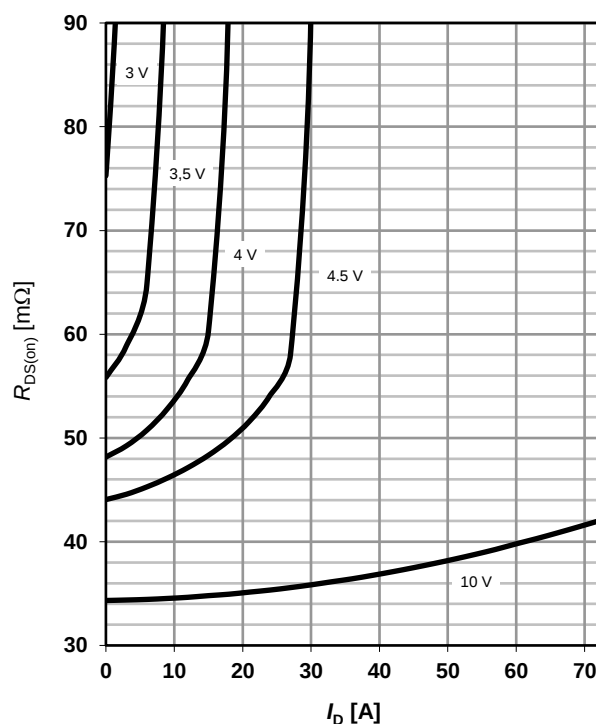
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


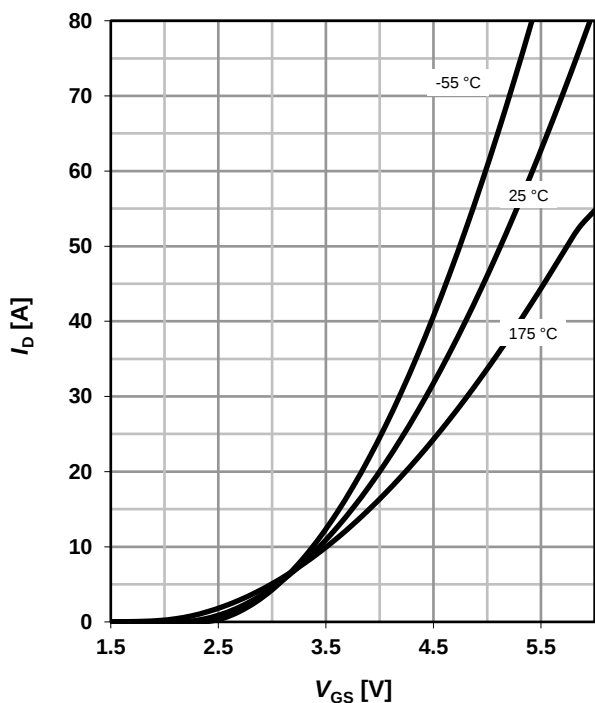
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


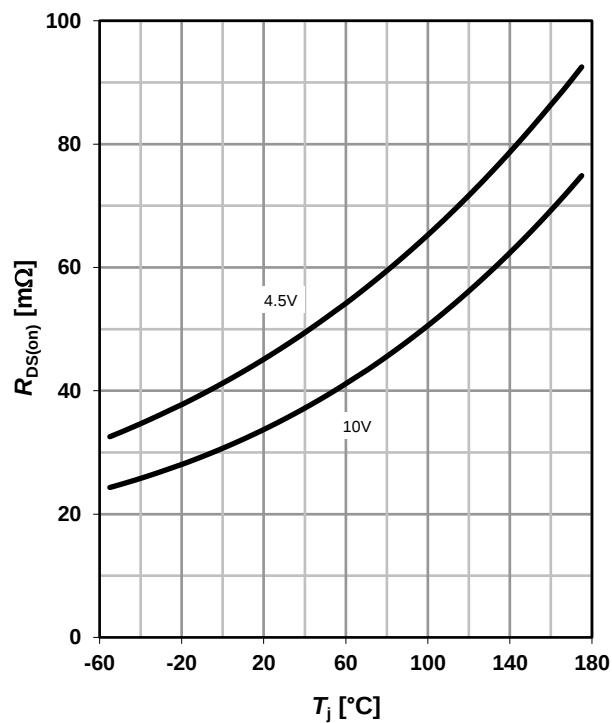
7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j


8 Typ. drain-source on-state resistance

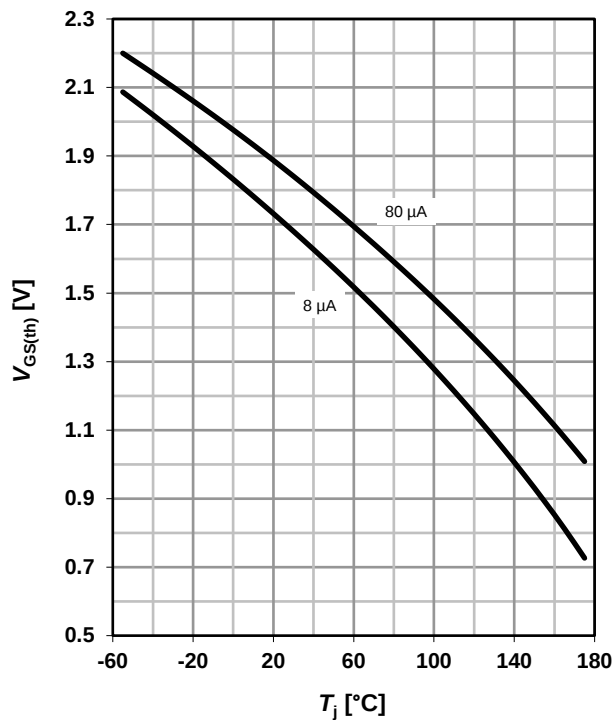
 $R_{DS(on)} = f(T_j); I_D = 9\text{ A}$

Parameter: V_{GS}


9 Typ. gate threshold voltage

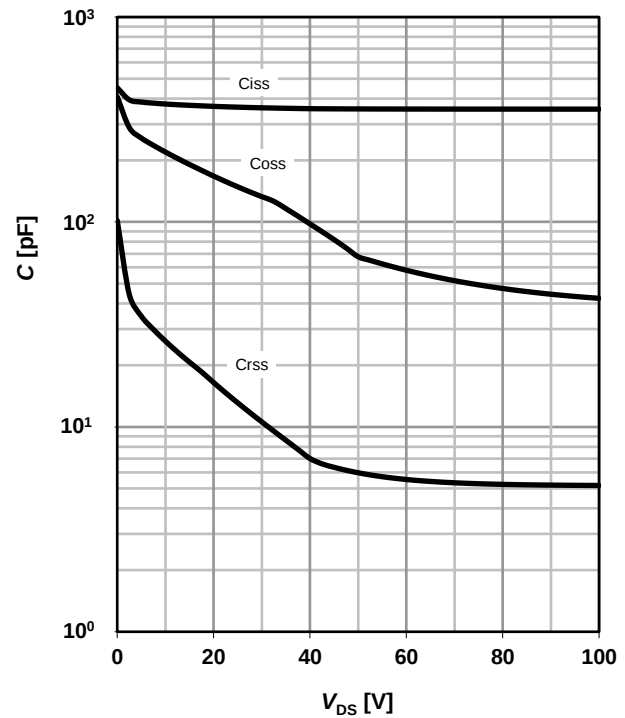
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

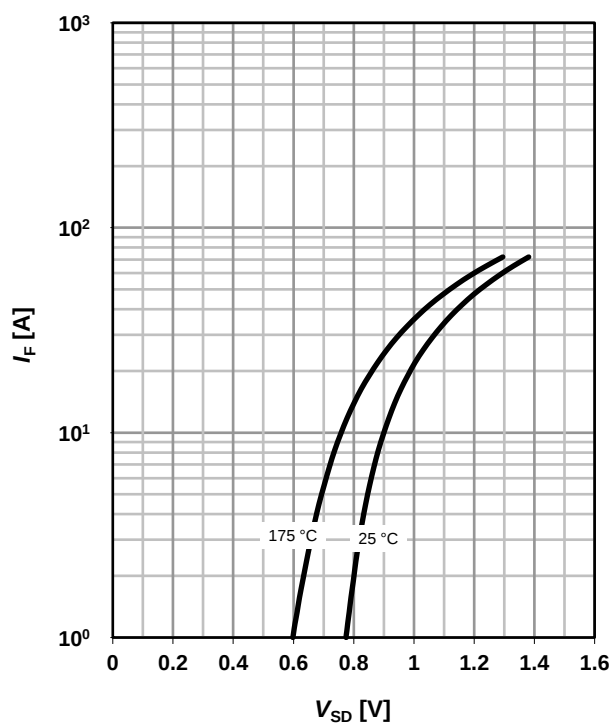
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

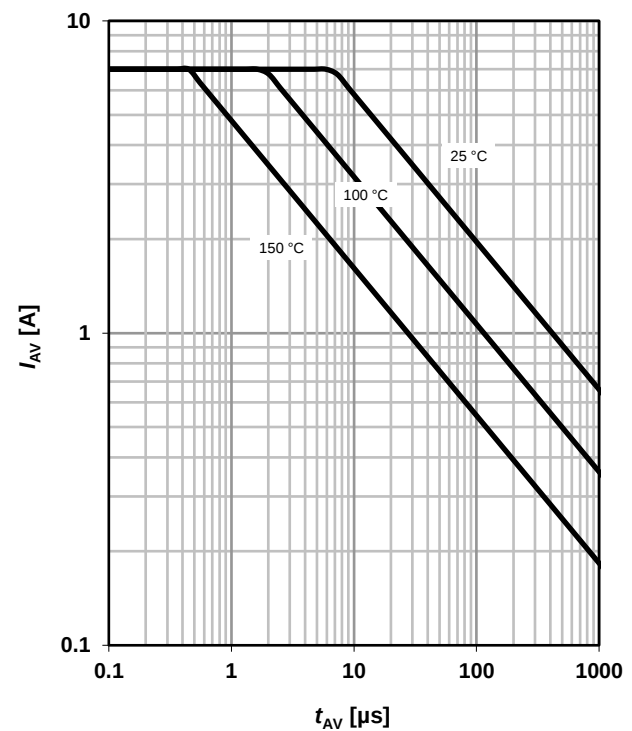
parameter: T_j



12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

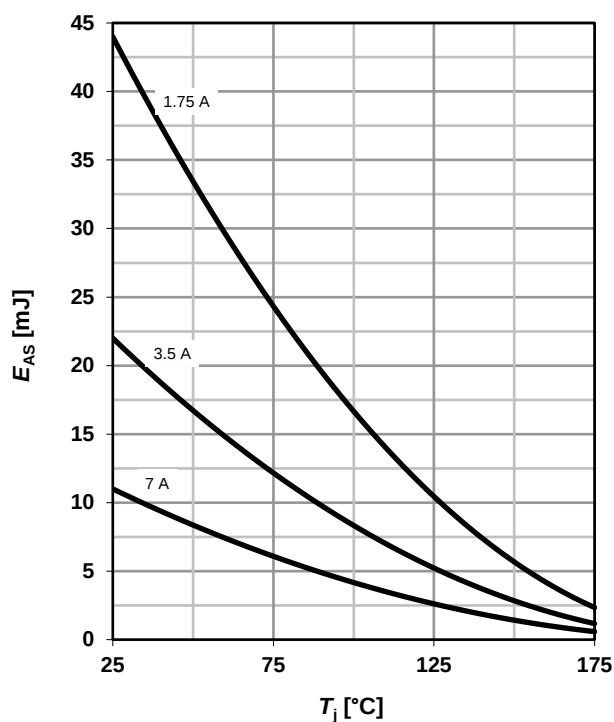
parameter: $T_{j(start)}$



13 Avalanche energy

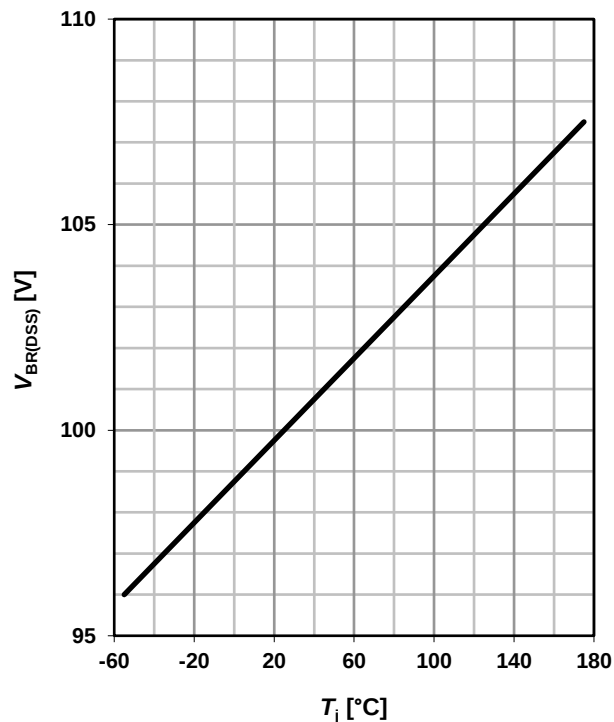
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

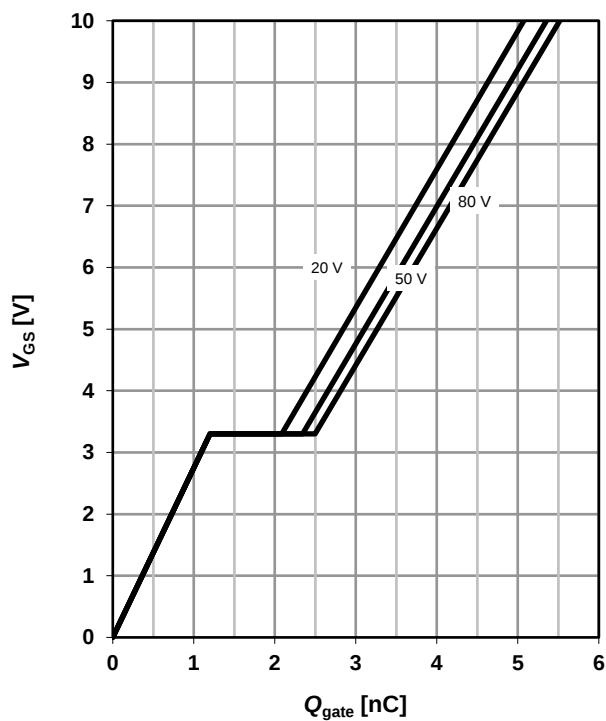
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



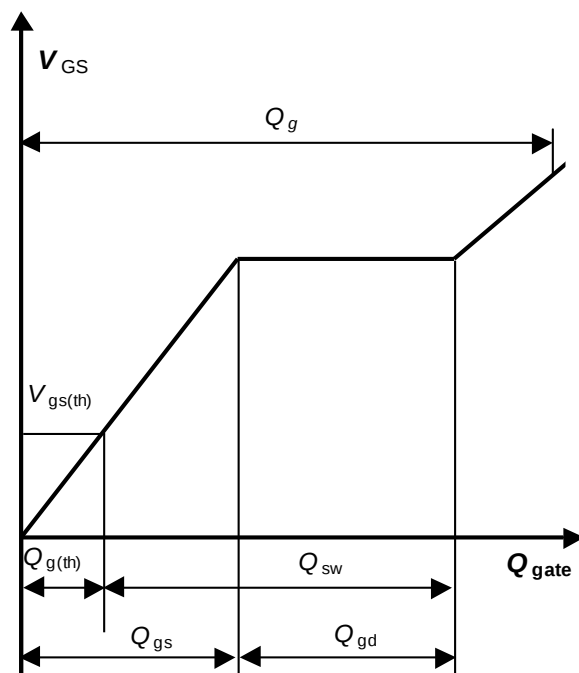
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 9 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of a 3x3 LED array package showing top, side, and detail views with dimensions and tolerances.

Top View:

- Overall width: 3.3 ± 0.1
- Overall height: 3.3 ± 0.1
- Pin 1 Marking: Indicated by a circle and leader line.

Side View:

- Package height: 1 ± 0.1
- LED chip height: 0.2 ± 0.1
- Stand-off height: $0 \dots 0.05$
- LED chip width: 0.1
- LED chip length: 1.85 ± 0.1
- LED chip spacing: 0.25 ± 0.1
- LED chip thickness: 0.05
- LED chip position: Z
- LED chip width: 1.15 MAX.

Detail View (LED Chip):

- LED chip width: 0.07 MIN.
- LED chip height: 0.05 MIN.

Bottom View:

- Overall width: 2.29 ± 0.1
- Overall height: 2.11 ± 0.1
- Pin 1 Marking: Indicated by a circle and leader line.
- Pin 1 Marking: 0.34 ± 0.1
- Pin 1 Marking: $8x$
- Pin 1 Marking: $3 \times 0.65 = 1.95$
- Pin 1 Marking: 0.65
- Pin 1 Marking: 0.65 ± 0.1
- Pin 1 Marking: 0.4 ± 0.1
- Pin 1 Marking: 2.11 ± 0.1
- Pin 1 Marking: 0.3
- Pin 1 Marking: 0.34 ± 0.1
- Pin 1 Marking: $8x$
- Pin 1 Marking: $3 \times 0.65 = 1.95$

(a) Top view

Dimensions (mm):

- Overall width: 2.29
- Overall height: 2.36
- Top edge features: 0.65, 0.34, 0.65, 0.34
- Right edge features: 0.48, 1.58, 1.45
- Bottom edge features: 0.9, 0.45, 0.34, 1.64, 0.65, 0.34

(b) Side view

Dimensions (mm):

- Overall width: 0.475
- Overall height: 1.22
- Top edge features: 0.31, 0.325, 0.41, 0.24, 0.6, 1.4, 0.7
- Right edge features: 0.35, 1.55, 0.35, 1.09, 0.2, 0.41, 0.24, 0.41
- Bottom edge features: 0.3, 0.67, 0.24, 0.41

Legend:

- Copper
- Solder Mask
- Stencil Apertures

PIN 1
INDEX MARKING

8

12

3.6

0.5

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Revision History

Version	Date	Changes
Revision 1.0	23.07.2019	Final Data Sheet