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CCM-PFC

ICE3PCS02G

Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)

Power Management & Supply

Never stop thinking

Revision History: Datasheet

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Standalone Power Factor Correction (PFC) Controller in Continuous Conduction Mode (CCM)

ICE3PCS02G
PG-DSO-8

Product Highlights

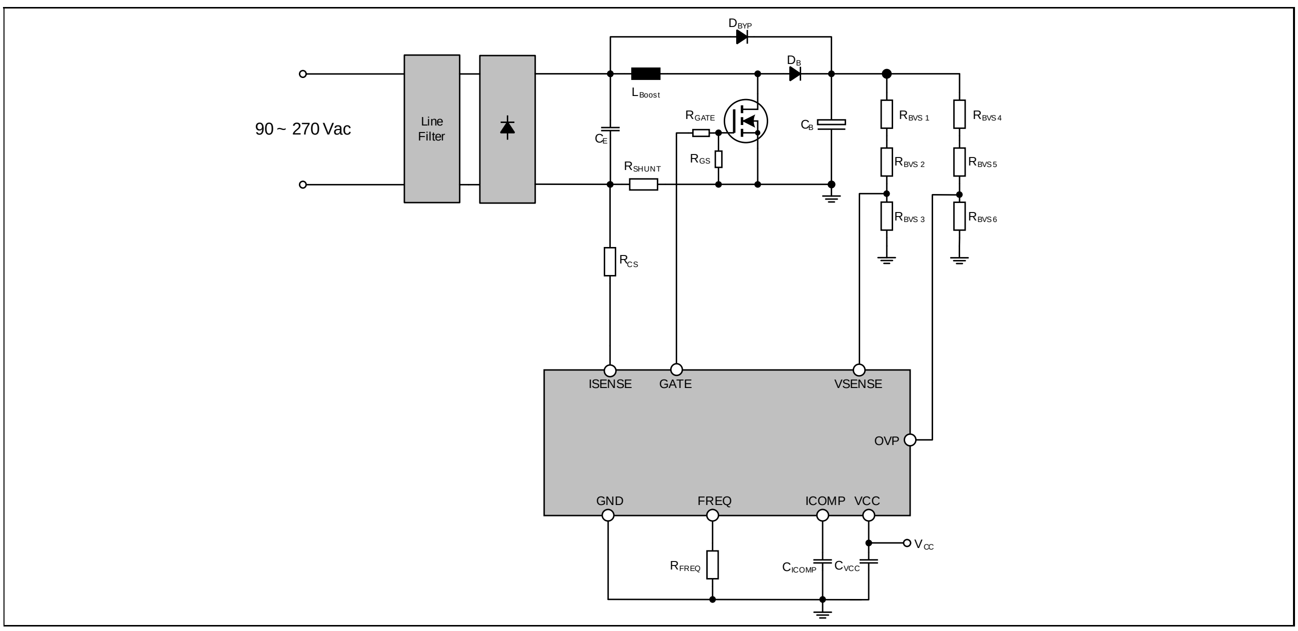
- High efficiency over the whole load range
- Lowest count of external components
- Accurate and adjustable switching frequency
- Integrated digital voltage loop compensation
- Fast output dynamic response during load jump
- External synchronization
- Low peak current limitation

Features

- Continuous current operation mode PFC
- Wide input range of Vcc up to 25V
- Enhanced dynamic response without input current distortion
- External current loop compensation for greater user flexibility
- Open loop protection
- Second over bulk voltage protection
- Maximum duty cycle of 95% (typical)

Description

The ICE3PCS02G is a 8-pins wide input range controller IC for active power factor correction converters. It is designed for converters in boost topology, and requires few external components. Its power supply is recommended to be provided by an external auxiliary supply which will switch on and off the IC.



Type	Package
ICE3PCS02G	PG-DSO-8

1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	ISENSE	Current Sense Input
2	GND	IC Ground
3	ICOMP	Current Loop Compensation
4	FREQ	Switching Frequency Setting
5	OVP	Over Voltage Protection
6	VSENSE	Bulk Voltage Sense
7	VCC	IC Supply Voltage
8	GATE	Gate Drive

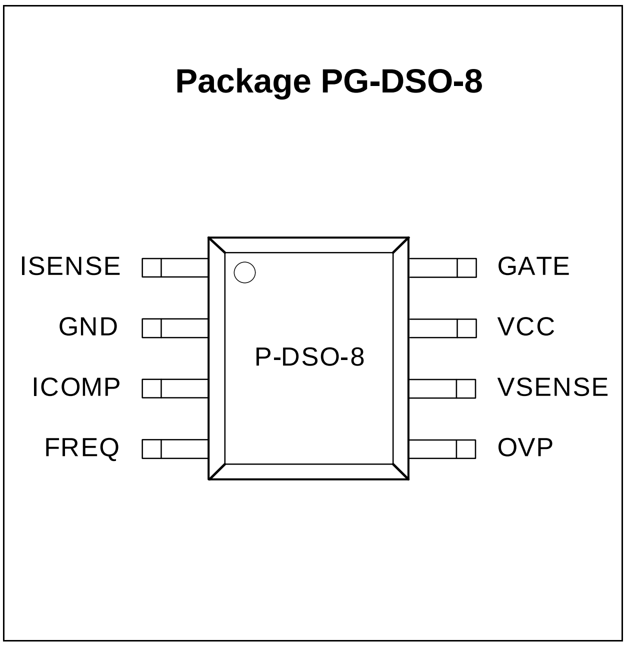


Figure 1 Pin Configuration (top view)

1.2 Pin Functionality

ISENSE (Current Sense Input)

The ISENSE Pin senses the voltage drop at the external sense resistor (R_{SHUNT}). This is the input signal for the average current regulation in the current loop. It is also fed to the peak current limitation block.

During power up time, high inrush currents cause high negative voltage drop at R_{SHUNT}, driving currents out of pin 1 which could be beyond the absolute maximum ratings. Therefore a series resistor (R_{CS}) of around 50Ω is recommended in order to limit this current into the IC.

GND (IC Ground)

The ground potential of the IC.

ICOMP (Current Loop Compensation)

Low pass filter and compensation of the current control loop. The capacitor which is connected at this pin integrates the output current of OTA6 and averages the current sense signal.

FREQ (Frequency Setting)

This pin allows the setting of the operating switching frequency by connecting a resistor to ground. The frequency range is from 21kHz to 250kHz.

OVP

A resistive voltage divider from bulk voltage to GND can set the over voltage protection threshold. This additional OVP is able to ensure system safety operation.

VSENSE

VSENSE is connected via a resistive divider to the bulk voltage. The voltage of VSENSE relative to GND represents the output voltage. The bulk voltage is monitored for voltage regulation, over voltage protection and open loop protection.

VCC

VCC provides the power supply of the ground related to IC section.

GATE

GATE is the output for driving the PFC MOSFET.Its gate drive voltage is clamped at 15V (typically).

2 Block Diagram

A functional block diagram is given in Figure 2. Note that the figure only shows the brief functional block and does not represent the implementation of the IC.

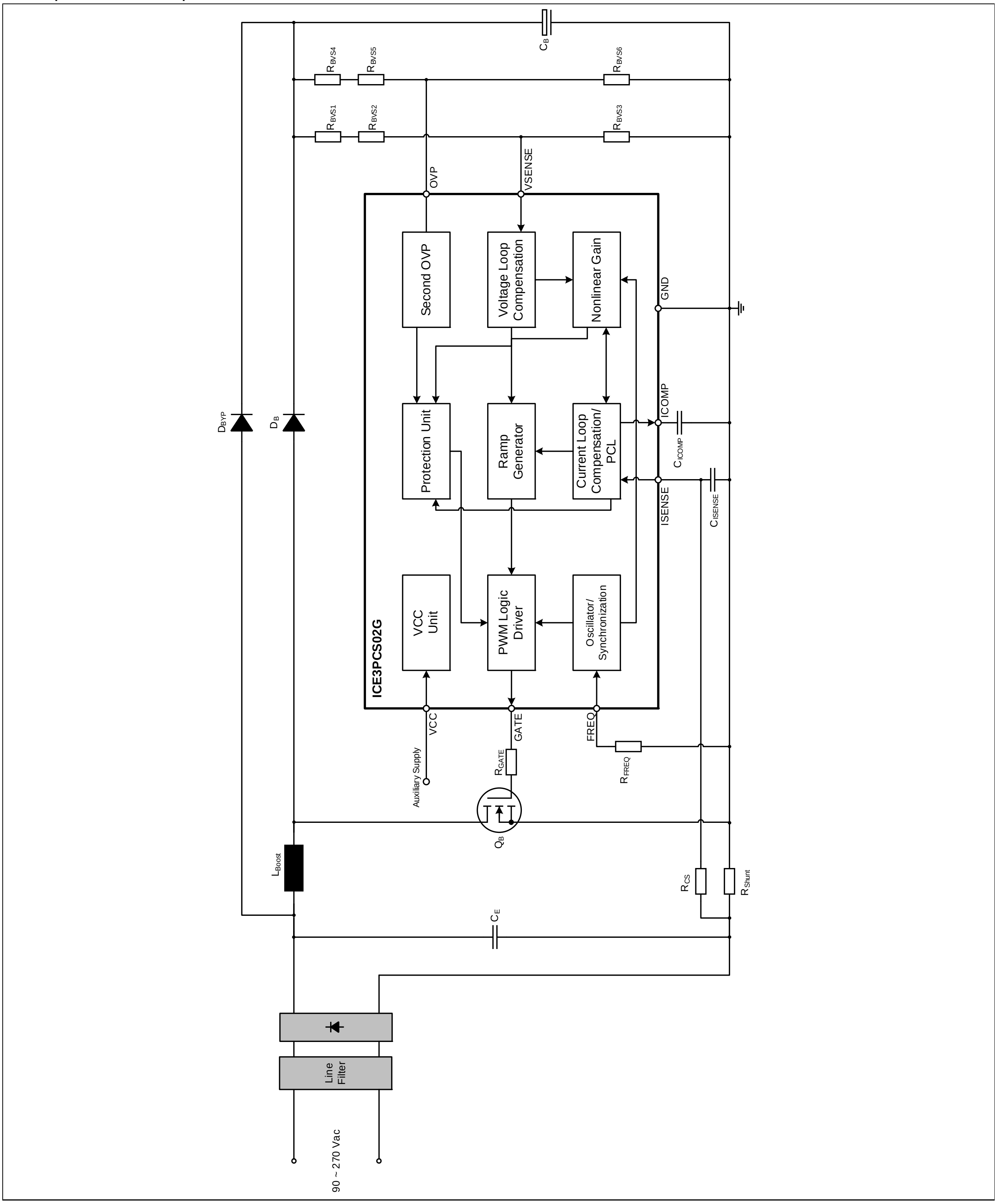


Figure 2 Block Diagram

Table 1 Bill Of Material

Component	Parameters
Rectifier Bridge	GBU8J
C_E	100nF/X2/275V
L_{Boost}	750uH
Q_B	IPP60R199CP
D_{BYP}	MUR360
D_B	IDT04S60C
C_B	220µF/450V
R_{shunt}	60mΩ
C_{isense}	1nF
R_{CS}	50Ω
R_{GATE}	3.3Ω
R_{FREQ}	67kΩ
C_{ICOMP}	4.7nF/25V
$R_{BVS1...2}$	1.5MΩ
R_{BVS3}	18.85kΩ
$R_{BVS4...5}$	2MΩ
R_{BVS6}	23kΩ

3 Functional Description

3.1 General

The ICE3PCS02G is a 8-pins control IC for power factor correction converters. It is suitable for wide range line input applications from 85 to 265 VAC with overall efficiency above 90%. The IC supports converters in boost topology and it operates in continuous conduction mode (CCM) with average current control.
The IC operates with a cascaded control; the inner current loop and the outer voltage loop. The inner current loop of the IC controls the sinusoidal profile for the average input current. It uses the dependency of the PWM duty cycle on the line input voltage to determine the corresponding input current. This means the average input current follows the input voltage as long as the device operates in CCM. Under light load condition, depending on the choke inductance, the system may enter into discontinuous conduction mode (DCM) resulting in a higher harmonics but still meeting the Class D requirement of IEC 1000-3-2.
The outer voltage loop controls the output bulk voltage, integrated digitally within the IC. Depending on the load condition, internal PI compensation output is converted to an appropriate DC voltage which controls the amplitude of the average input current.
The IC is equipped with various protection features to ensure safe operating condition for both the system and device.

3.2 Power Supply

An internal under voltage lockout (UVLO) block monitors the VCC power supply. As soon as it exceeds 12.0V and voltage at pin 6 (VSENSE) >0.5V, the IC begins operating its gate drive and performs its startup as shown in Figure 3.
If VCC drops below 11V, the IC is off. The IC will then be consuming typically 1.4mA, whereas consuming 6.4mA during normal operation
The IC can be turned off and forced into standby mode by pulling down the voltage at pin 6 (VSENSE) below 0.5V.

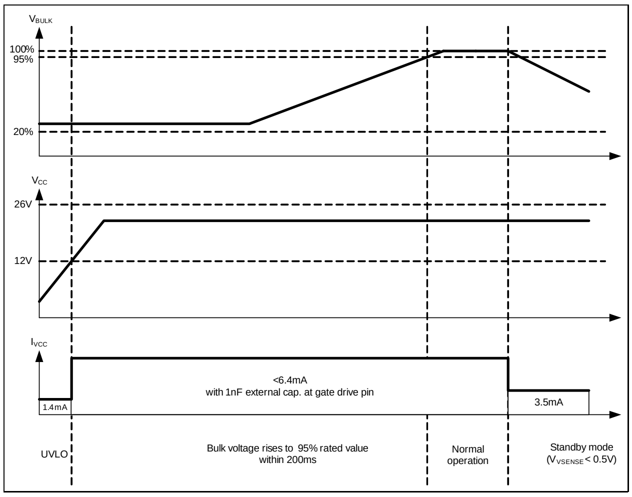


Figure 3 State of Operation respect to VCC

3.3 Start-up

During power up when the Vout is less than 95% of the rated level, internal voltage loop output increases from initial voltage under the soft-start control. This results in a controlled linear increase of the input current from 0A thus reducing the stress in the external components.

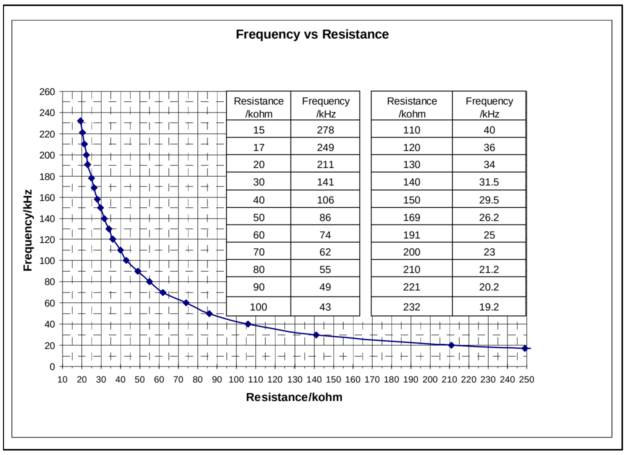
Once Vout has reached 95% of the rated level, the soft-start control is released to achieve good regulation and dynamic response in normal operation.

3.4 Frequency Setting and External Synchronization

The IC can provide external switching frequency setting by an external resistor R_{FREQ} and the online synchronization by external pulse signal at FREQ pin.

3.4.1 Frequency Setting

The switching frequency of the PFC converter can be set with an external resistor R_{FREQ} at FREQ pin as shown Figure 2. The pin voltage at V_{FREQ} is typical 1V. The corresponding capacitor for the oscillator is integrated in the device and the R_{FREQ}/frequency is given in Figure 4. The recommended operating frequency range is from 21kHz to 250kHz. As an example, a R_{FREQ} of 67kΩ at pin FREQ will set a switching frequency F_{SW} of 65kHz typically.



Resistance /kohm	Frequency /kHz	Resistance /kohm	Frequency /kHz
15	278	110	40
17	249	120	36
20	211	130	34
30	141	140	31.5
40	106	150	29.5
50	86	169	26.2
60	74	191	25
70	62	200	23
80	55	210	21.2
90	49	221	20.2
100	43	232	19.2

Figure 4 Frequency Versus R_{FREQ}

3.4.2 External Synchronization

The switching frequency can be synchronized to the external pulse signal after 6 external pulses delay once the voltage at the FREQ pin is higher than 2.5V. The synchronization means two points. Firstly, the PFC switching frequency is tracking the external pulse signal frequency. Secondly, the falling edge of the PFC signal is triggered by the rising edge of the external pulse signal. Figure 5 shows the blocks of frequency setting and synchronization. The external R_{SYN} combined with R_{FREQ} and the external diode D_{SYN} can ensure pin voltage to be kept between 1.0V (clamped externally) and 5V (maximum pin voltage). If the external pulse signal has disappeared longer than 108μs (typical) the switching frequency will be synchronized to internal clock set by the external resistor R_{FREQ}.

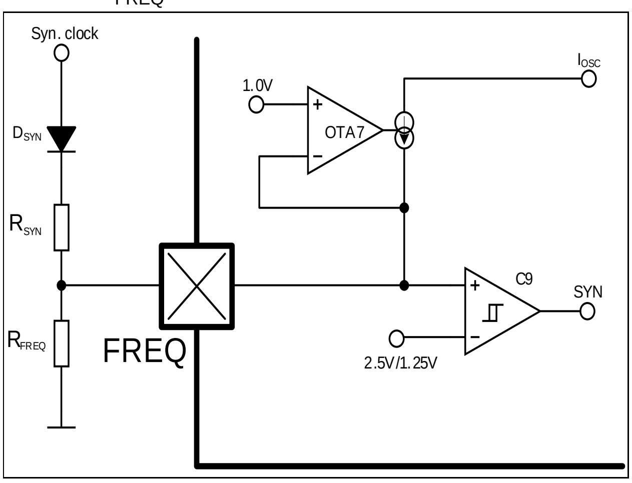


Figure 5 Frequency Setting and Synchronization

3.5 Voltage Loop

The voltage loop is the outer loop of the cascaded control scheme which controls the PFC output bus voltage V_{OUT}. This loop is closed by the feedback sensing voltage at VSENSE which is a resistive divider tapping from V_{OUT}. The pin VSENSE is the input of sigma-delta ADC which has an internal reference of 2.5V and sampling rate of 3.55kHz (typical). The voltage loop compensation is integrated digitally for better dynamic response and saving design effort. Figure 6 shows the important blocks of this voltage loop.

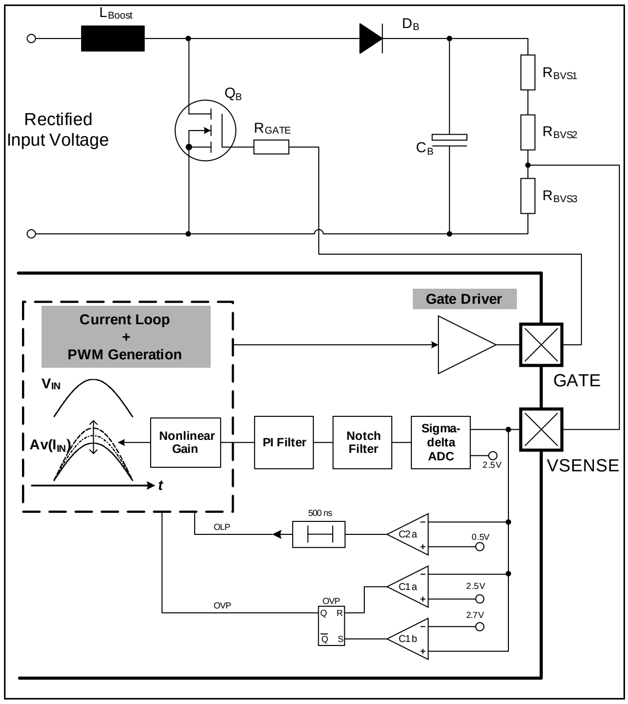


Figure 6 Voltage Loop

3.5.1 Notch Filter

In the PFC converter, an averaged current through the output diode of rectified sine waveform charges the output capacitor and results in a ripple voltage at the output capacitor with a frequency two times of the line frequency. In this digital PFC, a notch filter is used to remove the ripple of the sensed output voltage while keeping the rest of the signal almost uninfluenced. In this way, an accurate and fast output voltage regulation without influence of the output voltage ripple is achieved.

3.5.2 Voltage Loop Compensation

The Proportion-Integration (PI) compensation of the voltage loop is integrated digitally inside the IC. The digital data out of the PI compensator is converted to analog voltage for current loop control.

The nonlinear gain block controls the amplitude of the regulated inductor current. The input of this block is the output voltage of integrated PI compensator. This block has been designed to reduce the voltage loop dependency on the input voltage in order to support the wide input voltage range (85VAC-265VAC). Figure 7 gives the relative output power transfer curve versus the digital word from the integrated PI compensator. The output power at the input voltage of 85VAC and maximum digital word of 256 from PI compensator is set as the normative power and the power curves at different input voltage present the relative power to the normative one.

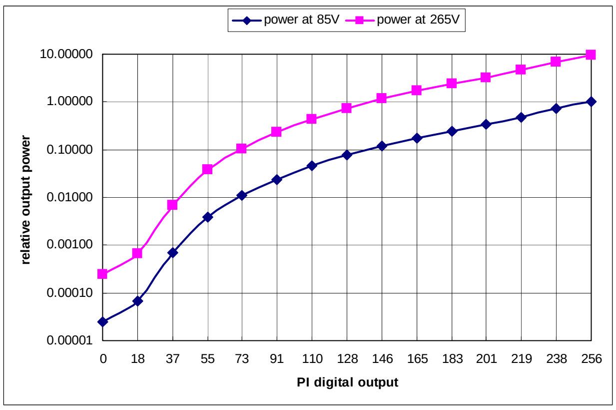


Figure 7 Power Transfer Curve

3.6 Average Current Control

The choke current is sensed through the voltage across the shunt resistor and averaged by the ICOMP pin capacitor so that the IC can control the choke current to track the instant variation of the input voltage.

3.6.1 Complete Current Loop

The complete system current loop is shown in Figure 8. It consists of the current loop block which averages the voltage at ISENSE pin resulted from the inductor current flowing across R_{shunt}. The averaged waveform is compared with an internal ramp in the ramp generator and PWM block. Once the ramp crosses the average waveform, the comparator C10 turns on the driver stage through the PWM logic block. The Nonlinear Gain block defines the amplitude of the inductor current. The following sections describe the functionality of each individual blocks.

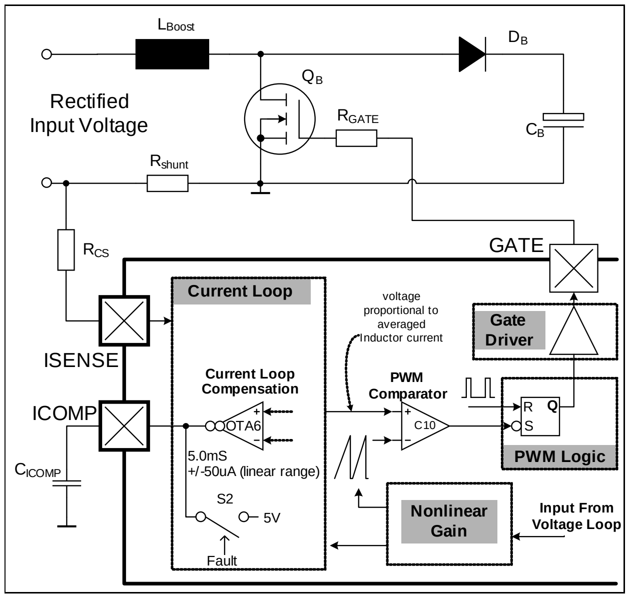


Figure 8 Complete System Current Loop

3.6.2 Current Loop Compensation

The compensation of the current loop is implemented at the ICOMP pin. This is OTA6 output and a capacitor C_{ICOMP} has to be installed at this node to ground (see Figure 8). Under normal mode of the operation, this pin gives a voltage which is proportional to the averaged inductor current. This pin is internally shorted to 5V in the event of standby mode.

3.6.3 Pulse Width Modulation (PWM)

The IC employs an average current control scheme in continuous mode (CCM) to achieve the power factor correction. Assuming the loop voltage is working and output voltage is kept constant, the off duty cycle D_{OFF} for a CCM PFC system is given as:

$$D_{OFF}=V_{IN}/V_{OUT}$$

From the above equation, D_{OFF} is proportional to V_{IN}.

The objective of the current loop is to regulate the average inductor current such that it is proportional to the off duty cycle D_{OFF}, and thus to the input voltage V_{IN}. Figure 9 shows the scheme to achieve the objective.

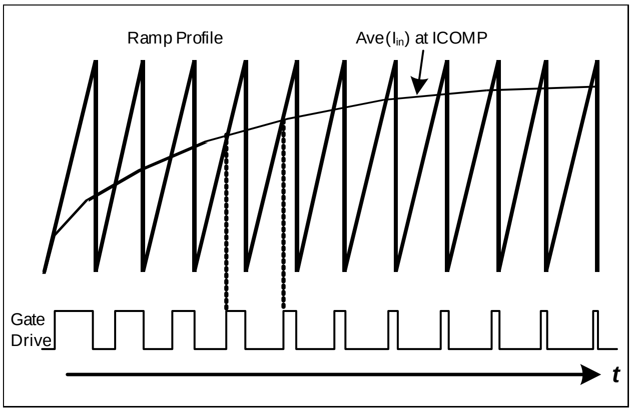


Figure 9 Average Current Control in CCM

The PWM is performed by the intersection of a ramp signal with the averaged inductor current at pin 3 (ICOMP). The PWM cycles starts with the Gate turn off for a duration of T_{OFFMIN} (600ns typ.) and the ramp is kept discharged. The ramp is allowed to rise after the T_{OFFMIN} expires. The off time of the boost transistor ends at the intersection of the ramp signal and the averaged current waveform. This results in the proportional relationship between the average current and the off duty cycle D_{OFF}.

Figure 10 shows the timing diagrams of the T_{OFFMIN} and the gate waveforms.

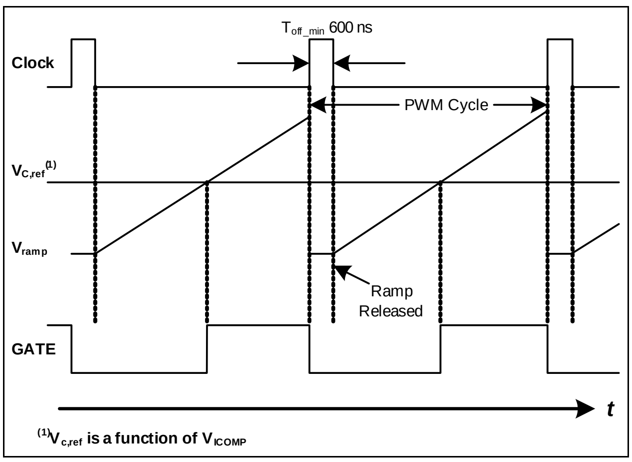


Figure 10 Ramp and PWM waveforms

3.7 PWM Logic

The PWM logic block prioritizes the control input signal and generates the final logic signal to turn on the driver stage. The speed of the logic gates in this block, together with the width of the reset pulse T_{OFFMIN}, are designed to meet a maximum duty cycle D_{MAX} of 95% at the GATE output under 65kHz of operation.

In case of high input currents which results in Peak Current Limitation, the GATE will be turned off immediately and maintained in off state for the current PWM cycle. The signal T_{OFFMIN} resets (highest priority, overriding other input signals) both the current limit latch and the PWM on latch as illustrated in Figure 11.

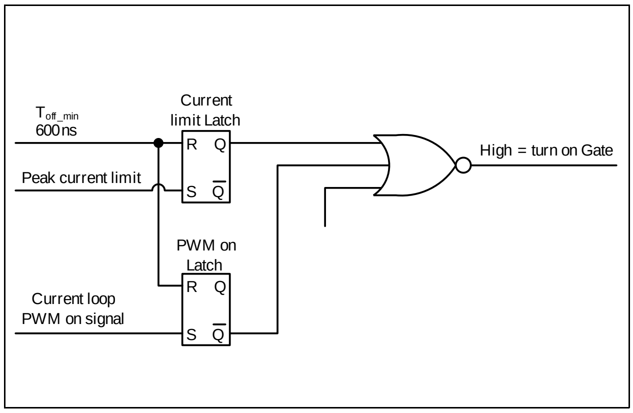


Figure 11 PWM LOGIC

3.8 System Protection

The IC provides numerous protection features in order to ensure the PFC system in safe operation.

3.8.1 Peak Current Limit (PCL)

The IC provides a cycle by cycle peak current limitation (PCL). It is active when the voltage at pin 1 (ISENSE) reaches -0.4V. This voltage is amplified by a factor of -2.5 and connected to comparator with a reference voltage of 1.0V as shown in Figure 12. A deglitcher with 200ns after the comparator improves noise immunity to the activation of this protection.

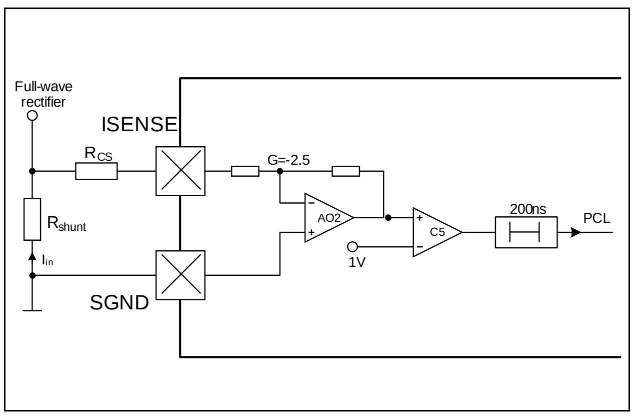


Figure 12 Peak Current Limit (PCL)

3.8.2 Open Loop Protection (OLP)

Whenever VSENSE voltage falls below 0.5V, or equivalently V_{OUT} falls below 20% of its rated value, it indicates an open loop condition (i.e. VSENSE pin not connected) or an insufficient input voltage V_{IN} for normal operation. It is implemented using comparator

C2a with a threshold of 0.5V as shown in the IC block diagram in Figure 6.

3.8.3 First Over-Voltage Protection (OVP1)

Whenever V_{OUT} exceeds the rated value by 8%, the over-voltage protection OVP1 is active as shown in Figure 6. This is implemented by sensing the voltage at VSENSE pin with respect to a reference voltage of 2.7V. A VSENSE voltage higher than 2.7V will immediately turn off the gate, thereby preventing damage to bus capacitor. After bulk voltage falls below the rated value, gate drive resumes switching again.

3.8.4 Second Over Voltage Protection (OVP2)

The second OVP is provided in case that the first one fails due to the aging or incorrect resistors connected to the VSENSE pin. This is implemented by sensing the voltage at pin OVP with respect to a reference voltage of 2.5V. When voltage at OVP pin is higher than 2.5V, the IC will immediately turn off the gate, thereby preventing damage to bus capacitor.

When the bulk voltage drops out of the hysteresis the IC will begin auto soft-start.

In normal operation the trigger level of second OVP should be designed higher than the first OVP. However in the condition of mains transient overshoot the bulk voltage may be pulled up to the peak value of mains that is higher than the threshold of OVP1 and OVP2. In this case the OVP1 and OVP2 are triggered in the same time the IC will shut down the gate drive until bulk voltage falls out of the two protection hysteresis, then resume the gate drive again.

3.9 Output Gate Driver

The output gate driver is a fast totem pole gate drive. It has an in-built cross conduction currents protection and a Zener diode Z1 (see Figure 13) to protect the external transistor switch against undesirable over voltages. The maximum voltage at pin 8 (GATE) is typically clamped at 15V.

The output is active HIGH and at VCC voltages below the under voltage lockout threshold V_{CCUVLO}, the gate drive is internally pull low to maintain the off state.

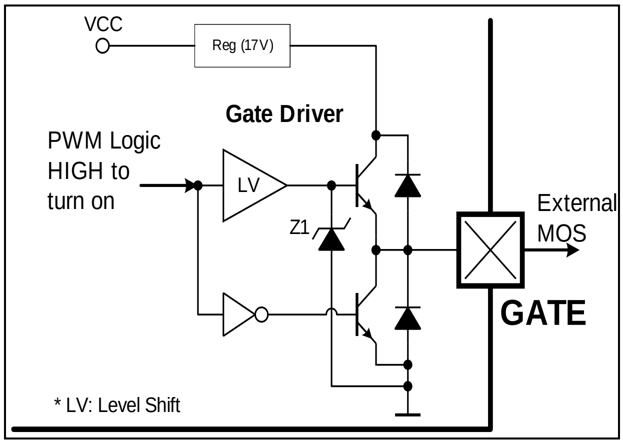


Figure 13 Gate Driver

3.10 Protection Function

Description of Fault	Fault-Type	Min. Duration of Effect	Consequence
Voltage at Pin ISENSE < -400mV	PCL	200 ns	Gate Driver is turned off immediately during current switching cycle
Voltage at Pin VSENSE < 0.5V	OLP	1 µs	Power down. Soft-restart after VSENSE voltage > 0.5V
Voltage at Pin VSENSE > 108% of rated level	OVP1	12 µs	Gate Driver is turned off until VSENSE voltage < 2.5V.
Voltage at Pin OVP > 2.5V and Voltage at Pin VSENSE > 108% of rated level	OVP1 and OVP2	12 µs	Gate Driver is turned off until bulk voltage drops out of both OVP hysteresis
Voltage at Pin OVP > 2.5V	OVP2 (auto-restart mode)	12 µs	Gate Driver is turned off. Soft-restart after OVP voltage < 2.3V

4 Electrical Characteristics

All voltages are measured with respect to ground (pin 2). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Supply Voltage	V_{VCC}	-0.3		26	V	
GATE Voltage	V_{GATE}	-0.3		17	V	Clamped at 15V if driven internally.
ISENSE Voltage	V_{ISENSE}	-20		5.3	V	1)
ISENSE Current	I_{ISENSE}	-1		1	mA	
VSENSE Voltage	V_{VSENSE}	-0.3		5.3	V	
VSENSE Current	I_{VSENSE}	-1		1	mA	
ICOMP Voltage	V_{ICOMP}	-0.3		5.3	V	
FREQ Voltage	V_{FREQ}	-0.3		5.3	V	
OVP Voltage	V_{OVP}	-0.3		5.3	V	
Junction Temperature	T_J	-40		150	°C	
Storage Temperature	$T_{A,STO}$	-55		150	°C	
Thermal Resistance	R_{THJA}			185	K/W	Junction to Air
Soldering Temperature	T_{SLD}			260	°C	Wave Soldering 2)
ESD Capability	V_{ESD}			2	kV	Human Body Model 3)

1) Absolute ISENSE current should not be exceeded
2) According to JESD22A111
3) According to EIA/JESD22-A114-B (discharging an 100 pF capacitor through an 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VCC Supply Voltage @ 25°C	V_{VCC}	$V_{VCC,OFF}$		25	V	T_J=25°C
Junction Temperature	T_J	-25		125	°C	
PFC switching frequency	F_{PFC}	21		250	kHz	

4.3 Characteristics

Note: The electrical Characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -25 °C to 125 °C. Typical values represent the median values, which are related to 25 °C. If not otherwise stated, a supply voltage of V_{VCC} = 18V, a typical switching frequency of f_{freq}=65kHz are assumed and the IC operates in active mode. Furthermore, all voltages are referring to GND if not otherwise mentioned.

4.3.1 Supply Section

Parameter	Symbol	Limit Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VCC Turn-On Threshold	V_{CCon}	11.5	12	12.9	V	
VCC Turn-Off Threshold/ Under Voltage Lock Out	V_{CCUVLO}	10.5	11.0	11.9	V	
VCC Turn-On/Off Hysteresis	V_{CChy}	0.7	1	1.45	V	
Start Up Current Before V_{CCon}	$I_{CCstart1}$	-	380	680	µA	V_{CCon}-1.2V
Start Up Current Before V_{CCon}	$I_{CCstart2}$	-	1.4	2.4	mA	V_{CCon}-0.2V
Operating Current with active GATE	I_{CCHG}	-	6.4	8.5	mA	C_L= 1nF
Operating Current during Standby	$I_{CCStdby}$	-	3.5	4.7	mA	V_{VSENSE}= 0.4V V_{ICOMP}= 4V

4.3.2 Variable Frequency Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Switching Frequency (Typical)	F_{SWnom}	62.5	65	67.5	kHz	R5 = 67kΩ
Switching Frequency (Min.)	F_{SWmin}	-	21	-	kHz	R5 = 212kΩ
Switching Frequency (Max.)	F_{SWmax}	-	250	-	kHz	R5 = 17kΩ
Voltage at FREQ pin	V_{FREQ}	-	1	-	V	
Max. Duty Cycle	*Dmax*	93	95	98.5	%	f_{SW}=f_{SWnom} (R_{FREQ}=67kΩ)

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Min. Duty Cycle	D_{MIN}			0	%	V_{VSENSE}= 2.5V V_{ICOMP}= 4.3V
Min. Off Time	T_{OFFMIN}	310	600	920	ns	V_{VSENSE}= 2.5V V_{ISENSE}= 0V (R5 = 67kΩ)

4.3.4 External Synchronization

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Detection threshold of external clock	V_{thr_EXT}		2.5		V	
Synchronization range	f_{EXT_range}	50		150	kHz	
Synchronization frequency ratio	f_{EXT}:f_{PFC}		1:1			
propagation delay from rising edge of external clock to falling edge of PFC gate drive	$T_{EXT2GATE}$			500	ns	f_{EXT}=65kHz
Allowable external duty on time	T_{D_on}	10		70	%	

4.3.5 System Protection Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Over Voltage Protection (OVP1) Low to High	V_{OVP1_L2H}	2.65	2.7	2.77	V	108%$V_{BULKRated}$
Over Voltage Protection (OVP1) High to Low	V_{OVP1_H2L}	2.45	2.5	2.55	V	
Over Voltage Protection (OVP1) Hysteresis	V_{OVP1_HYS}	150	200	270	mV	
Blanking time for OVP1	T_{OVP1}		12		µs	
Over Voltage Protection (OVP2) Low to High	V_{OVP2_L2H}	2.45	2.5	2.55	V	
Over Voltage Protection (OVP2) High to Low	I_{OVP2_H2L}	2.25	2.3	2.35	V	
Blanking time for OVP2	T_{OVP2}		12		µs	
OVP2 mode detection threshold	V_{OVP2_mode}		0.5		V	comparator at VBTHL pin
Current source for OVP2 mode detection[1)]	I_{OVP2_mode}	4	5	6	µA	current source at VBTHL pin
Peak Current Limitation (PCL) ISENSE Threshold	V_{PCL}	-365	-400	-435	mV	
Blanking time for PCL turn_on	T_{PCLon}		200		ns	

1) The parameter is not subject to production test - verified by design/characterization

4.3.6 Current Loop Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
OTA6 Transconductance Gain	Gm_{OTA6}	3.5	5.0	6.35	mS	At Temp = 25°C
OTA6 Output Linear Range[1)]	I_{OTA6}		± 50		µA	
ICOMP Voltage during OLP	V_{ICOMPF}	4.8	5.0	5.2	V	V_{VSENSE}= 0.4V

1) The parameter is not subject to production test - verified by design/characterization

4.3.7 Voltage Loop Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trimmed Reference Voltage	V_{VSREF}	2.47	2.5	2.53	V	±1.2%
Open Loop Protection (OLP) VSENSE Threshold	V_{VS_OLP}	0.45	0.5	0.55	V	
VSENSE Input Bias Current	I_{VSENSE}	-1	-	1	µA	V_{VSENSE}= 2.5V

4.3.8 Driver Section

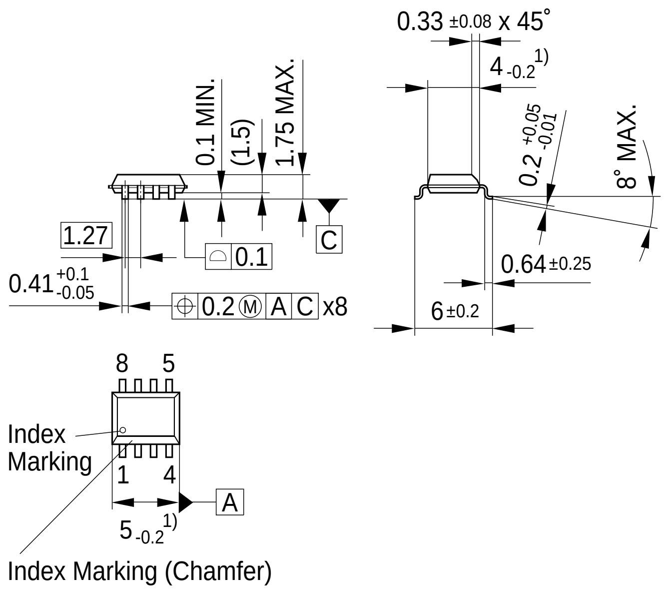
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GATE Low Voltage	V_{GATEL}	-	-	1.2	V	V_{CC} =10V I_{GATE} = 5 mA
		-	0.4	-	V	I_{GATE} = 0 A
		-	-	1.4	V	I_{GATE} = 20 mA
		-0.2	0.8	-	V	I_{GATE} = -20 mA
GATE High Voltage	V_{GATEH}	-	15	-	V	V_{CC} = 25V C_L = 1nF
		-	12.4	-	V	V_{CC} = 15V C_L = 1nF
		8.0	-	-	V	$V_{CC} = V_{VCCoff}$ + 0.2V C_L = 1nF

4.3.9 Gate Drive Section

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GATE Rise Time	t_r	-	30	-	ns	V_{Gate} = 20% - 80% V_{GATEH} C_L = 1nF
GATE Fall Time	t_f	-	25	-	ns	V_{Gate} = 80% - 20% V_{GATEH} C_L = 1nF

5 Outline Dimension

PG-DSO-8 Outline Dimension



1) Does not include plastic or metal protrusion of 0.15 max. per side

Notes:

1. *You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": **http://www.infineon.com/products**.*
2. *Dimensions in mm.*

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an allencompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

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