

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ Power-Transistor, 60 V
IPA040N06N

Data Sheet

Rev. 2.1
Final

1 Description

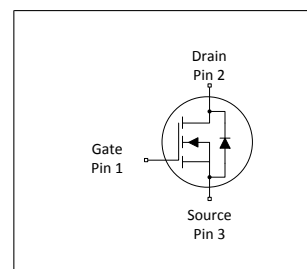
Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	4.0	mΩ
I_D	69	A
Q_{OSS}	44	nC
$Q_G(0V..10V)$	38	nC



Type / Ordering Code	Package	Marking	Related Links
IPA040N06N	PG-TO220-FP	040N06N	-

¹⁾ J-STD20 and JESD22

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2 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	69 48	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$
Pulsed drain current ¹⁾	$I_{D,pulse}$	-	-	276	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ²⁾	E_{AS}	-	-	77	mJ	$I_D=69\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	36	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	3.1	4.2	K/W	-

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=50\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.6 4.7	4.0 5.0	m Ω	$V_{GS}=10\text{ V}$, $I_D=69\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=18\text{ A}$
Gate resistance ³⁾	R_G	-	1.3	1.95	Ω	-
Transconductance	g_{fs}	55	110	-	S	$ V_{DS} > 2 I_D /R_{DS(on)max}$, $I_D=69\text{ A}$

¹⁾ See figure 3 for more detailed information

²⁾ See figure 13 for more detailed information

³⁾ Defined by design. Not subject to production test

Table 5 Dynamic characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2700	3375	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	670	838	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	28	56	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=69\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r	-	16	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=69\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=69\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Fall time	t_f	-	8	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=69\text{ A}$, $R_{G,ext}=3\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	13	-	nC	$V_{DD}=30\text{ V}$, $I_D=69\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	8	-	nC	$V_{DD}=30\text{ V}$, $I_D=69\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	7	9	nC	$V_{DD}=30\text{ V}$, $I_D=69\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	13	-	nC	$V_{DD}=30\text{ V}$, $I_D=69\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	38	44	nC	$V_{DD}=30\text{ V}$, $I_D=69\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.8	-	V	$V_{DD}=30\text{ V}$, $I_D=69\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	33	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	44	55	nC	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$

Table 7 Reverse diode

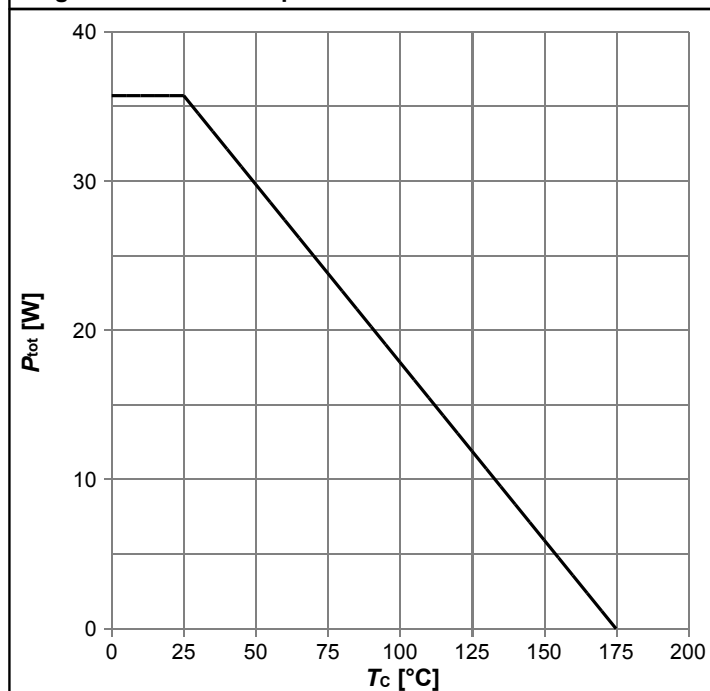
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	$T_C=25\text{ }^\circ\text{C}$
Diode pulse current	$I_{S,pulse}$	-	-	276	A	$T_C=25\text{ }^\circ\text{C}$
Diode forward voltage	V_{SD}	-	0.88	1.2	V	$V_{GS}=0\text{ V}$, $I_F=30\text{ A}$, $T_J=25\text{ }^\circ\text{C}$
Reverse recovery time ¹⁾	t_{rr}	-	33	53	ns	$V_R=30\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	28	-	nC	$V_R=30\text{ V}$, $I_F=30\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test

²⁾ See "Gate charge waveforms" for parameter definition

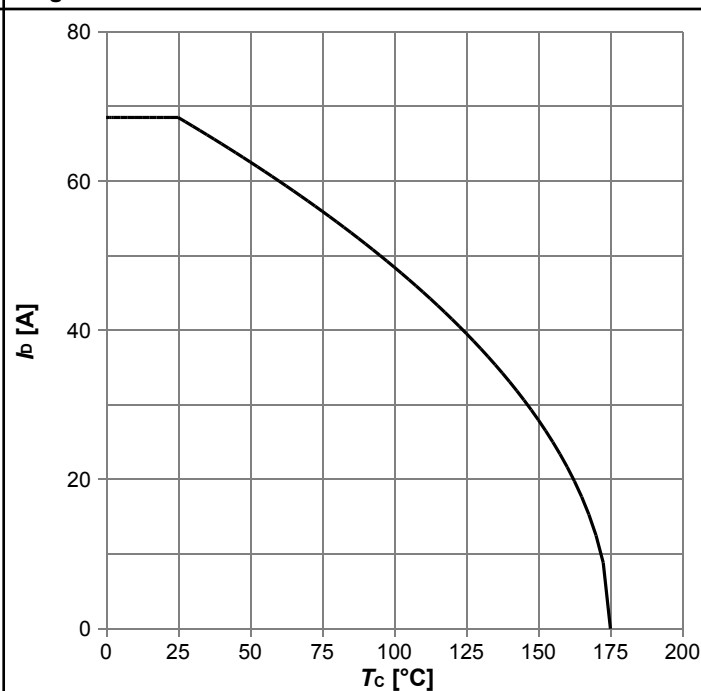
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



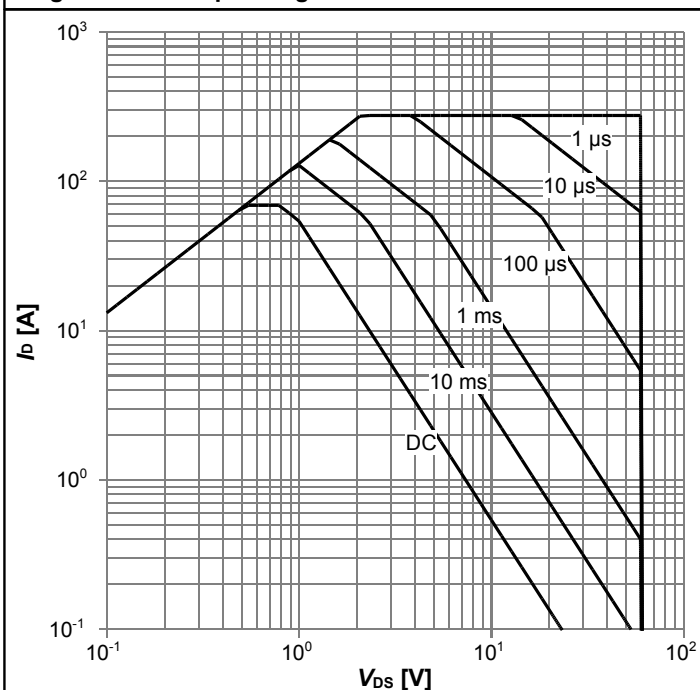
$$P_{tot}=f(T_c)$$

Diagram 2: Drain current



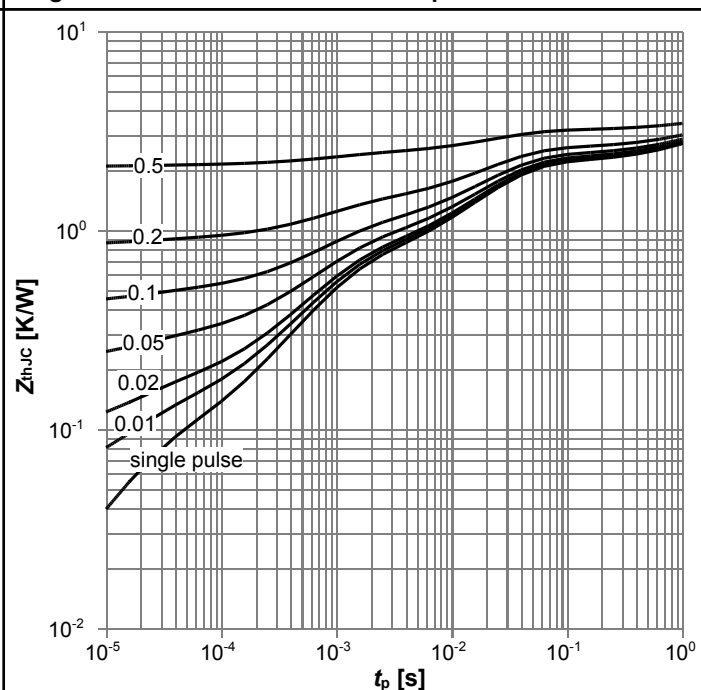
$$I_D=f(T_c); V_{GS} \geq 10 \text{ V}$$

Diagram 3: Safe operating area



$$I_D=f(V_{DS}); T_c=25^\circ\text{C}; D=0; \text{parameter: } t_p$$

Diagram 4: Max. transient thermal impedance



$$Z_{thJC}=f(t_p); \text{parameter: } D=t_p/T$$

Diagram 5: Typ. output characteristics

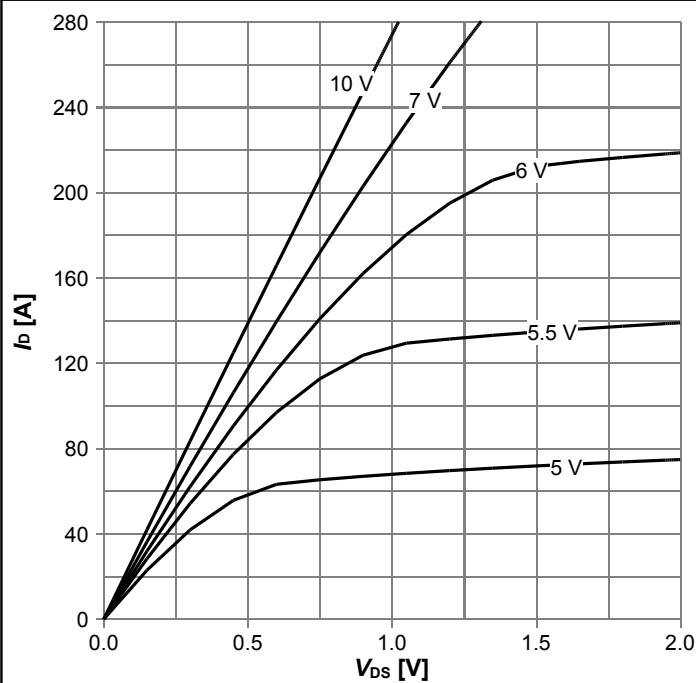

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance

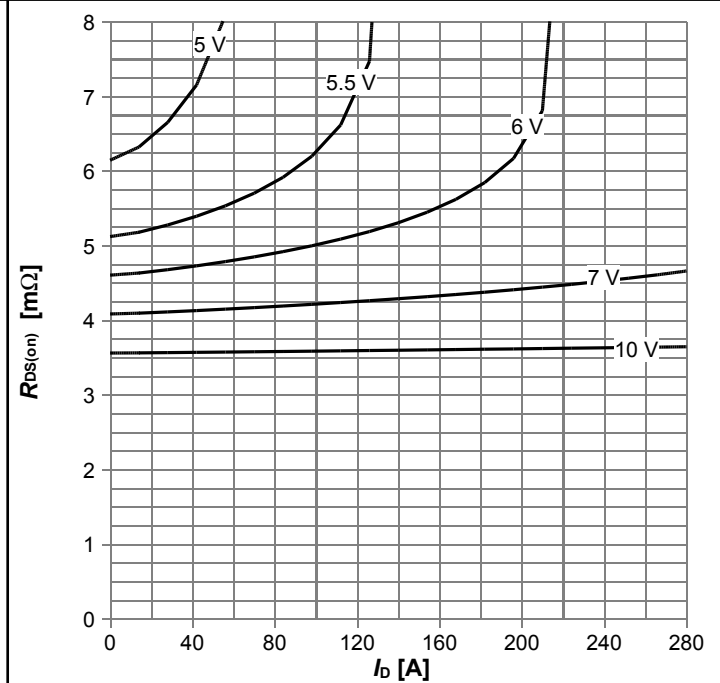

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics

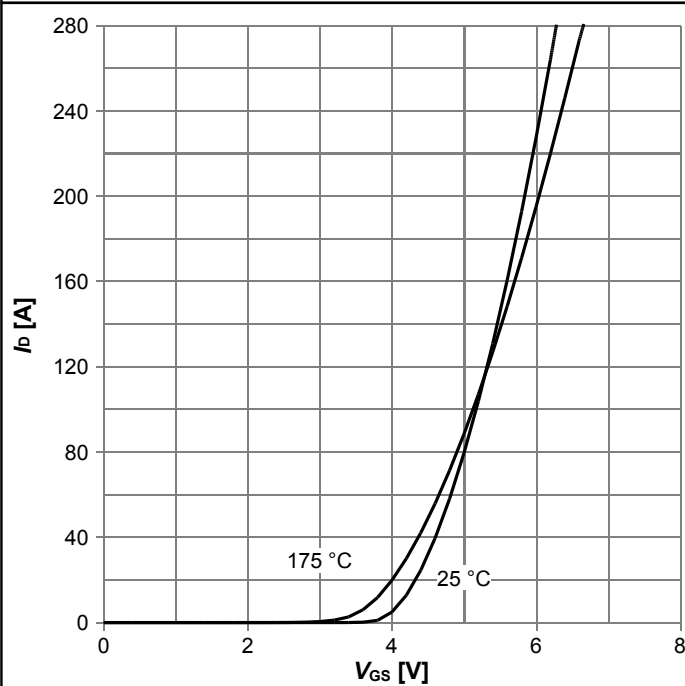

 $I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance

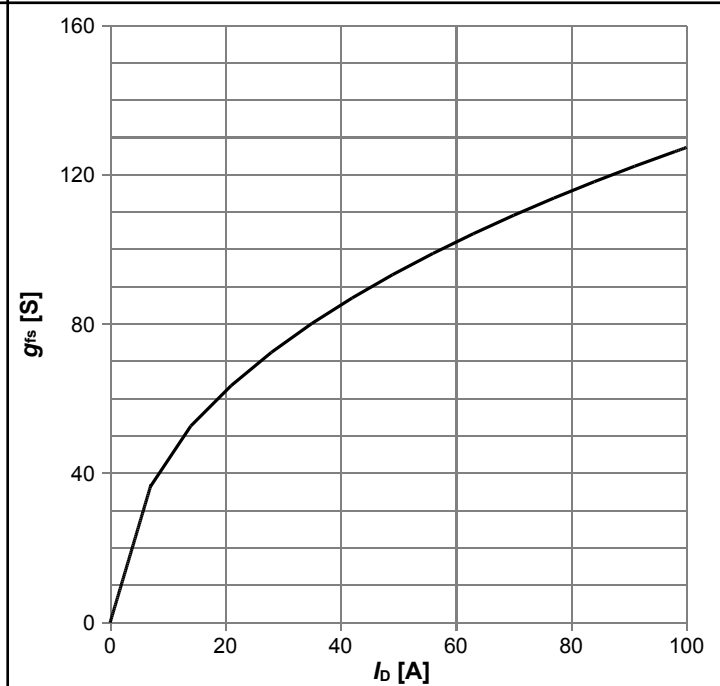
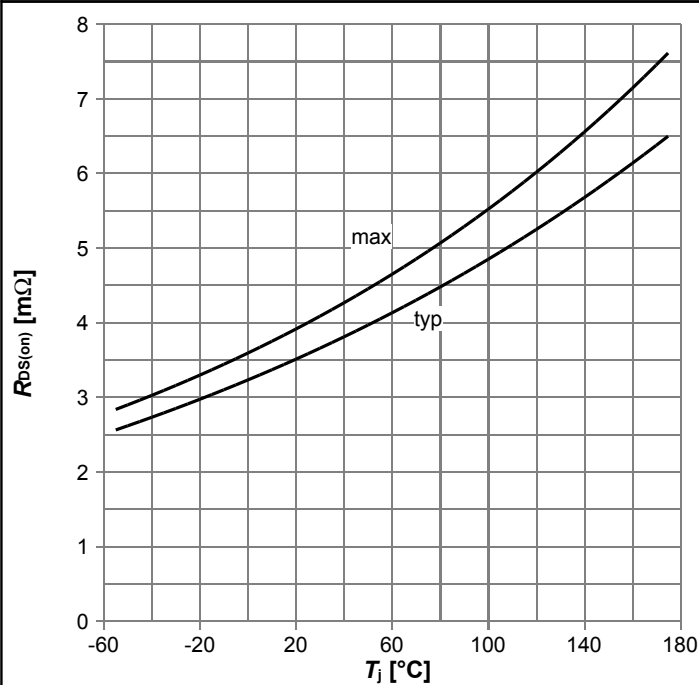
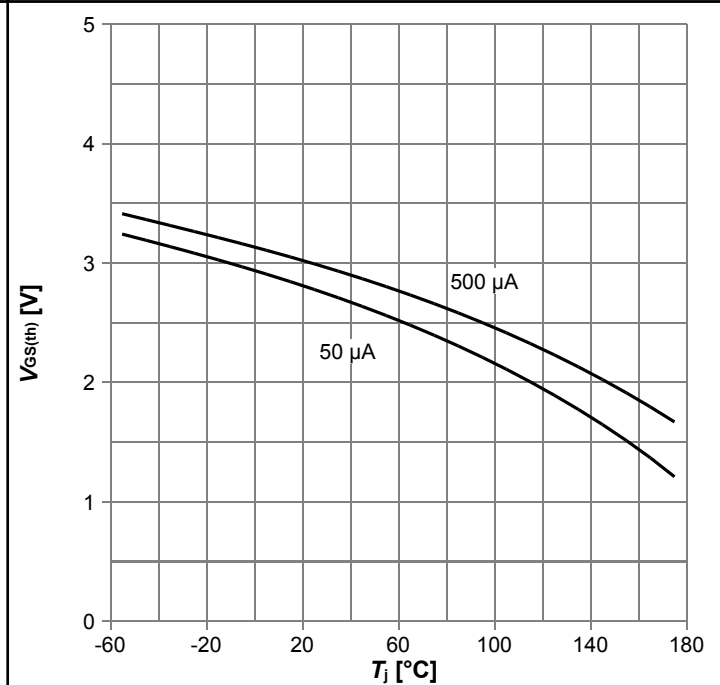

 $g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



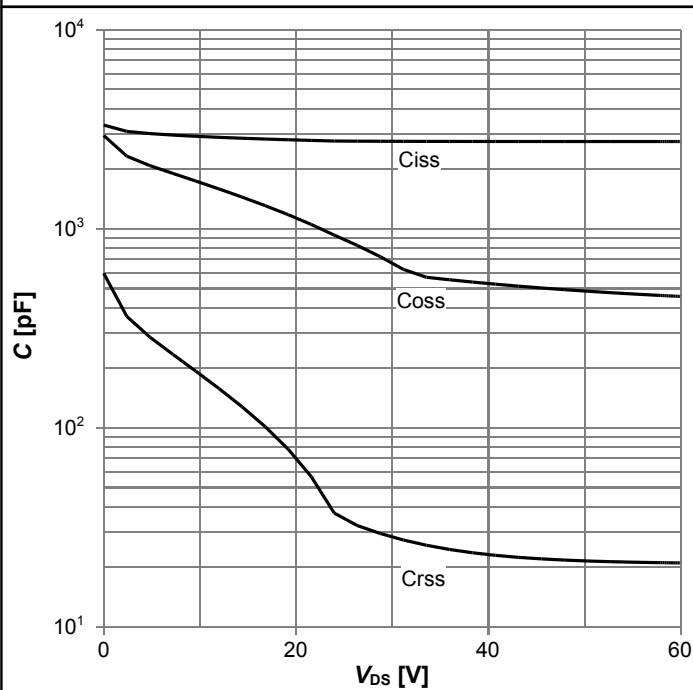
$$R_{DS(on)} = f(T_j); I_D = 69 \text{ A}; V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



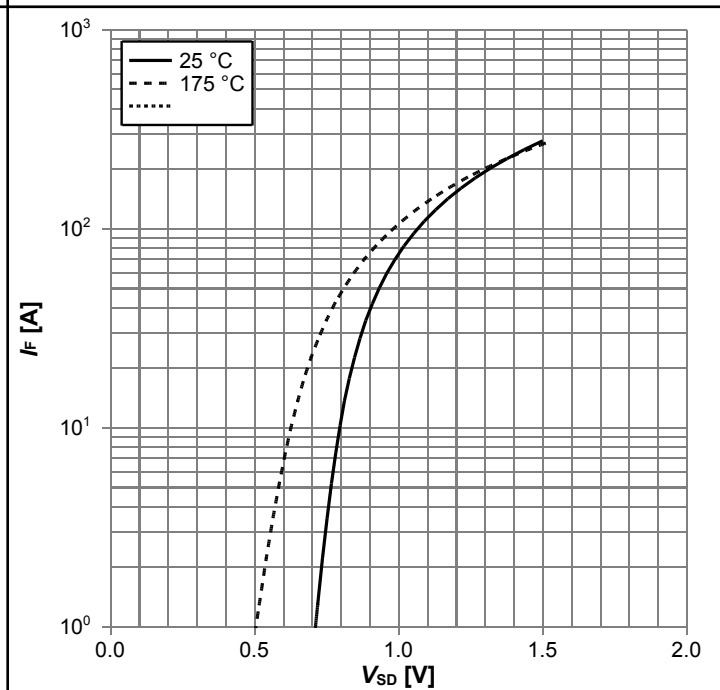
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

Diagram 11: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



$$I_F = f(V_{SD}); \text{parameter: } T_j$$

Diagram 13: Avalanche characteristics

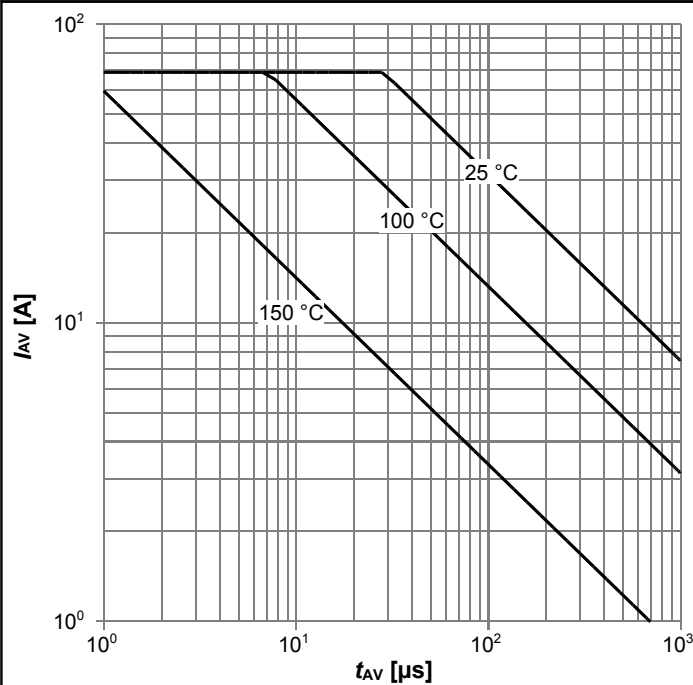

 $I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega; \text{parameter: } T_{j(\text{start})}$

Diagram 14: Typ. gate charge

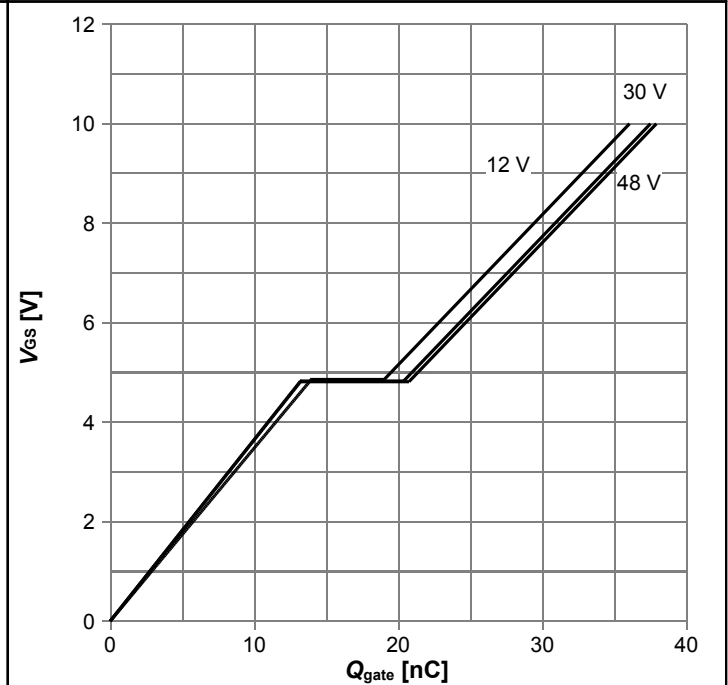
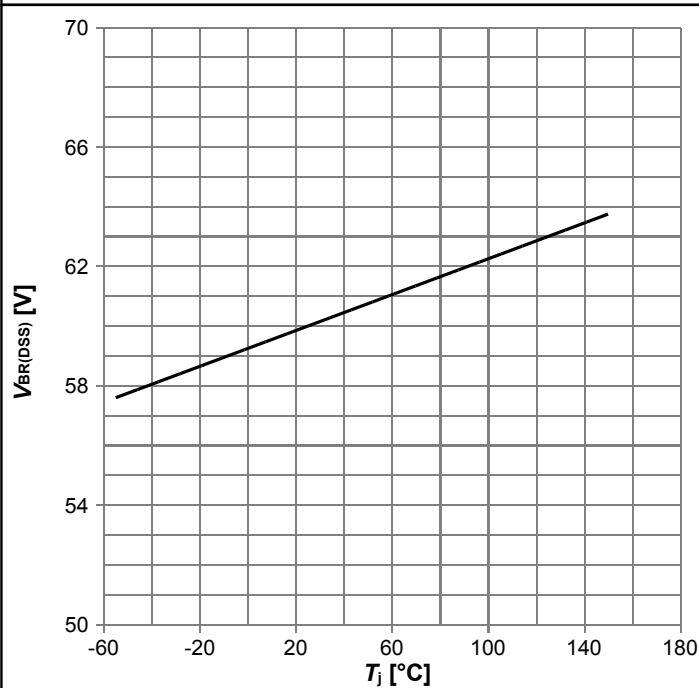
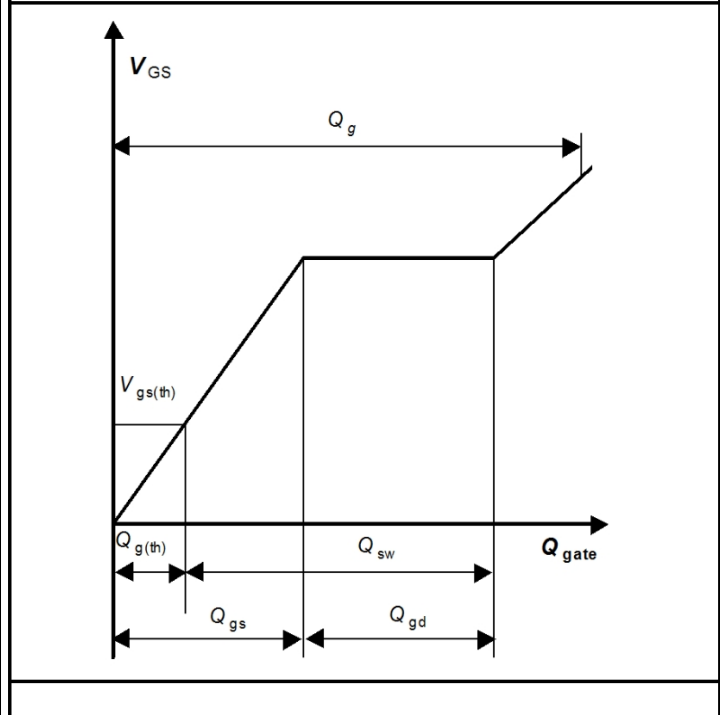

 $V_{GS}=f(Q_{\text{gate}}); I_D=69\ \text{A pulsed}; \text{parameter: } V_{DD}$

Diagram 15: Drain-source breakdown voltage


 $V_{BR(DSS)}=f(T_J); I_D=1\ \text{mA}$

Gate charge waveforms



Revision History

IPA040N06N

Revision: 2014-06-19, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.1	2014-06-19	Rev.2.1

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