MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ Power-Transistor, 300 V
IPB407N30N

Data Sheet

Rev. 2.0
Final

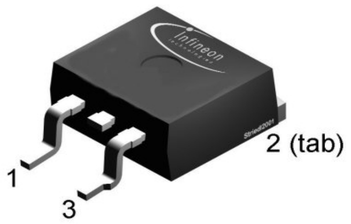
Power Management & Multimarket

1 Description

Features

- N-channel, normal level
- Fast Diode with reduced Q_{rr}
- Optimized for hard commutation ruggedness
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Halogen-free according to IEC61249-2-21

D²PAK



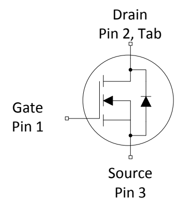


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	300	V
$R_{DS(on),max}$	40.7	mΩ
I_D	44	A

Type / Ordering Code	Package	Marking	Related Links
IPB407N30N	PG-TO 263-3	407N30N	-

[1] J-STD20 and JESD22

Table of Contents

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- -	- -	44 34	A	T_C=25 °C T_C=100 °C
Pulsed drain current[1]	$I_{D,pulse}$	-	-	176	A	T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	240	mJ	I_D=22 A, R_{GS}=50 Ω
Reverse diode peak dv/dt	dv/dt	-	-	60	kV/µs	I_D=44 A, V_{DS}=150 V, di/dt=1000 A/µs, $T_{j,max}$=175 °C
Gate source voltage	V_{GS}	-20	-	20	V	-
Diode hard commutation destructive current[2]	P_{tot}	-	-	300	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case[3]	R_{thJC}	-	0.3	0.5	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area[4]	R_{thJA}	-	-	40	K/W	-

[1] See figure 3
[2] Diode pulse current is defined by thermal and/or package limits
[3] Defined by design. Not subject to production test.
[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	300	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS}, I_D=270 µA
Zero gate voltage drain current	I_{DSS}	- -	1 10	10 300	µA	V_{DS}=240 V, V_{GS}=0 V, T_j=25 °C V_{DS}=240 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	1	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	36	40.7	mΩ	V_{GS}=10 V, I_D=44 A
Gate resistance[1]	R_G	-	2.4	3.6	Ω	-
Transconductance	g_{fs}	52	103	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=44 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1]	C_{iss}	-	5400	7180	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Output capacitance[1]	C_{oss}	-	281	374	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Reverse transfer capacitance[1]	C_{rss}	-	6	13	pF	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=22 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	9	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=22 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	43	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=22 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	9	-	ns	V_{DD}=100 V, V_{GS}=10 V, I_D=22 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24	-	nC	V_{DD}=100 V, I_D=44 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	7	-	nC	V_{DD}=100 V, I_D=44 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	15	-	nC	V_{DD}=100 V, I_D=44 A, V_{GS}=0 to 10 V
Gate charge total[1]	Q_g	-	65	87	nC	V_{DD}=100 V, I_D=44 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	V_{DD}=100 V, I_D=44 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	131	-	nC	V_{DD}=100 V, V_{GS}=0 V

[1] Defined by design. Not subject to production test.
[2] See "Gate charge waveforms" for parameter definition

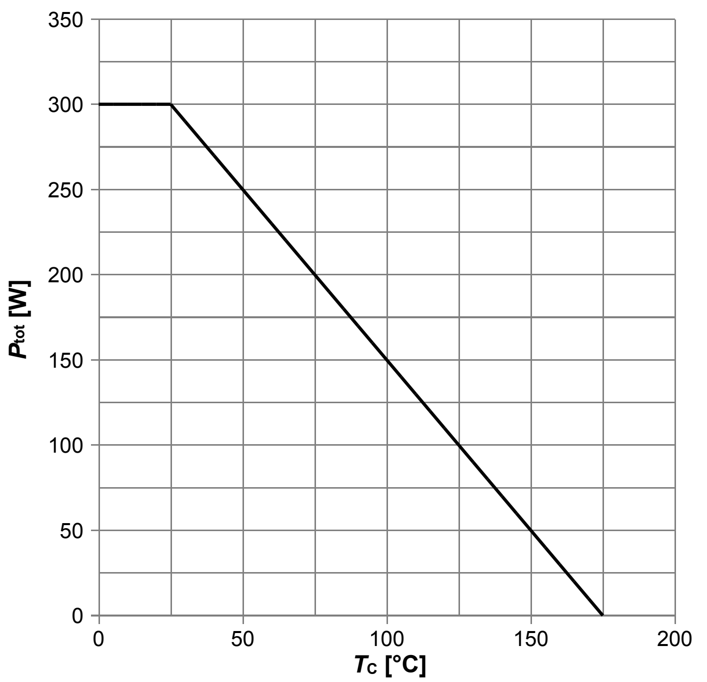
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continous forward current	I_S	-	-	44	A	T_C=25 °C
Diode pulse current[1)]	$I_{S,pulse}$	-	-	176	A	T_C=25 °C
Diode hard commutation current[2)]	$I_{S,hard}$	-	-	44	A	T_C=25 °C, di_F/dt=1000 A/µs
Diode forward voltage	V_{SD}	-	0.9	1.2	V	V_{GS}=0 V, I_F=44 A, T_j=25 °C
Reverse recovery time[3)]	t_{rr}	-	152	304	ns	V_R=100 V, I_F=32.2A, di_F/dt=100 A/µs
Reverse recovery charge[3)]	Q_{rr}	-	844	1689	nC	V_R=100 V, I_F=32.2A, di_F/dt=100 A/µs

1) Diode pulse current is defined by thermal and/or package limits
2) Maximum allowed hard-commutated current through diode at di/dt=1000 A/µs
3) Defined by design. Not subject to production test.

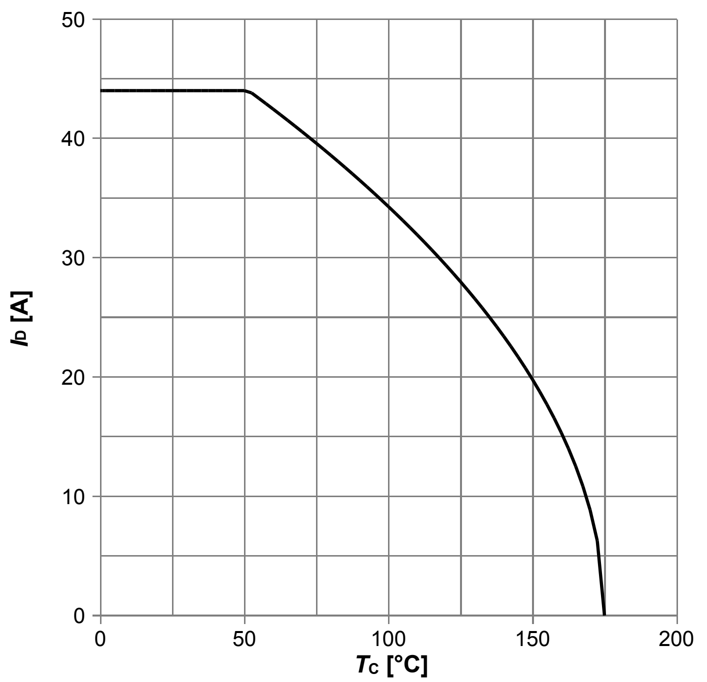
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



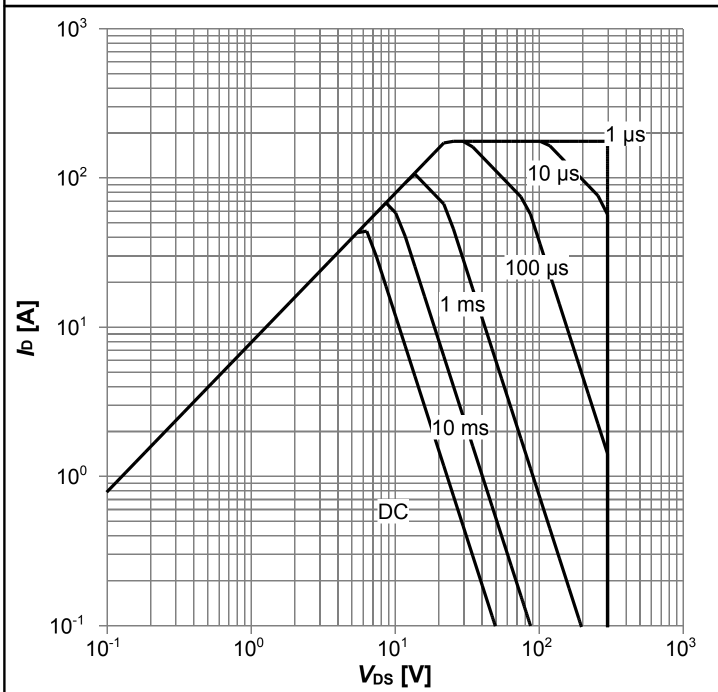
P_{tot}=f(T_C)

Diagram 2: Drain current



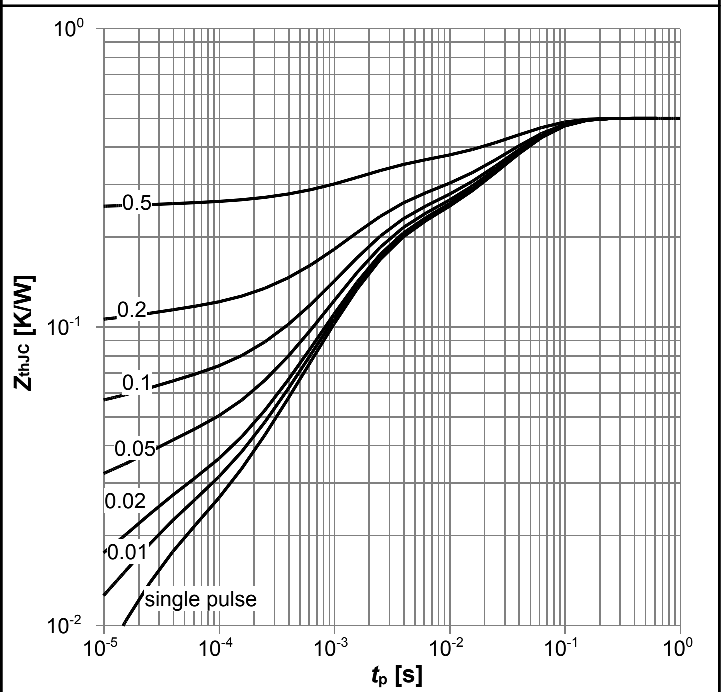
I_D=f(T_C); V_{GS}>=10 V

Diagram 3: Safe operating area



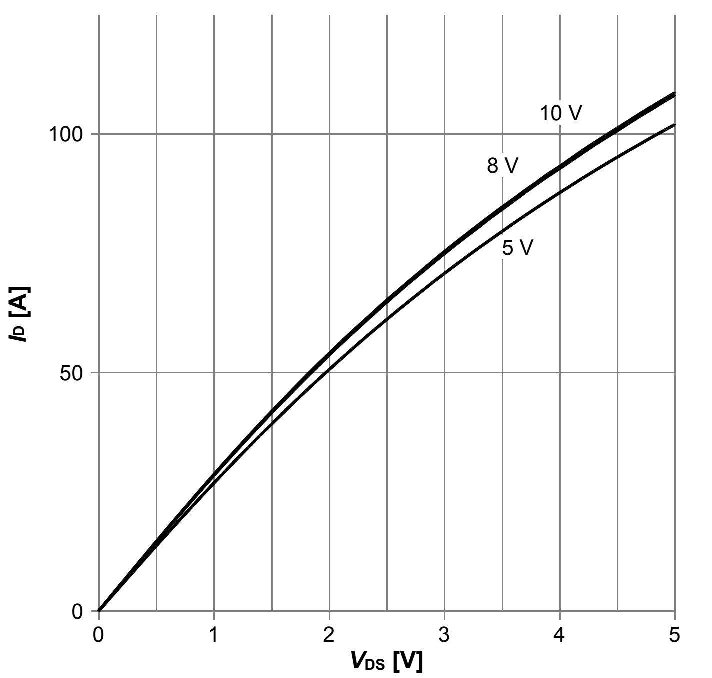
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



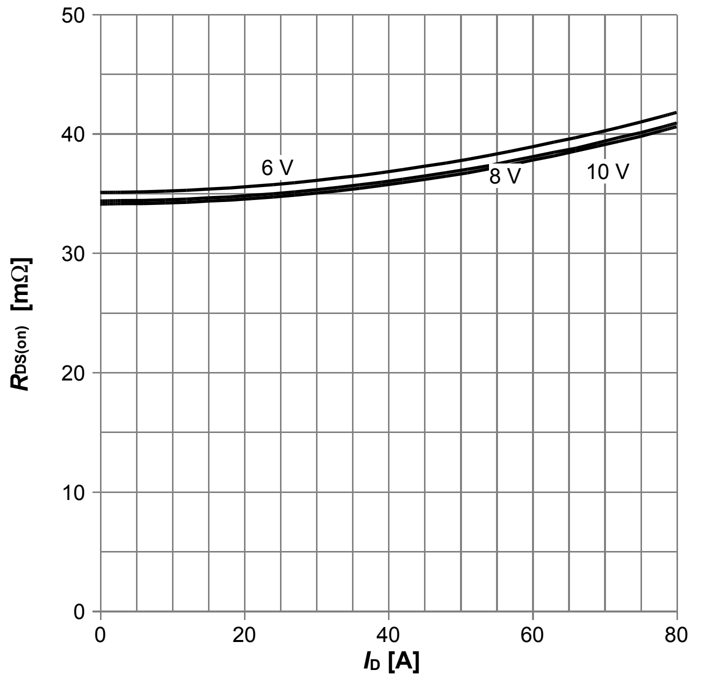
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



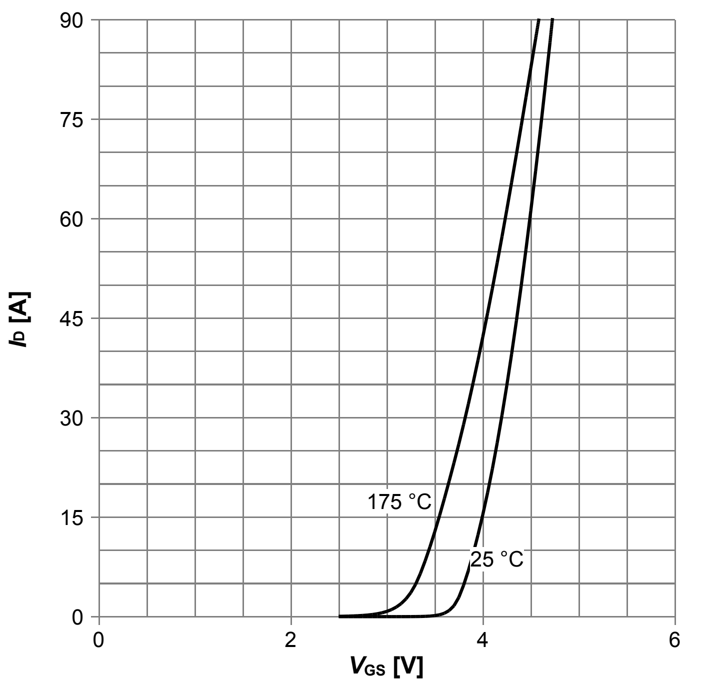
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



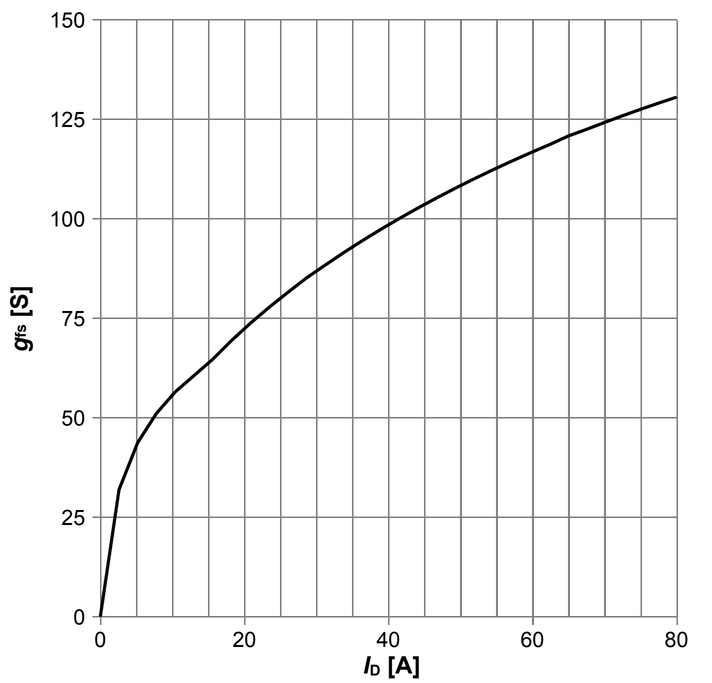
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



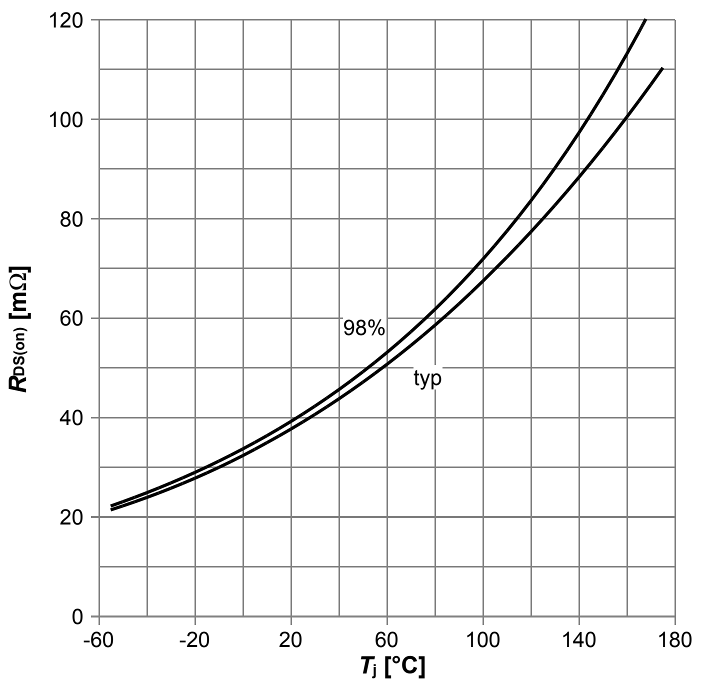
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



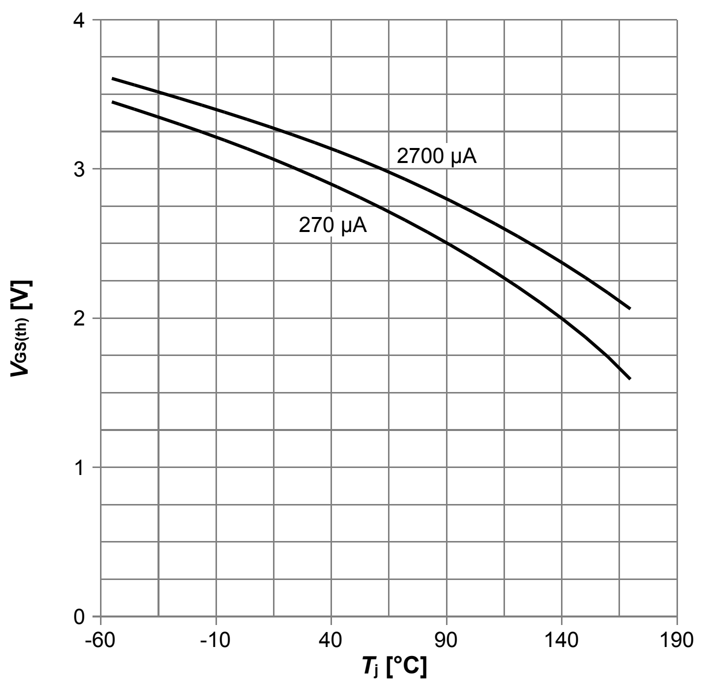
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



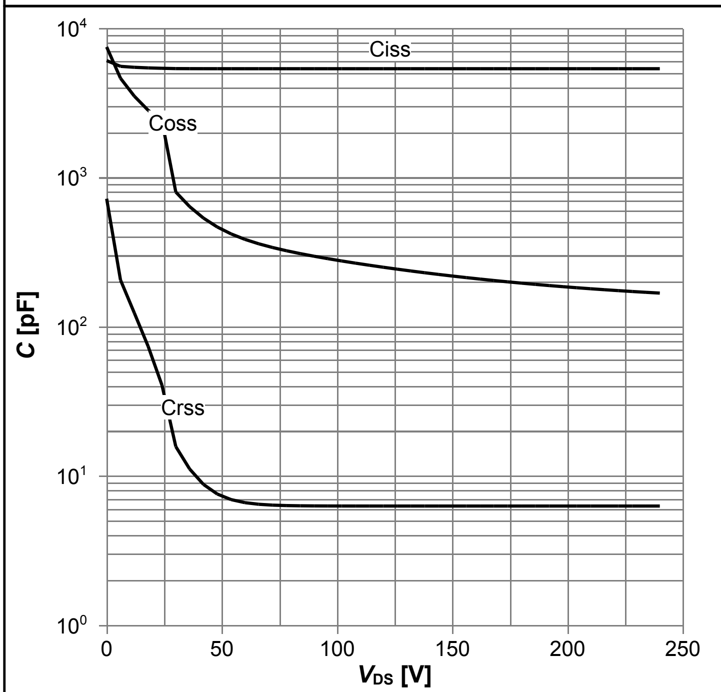
$R_{DS(on)}$=f(T_j); I_D=44 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



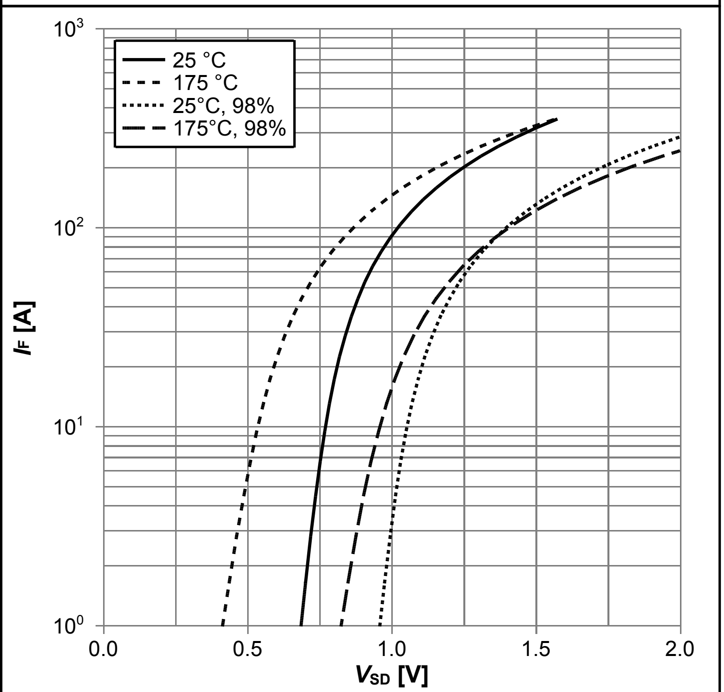
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



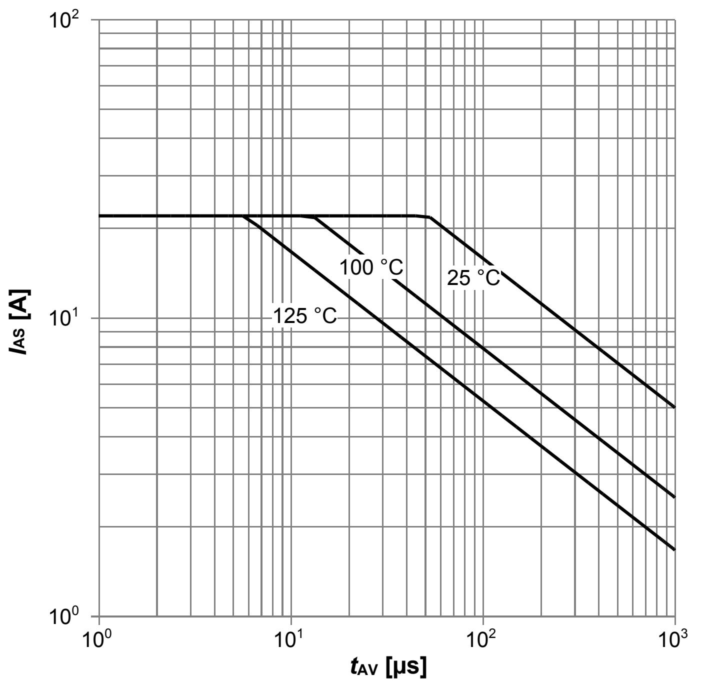
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



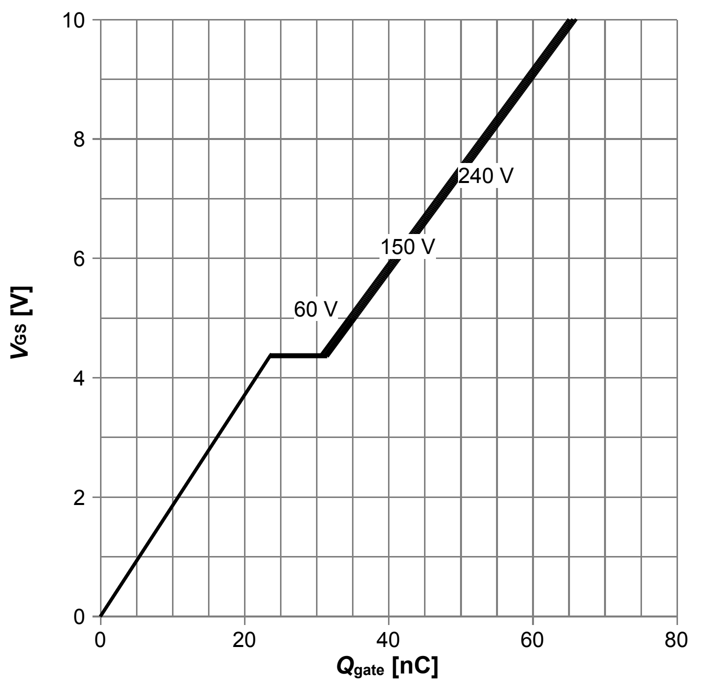
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



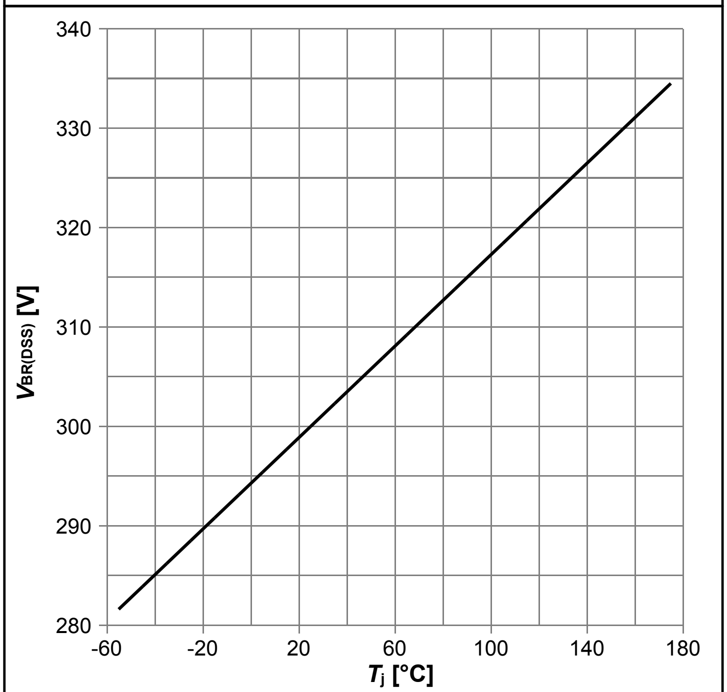
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



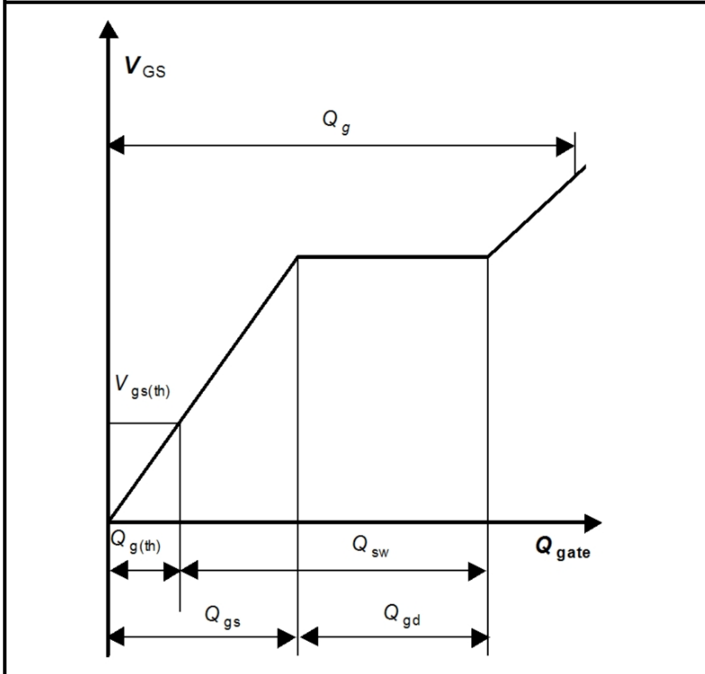
V_{GS}=f(Q_{gate}); I_D=44 A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

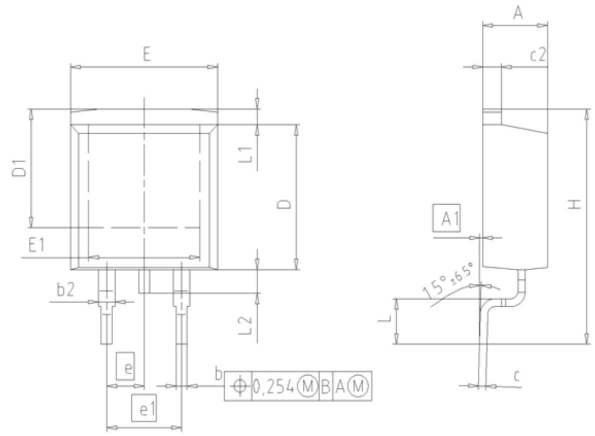


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

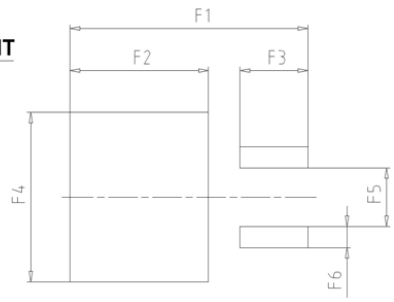
Gate charge waveforms



6 Package Outlines



FOOTPRINT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO.
Z8B00003324

SCALE
0 5 0 5
7.5mm

EUROPEAN PROJECTION

ISSUE DATE
30-08-2007

REVISION
01

Figure 1 Outline PG-TO 263-3, dimensions in mm/inches

Revision History

IPB407N30N

Revision: 2014-12-27, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-27	Release of final version

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