

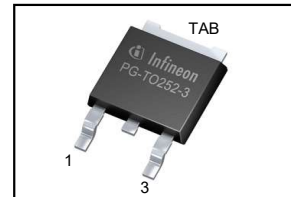
OptiMOS™-T2 Power-Transistor

Product Summary

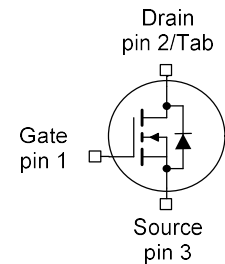
V_{DS}	100	V
$R_{DS(on),max}$	6.7	mΩ
I_D	90	A

Features

- N-channel - Normal Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested

PG-TO252-3-313


Type	Package	Marking
IPD90N10S4-06	PG-TO252-3-313	4N1006


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{V}$	90	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{V}^{2)}$	72	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	360	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=45\text{A}$	250	mJ
Avalanche current, single pulse	I_{AS}	-	70	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	136	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.1	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=90\mu A$	2.0	2.7	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	0.01	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=90A$	-	5.9	6.7	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	3740	4870	pF
Output capacitance	C_{oss}		-	1190	1550	
Reverse transfer capacitance	C_{rss}		-	75	150	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{V}, V_{GS}=10\text{V},$ $I_D=90\text{A}, R_G=3.5\Omega$	-	10	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	25	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=80\text{V}, I_D=90\text{A},$ $V_{GS}=0\text{ to }10\text{V}$	-	18	23	nC
Gate to drain charge	Q_{gd}		-	10	20	
Gate charge total	Q_g		-	52	68	
Gate plateau voltage	$V_{plateau}$		-	4.9	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ\text{C}$	-	-	90	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{V}, I_F=90\text{A},$ $T_J=25^\circ\text{C}$	-	1.0	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50\text{V}, I_F=50\text{A},$ $di_F/dt=100\text{A}/\mu\text{s}$	-	65	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	130	-	

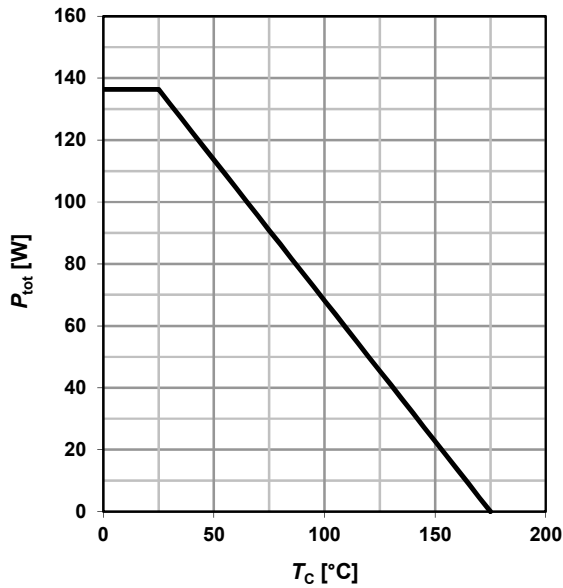
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 1.1\text{K/W}$ the chip is able to carry 101A at 25°C.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

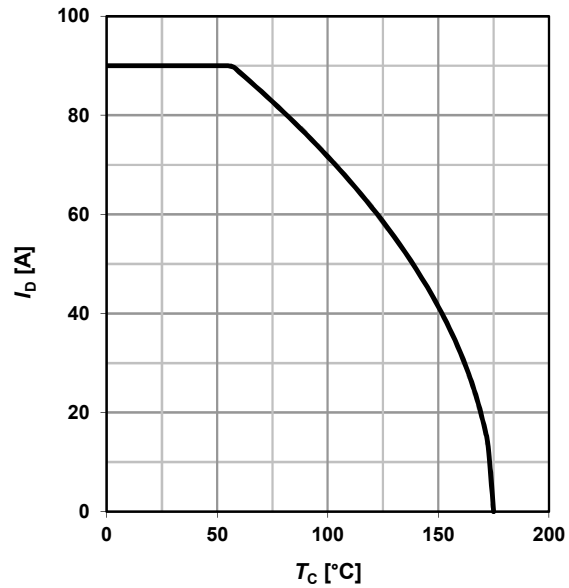
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} = 10\text{ V}$



2 Drain current

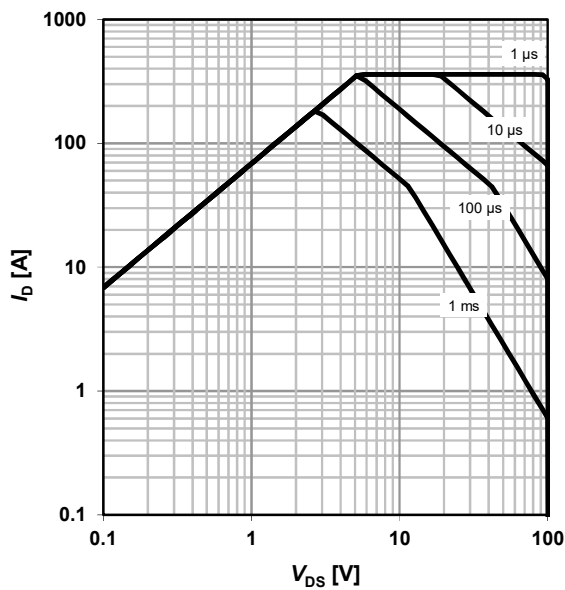
$I_D = f(T_C); V_{GS} = 10\text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

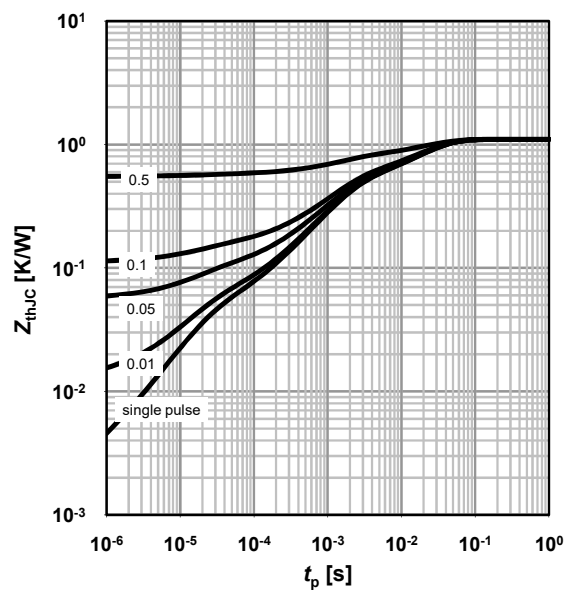
parameter: t_p



4 Max. transient thermal impedance

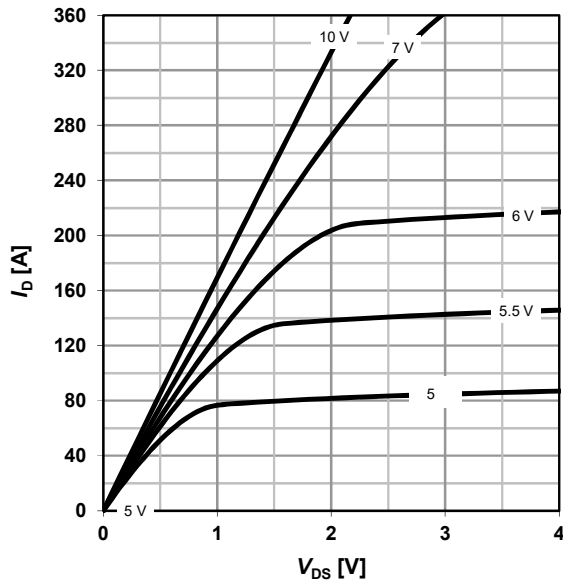
$Z_{thJC} = f(t_p)$

parameter: $D = t_p/T$

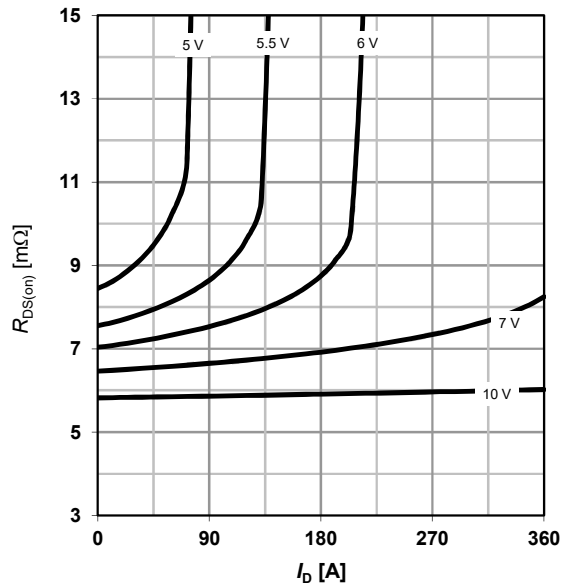


5 Typ. output characteristics

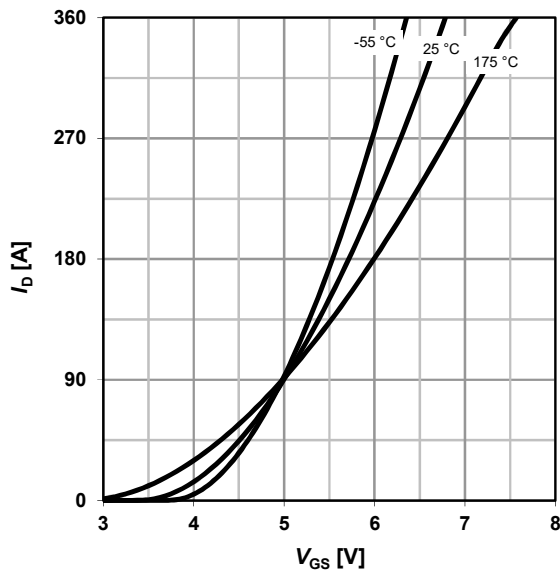
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter: V_{GS}

6 Typ. drain-source on-state resistance

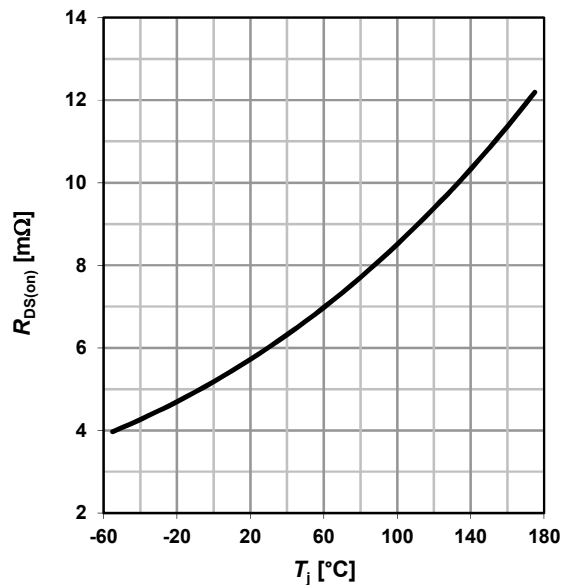
$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter: V_{GS}

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6V$$

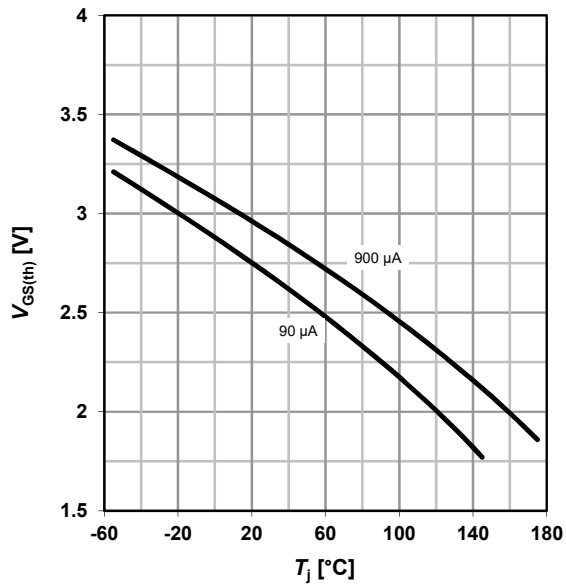
 parameter: T_j

8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = 90\text{ A}; V_{GS} = 10\text{ V}$$

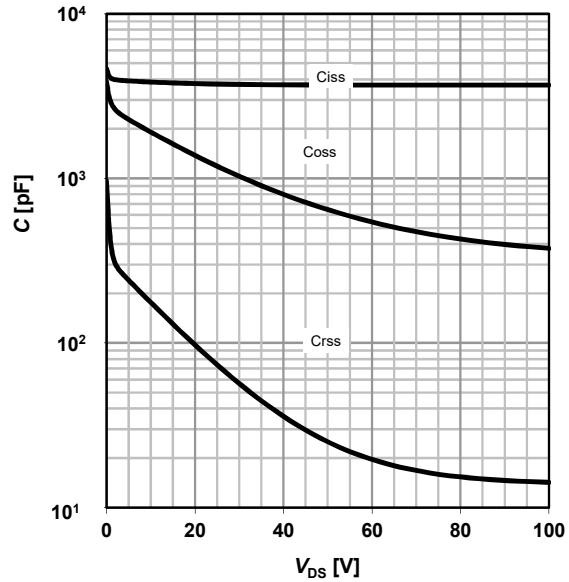
 $\alpha = 0.4$


9 Typ. gate threshold voltage

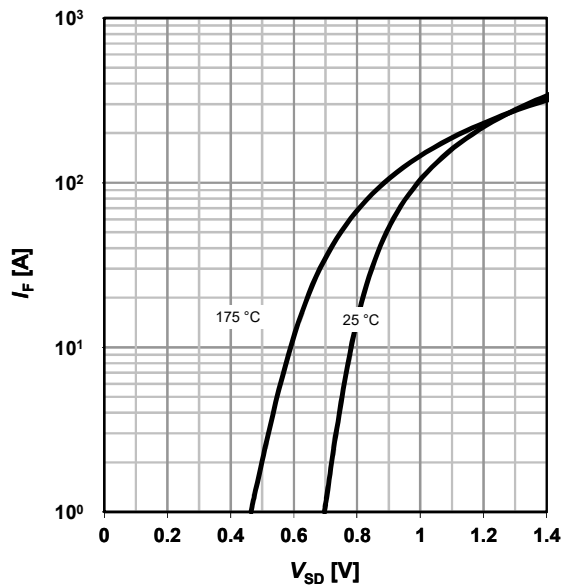
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

 parameter: I_D

10 Typ. capacitances

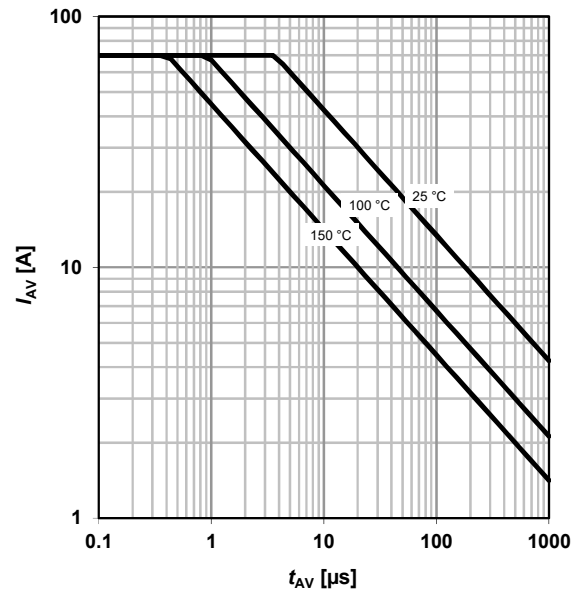
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 \text{ MHz}$$


11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

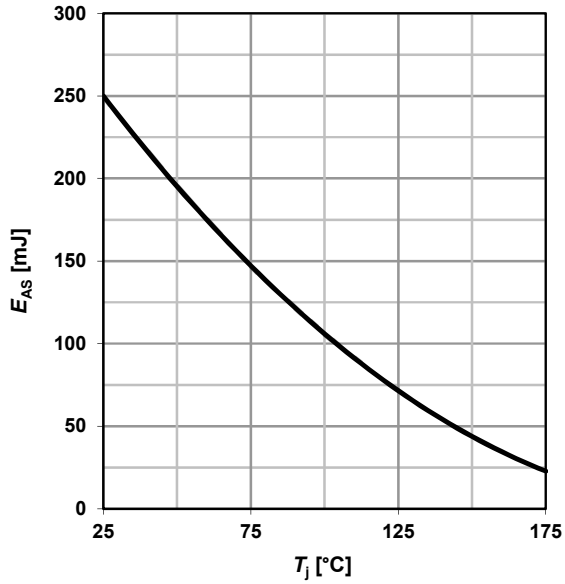
 parameter: T_j

12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

 parameter: $T_{j(start)}$


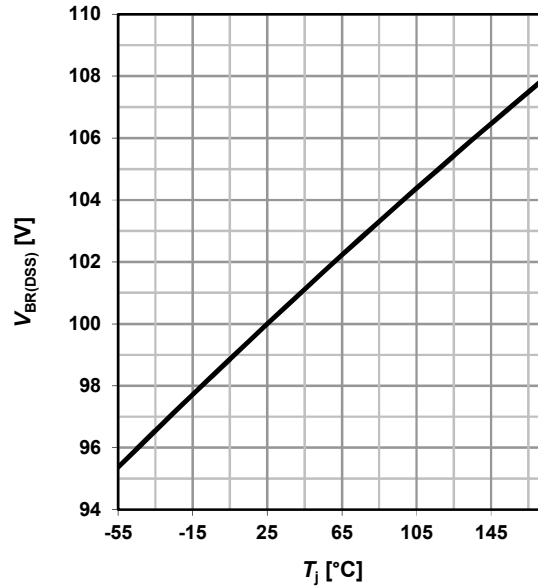
13 Avalanche energy

$E_{AS} = f(T_j); I_D = 45A$



14 Drain-source breakdown voltage

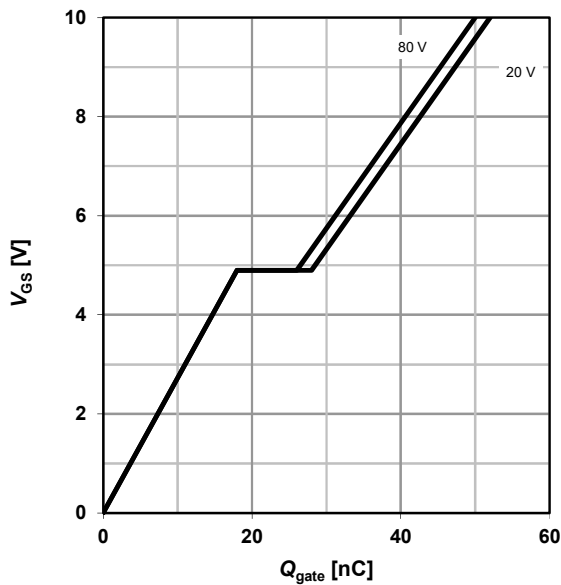
$V_{BR(DSS)} = f(T_j); I_D = 1 mA$



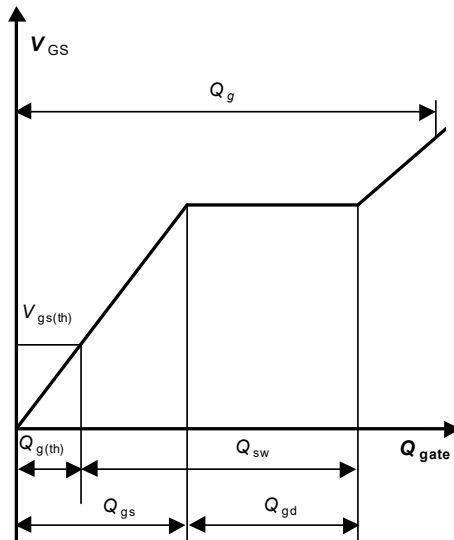
15 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 90 A$ pulsed

parameter: V_{DD}

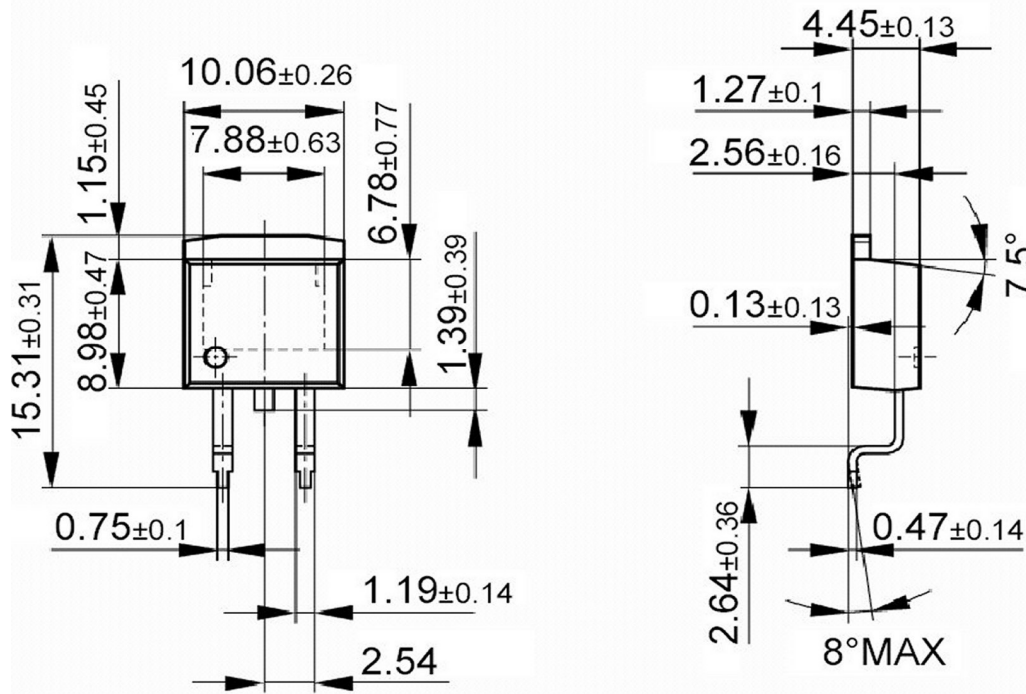


16 Gate charge waveforms

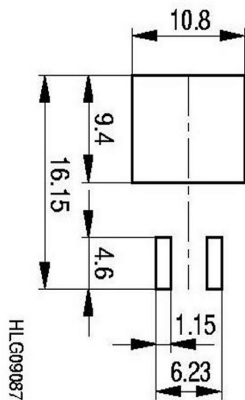


Package Outline

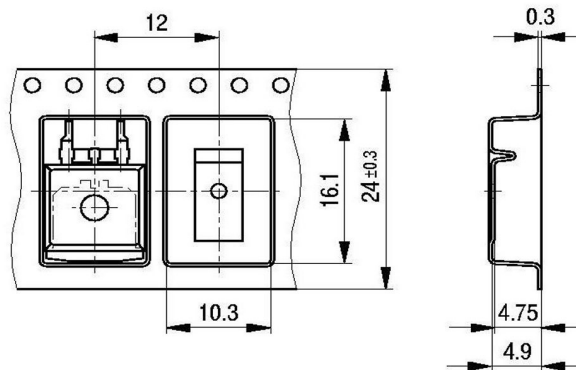
P-TO263-3-2: Outline



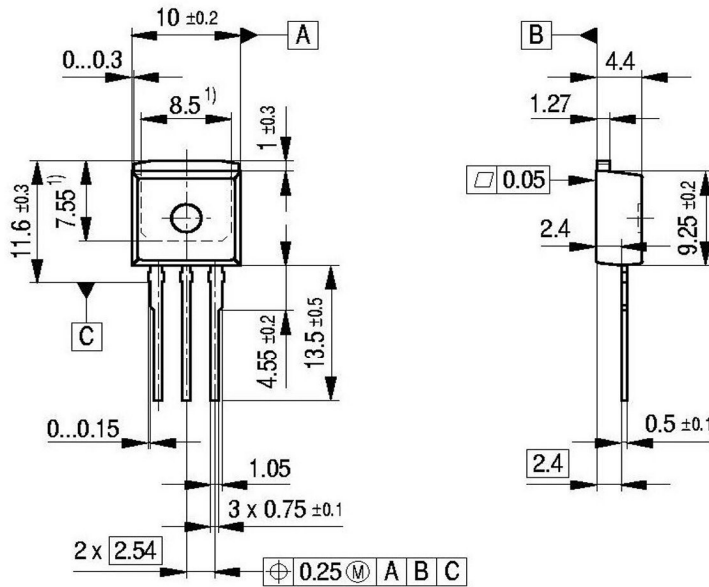
Footprint



Packaging

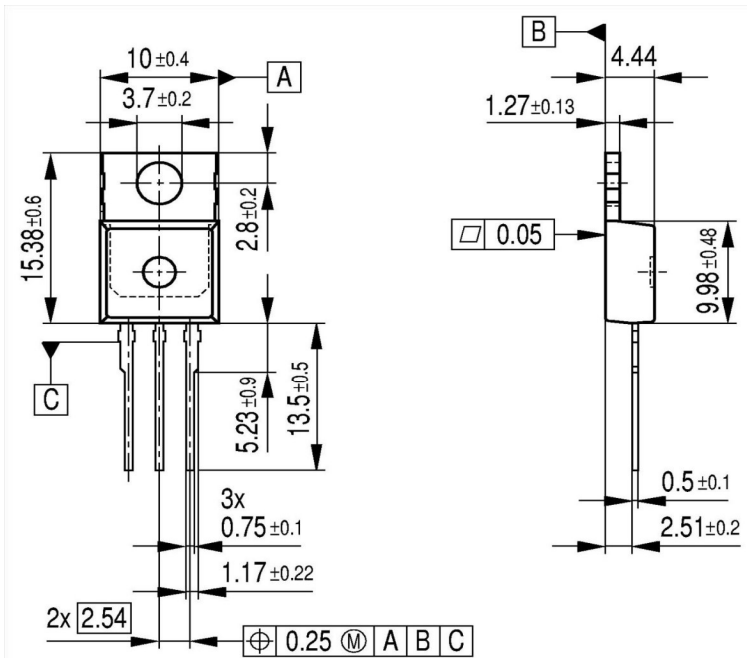


P-TO262-3-1: Outline



1) Typical
 Metal surface min. X = 7.25, Y = 6.9
 All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.
 Metal surface min. x=7.25, y=12.3

Packaging



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Revision History

Version	Date	Changes
Revision 1.0	2014-06-30	Data Sheet Revision 1.0
Revision 1.1	2023-01-30	Diagram 8 Typ. drain-source on-state resistance: used α value clarified