

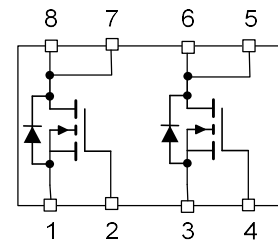
OptiMOS™-T2 Power-Transistor

Features

- Dual N-channel Normal Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

Product Summary

V_{DS}	100	V
$R_{DS(on),max}^{3)}$	61	m Ω
I_D	16	A

PG-TDSON-8-10


Type	Package	Marking
IPG16N10S4-61A	PG-TDSON-8-10	4N1061

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$	16	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	11	
Pulsed drain current ¹⁾ one channel active	$I_{D,pulse}$	-	64	
Avalanche energy, single pulse ^{1, 3)}	E_{AS}	$I_D=8\text{ A}$	33	mJ
Avalanche current, single pulse ³⁾	I_{AS}	-	10	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation one channel active	P_{tot}	$T_C=25\text{ °C}$	29	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	5.2	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm ² cooling area ²⁾	-	60	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=9\mu A$	2.0	2.8	3.5	
Zero gate voltage drain current ³⁾	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125\text{ °C}^{1)}$	-	1	100	
Gate-source leakage current ³⁾	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance ³⁾	$R_{DS(on)}$	$V_{GS}=10V, I_D=16A$	-	53	61	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance ³⁾	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	374	580	pF
Output capacitance ³⁾	C_{oss}		-	120	240	
Reverse transfer capacitance ³⁾	C_{rss}		-	10	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V,$ $I_D=16A, R_G=11\Omega$	-	3	-	ns
Rise time	t_r		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	5	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics^{1, 3)}

Gate to source charge	Q_{gs}	$V_{DD}=50V, I_D=16A,$ $V_{GS}=0$ to 10V	-	2	3.0	nC
Gate to drain charge	Q_{gd}		-	1.3	2.6	
Gate charge total	Q_g		-	5.4	9.5	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V

Reverse Diode

Diode continuous forward current ¹⁾ one channel active	I_S	$T_C=25^\circ C$	-	-	16	A
Diode pulse current ¹⁾ one channel active	$I_{S,pulse}$		-	-	64	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=16A,$ $T_j=25^\circ C$	-	1.0	1.3	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	50	-	ns
Reverse recovery charge ^{1, 3)}	Q_{rr}		-	70	-	nC

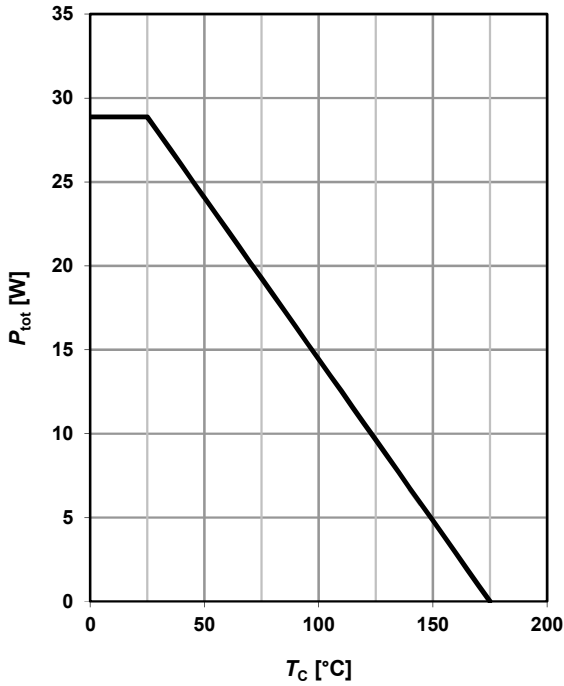
¹⁾ Specified by design. Not subject to production test.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ Per channel

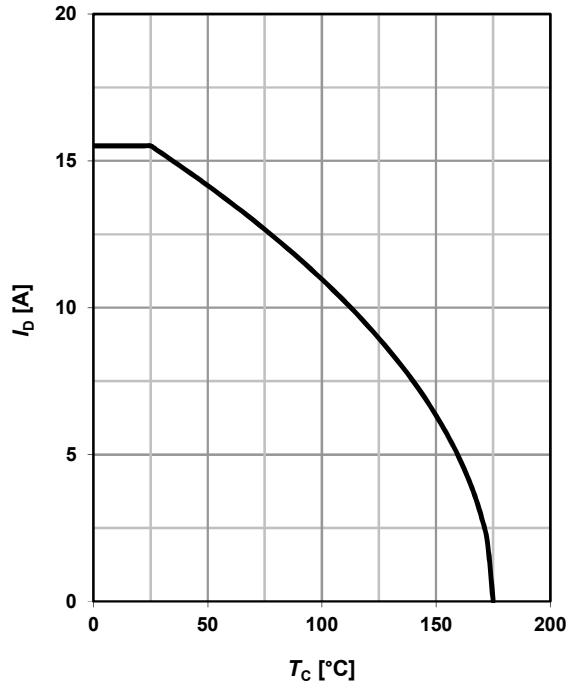
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6\text{ V}$; one channel active



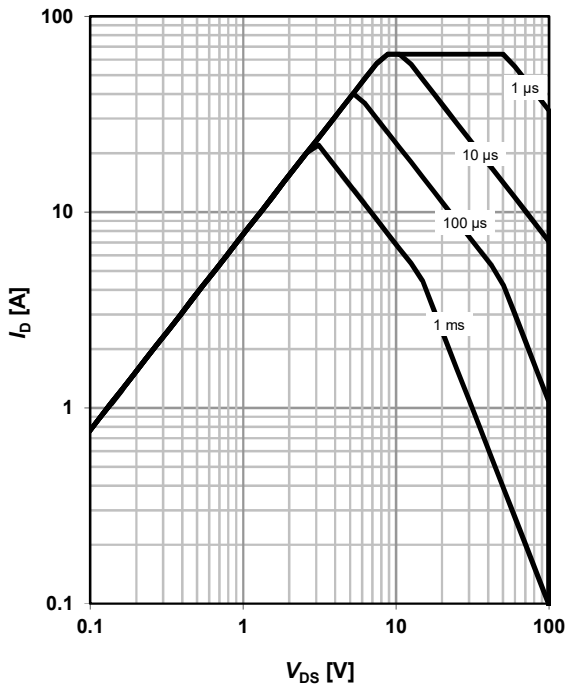
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6\text{ V}$; one channel active



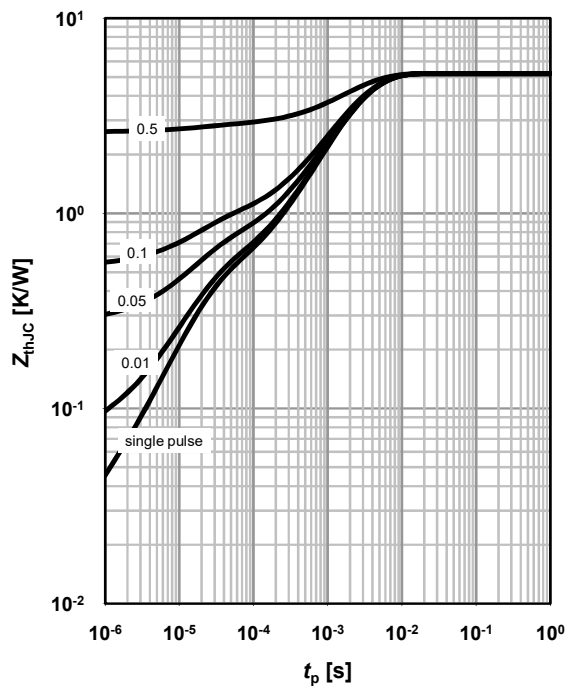
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25^\circ\text{C}$; $D = 0$; one channel active
parameter: t_p



4 Max. transient thermal impedance

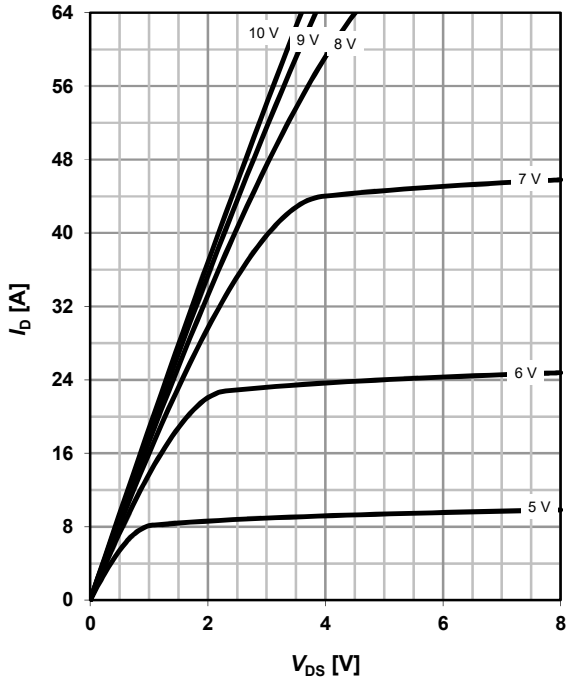
$Z_{thJC} = f(t_p)$
parameter: $D = t_p/T$



5 Typ. output characteristics³⁾

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

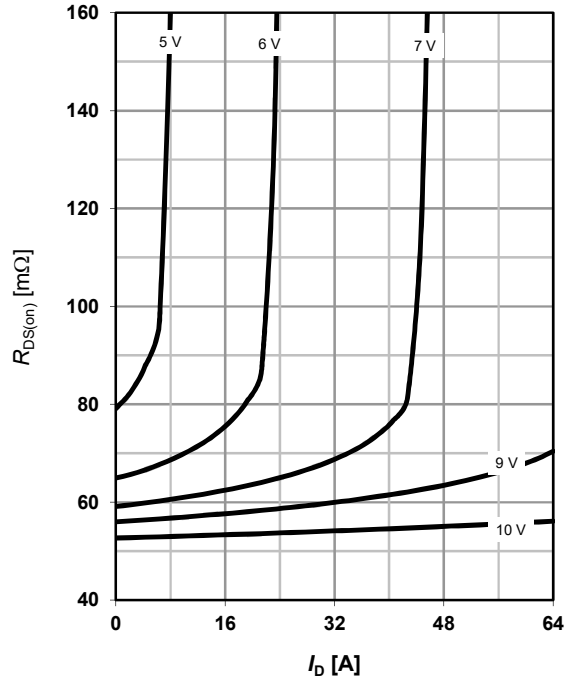
parameter: V_{GS}



6 Typ. drain-source on-state resistance³⁾

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

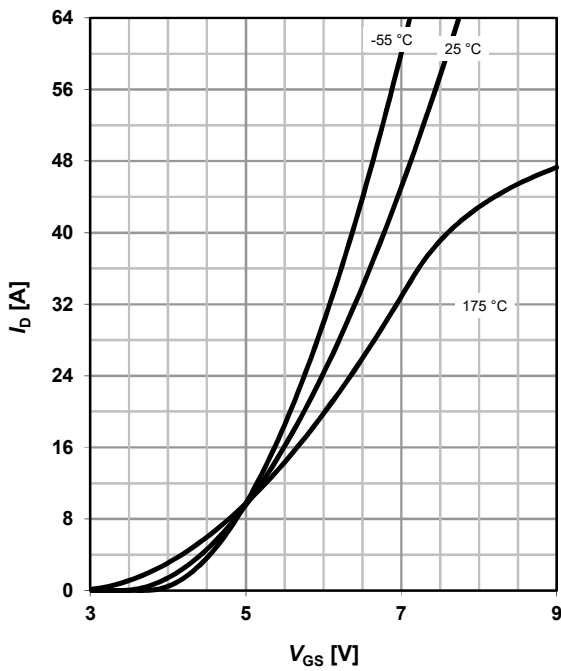
parameter: V_{GS}



7 Typ. transfer characteristics³⁾

$I_D = f(V_{GS}); V_{DS} = 6V$

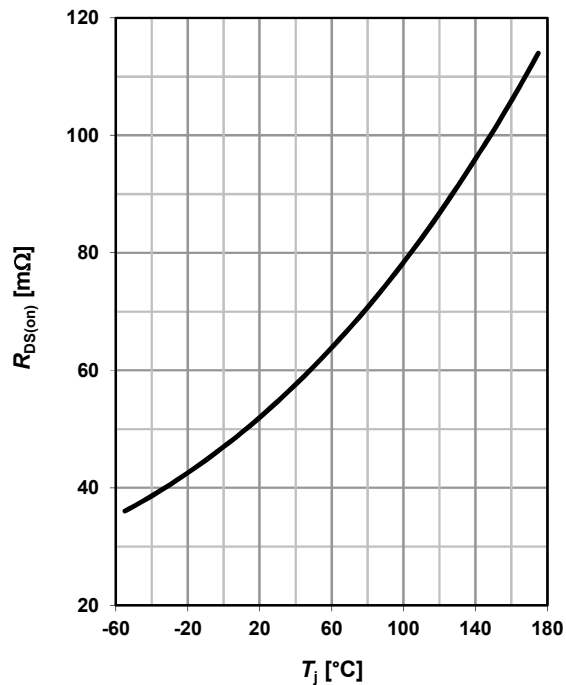
parameter: T_j



8 Typ. drain-source on-state resistance³⁾

$R_{DS(on)} = f(T_j); I_D = 16\text{ A}; V_{GS} = 10\text{ V}$

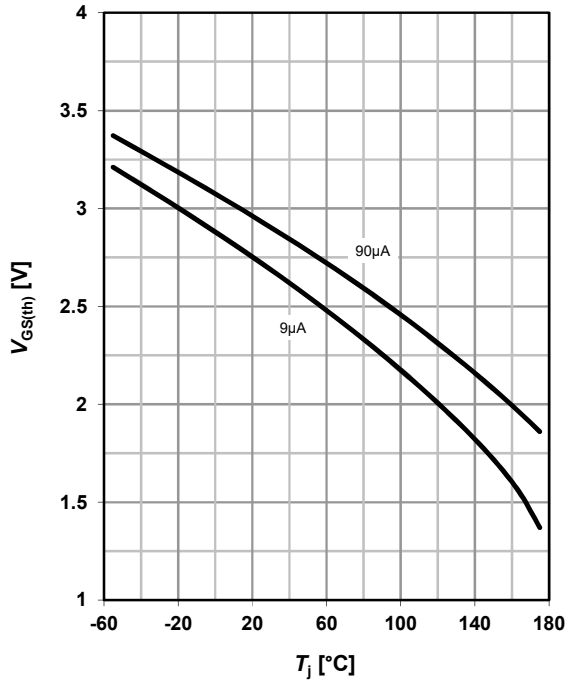
$\alpha = 0.4$



9 Typ. gate threshold voltage

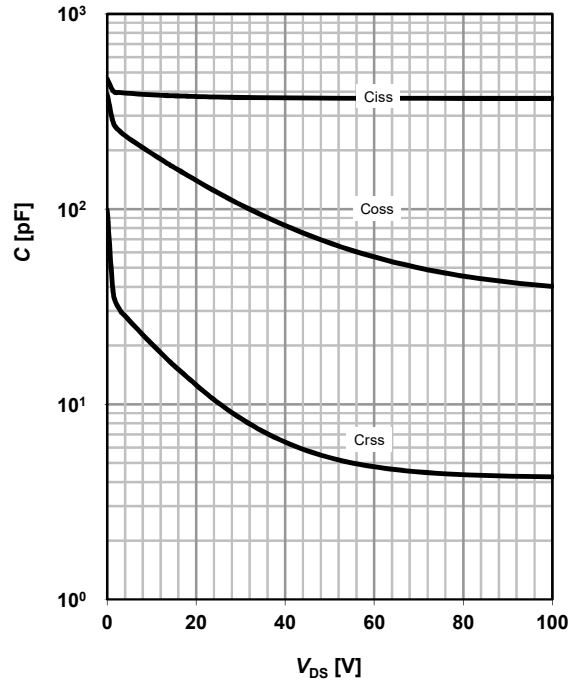
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances³⁾

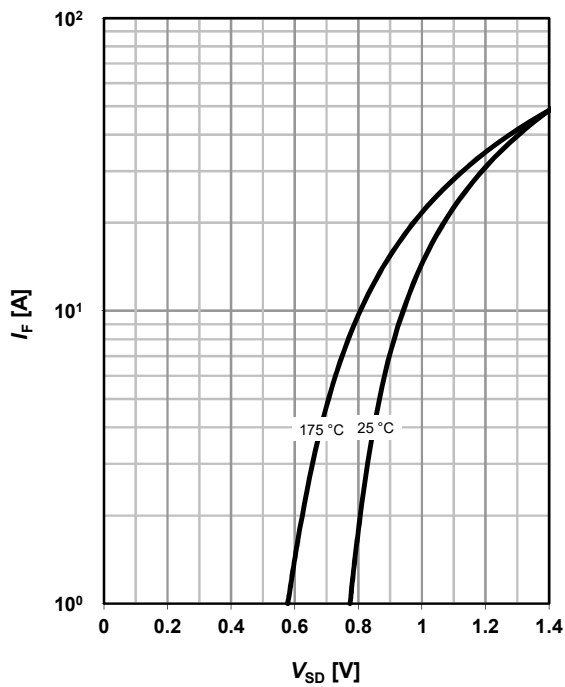
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics³⁾

$I_F = f(V_{SD})$

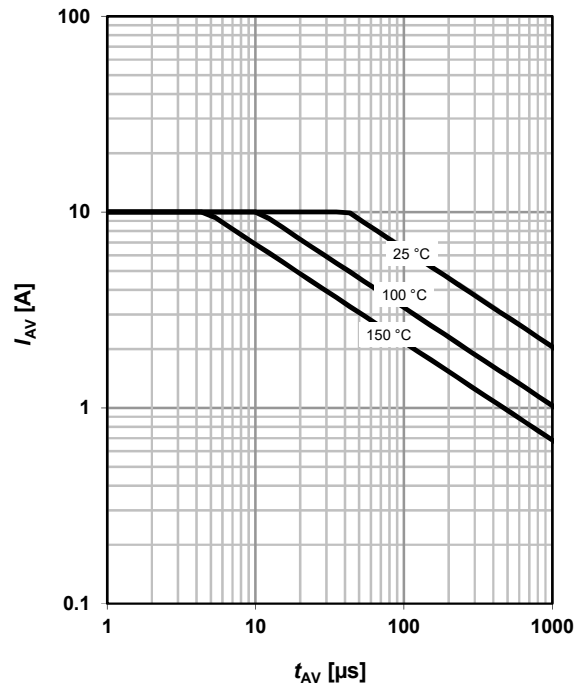
parameter: T_j



12 Avalanche characteristics³⁾

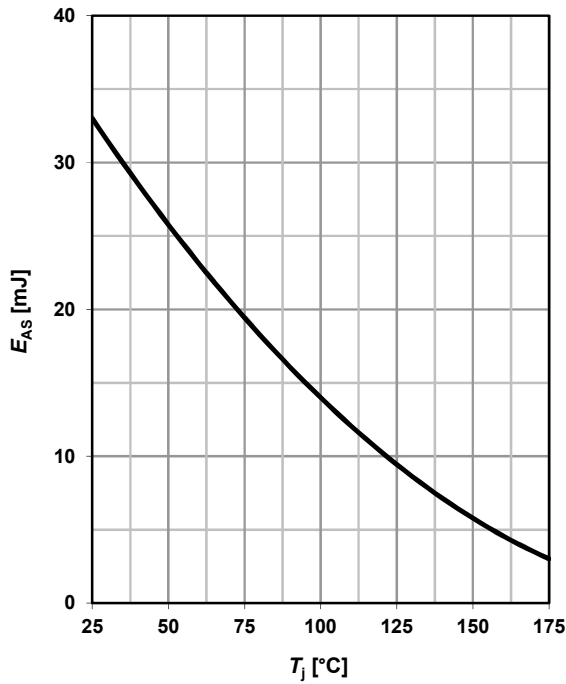
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



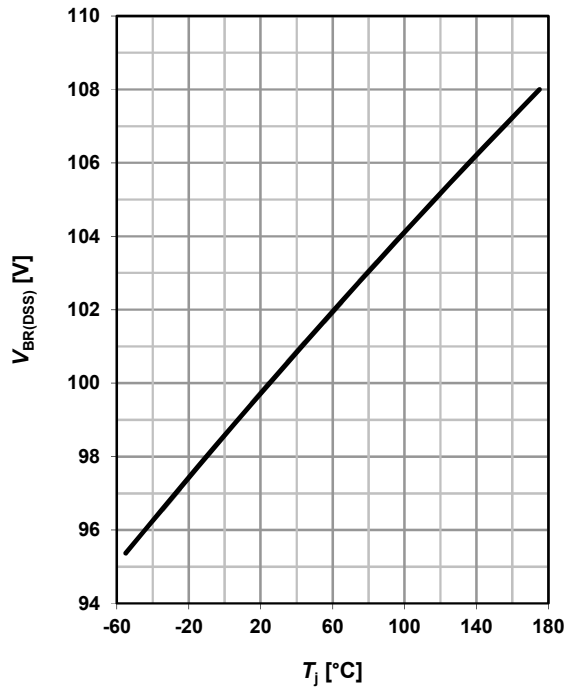
13 Avalanche energy³⁾

$E_{AS} = f(T_j), I_D = 8A$



14 Drain-source breakdown voltage

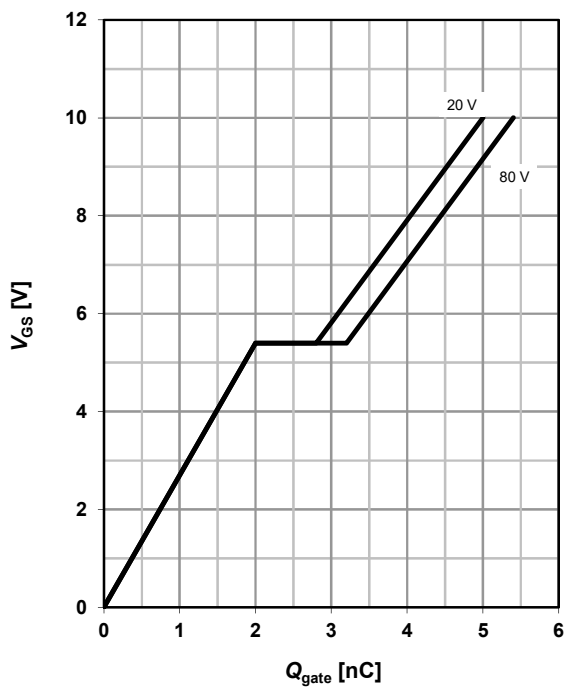
$V_{BR(DSS)} = f(T_j); I_D = 1 mA$



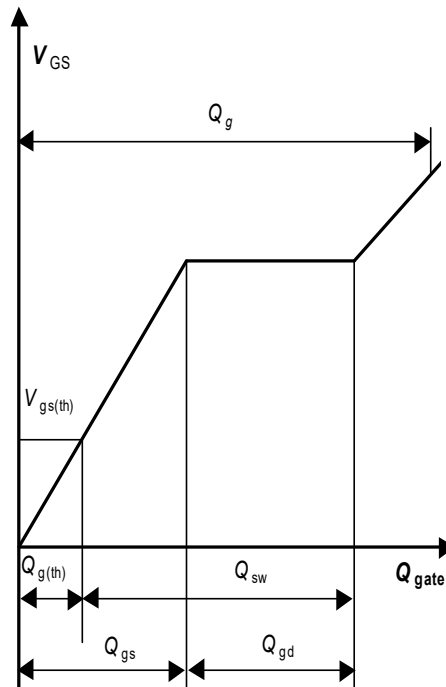
15 Typ. gate charge⁵⁾

$V_{GS} = f(Q_{gate}); I_D = 16 A$ pulsed

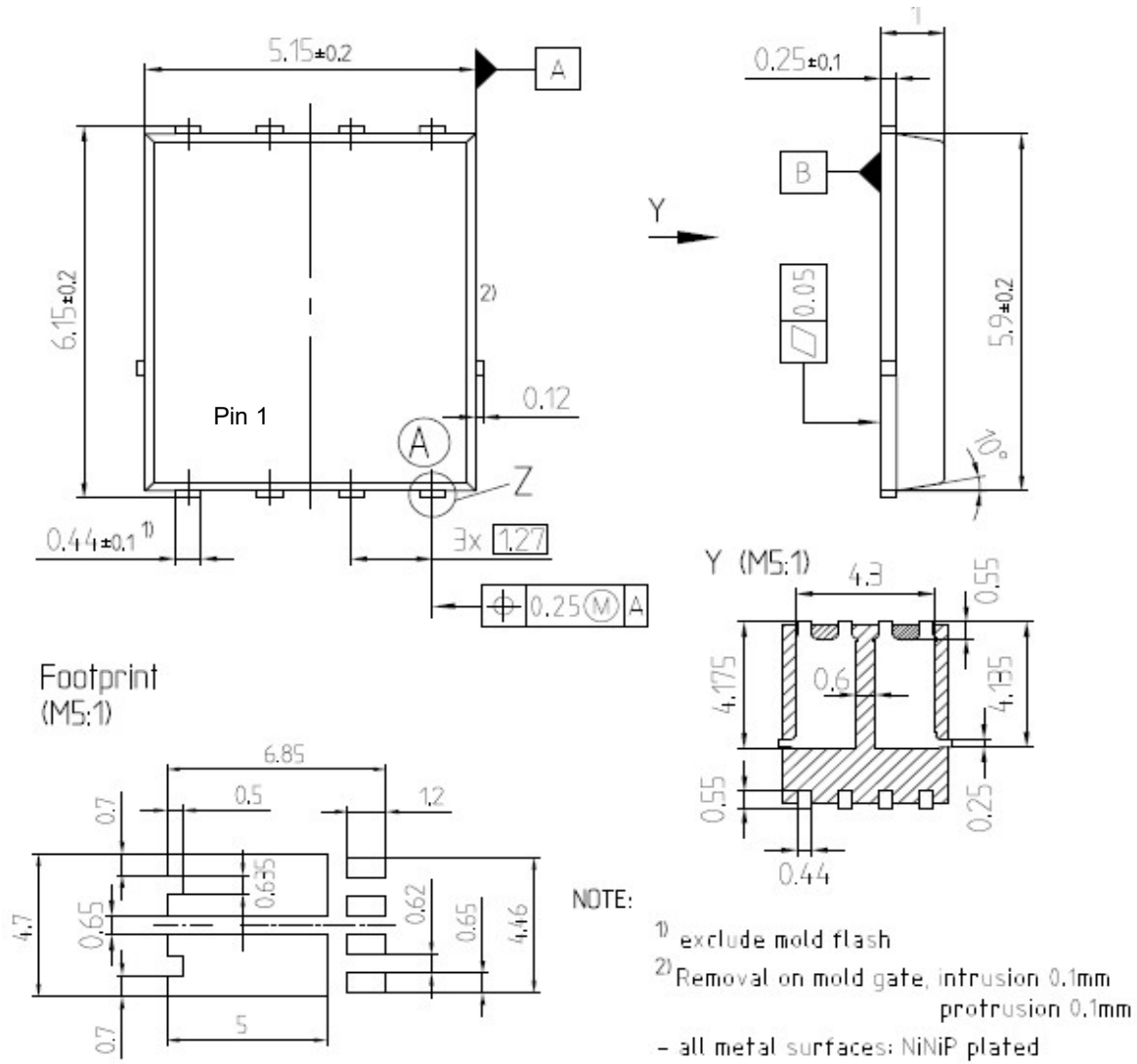
parameter: V_{DD}



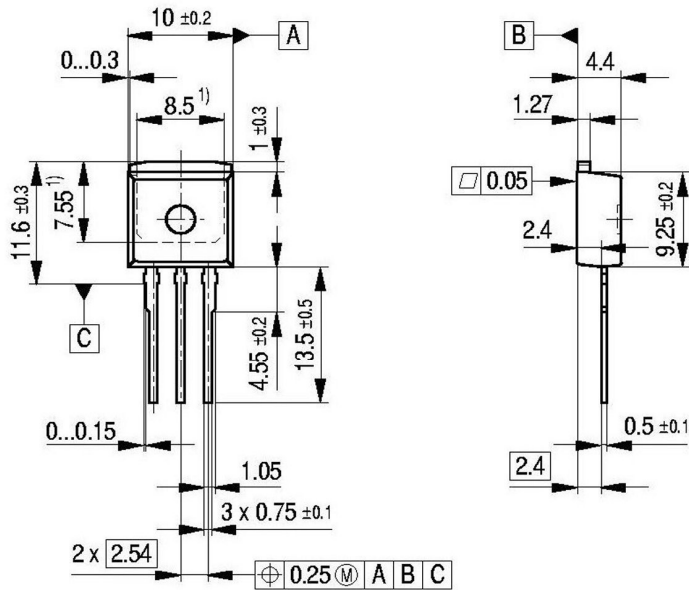
16 Gate charge waveforms



Package Outline



P-TO262-3-1: Outline

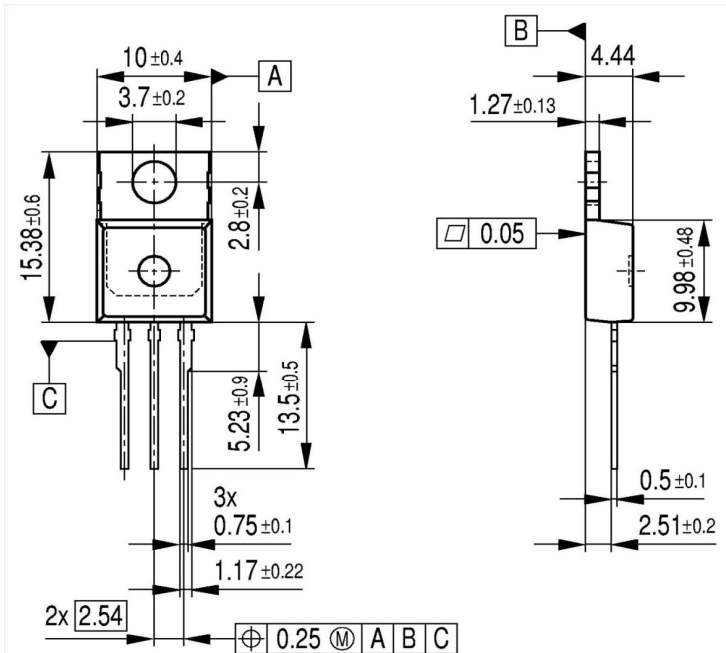


1) Typical

Metal surface min. X = 7.25, Y = 6.9

All metal surfaces tin plated, except area of cut.

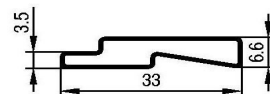
P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.

Metal surface min. x=7.25, y=12.3

Packaging



Dimensions in mm

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Revision History

Version	Date	Changes
Revision 1.0	2013-03-04	Final Data Sheet
Revision 1.1	2014-11-14	Update of Coss, Ciss, Qgs, Qtot
Revision 1.2	2022-07-28	Diagram 8 Typ. drain-source on-state resistance: used α value clarified