

OptiMOS™-T2 Power-Transistor



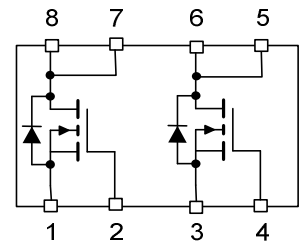
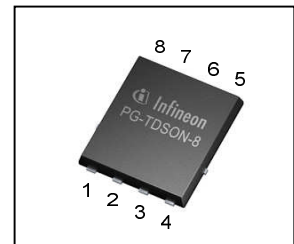
Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	100	V
$R_{DS(on),max}^{4)}$	35	mΩ
I_D	20	A

PG-TDSON-8-4



Type	Package	Marking
IPG20N10S4L-35	PG-TDSON-8-4	4N10L35

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	20	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	17	
Pulsed drain current ²⁾ one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse ^{2, 4)}	E_{AS}	$I_D=10\text{ A}$	60	mJ
Avalanche current, single pulse ⁴⁾	I_{AS}	-	15	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation one channel active	P_{tot}	$T_C=25\text{ °C}$	43	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	3.5	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm ² cooling area ³⁾	-	60	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=16\mu\text{A}$	1.1	1.6	2.1	
Zero gate voltage drain current ⁴⁾	I_{DSS}	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current ⁴⁾	I_{GSS}	$V_{GS}=16\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance ⁴⁾	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$, $I_D=10\text{ A}$	-	38	45	m Ω
		$V_{GS}=10\text{ V}$, $I_D=17\text{ A}$	-	29	35	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance ⁴⁾	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	850	1105	pF
Output capacitance ⁴⁾	C_{oss}		-	285	370	
Reverse transfer capacitance ⁴⁾	C_{rss}		-	30	60	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=11\ \Omega$	-	3	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	18	-	
Fall time	t_f		-	13	-	

Gate Charge Characteristics^{2, 4)}

Gate to source charge	Q_{gs}	$V_{DD}=80\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	2.9	3.8	nC
Gate to drain charge	Q_{gd}		-	3.2	6.4	
Gate charge total	Q_g		-	13.4	17.4	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V

Reverse Diode

Diode continuous forward current ²⁾ one channel active	I_S	$T_C=25\text{ °C}$	-	-	20	A
Diode pulse current ²⁾ one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=17\text{ A},$ $T_J=25\text{ °C}$	-	1.0	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	50	-	ns
Reverse recovery charge ^{2, 4)}	Q_{rr}		-	75	-	nC

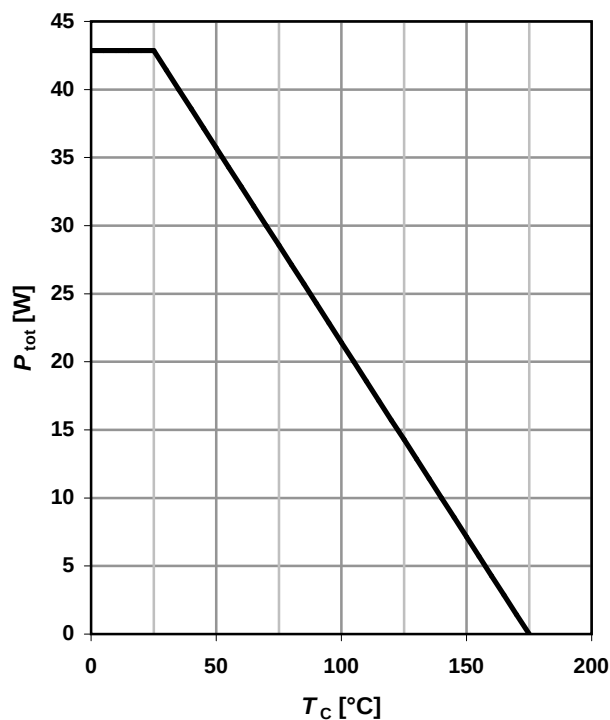
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 3.5\text{K/W}$ the chip is able to carry 24A at 25°C.

²⁾ Specified by design. Not subject to production test.

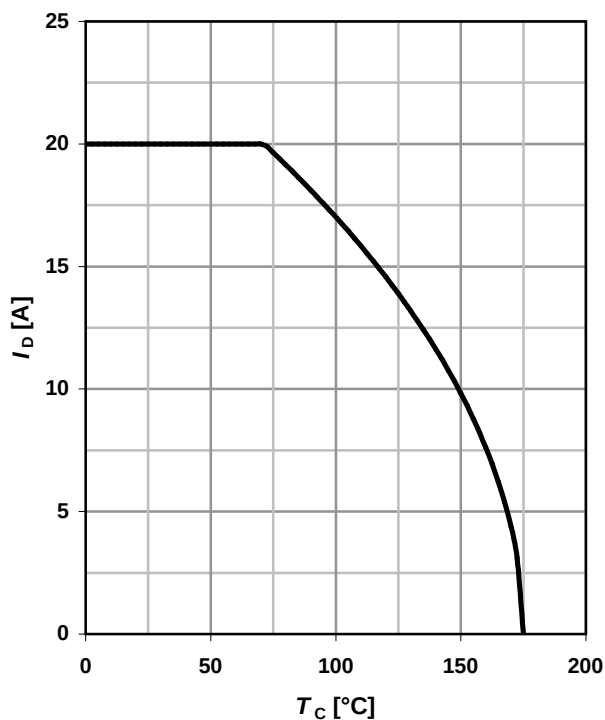
³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ Per channel

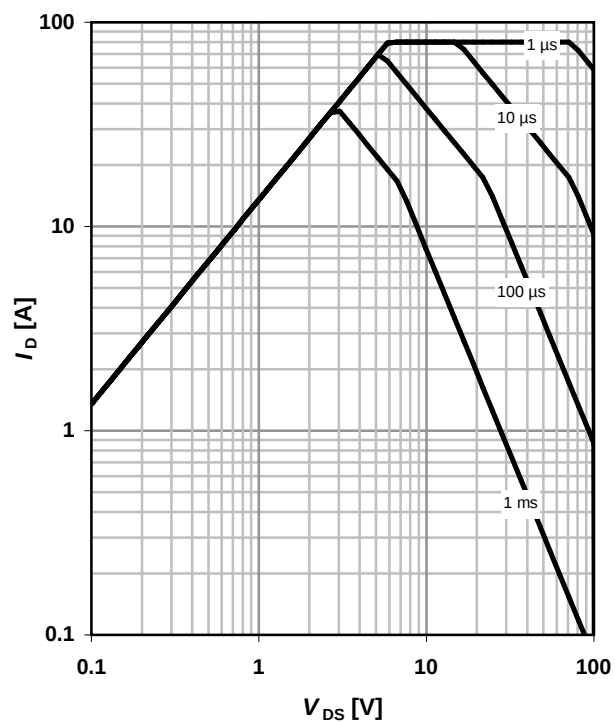
1 Power dissipation

 $P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{ one channel active}$


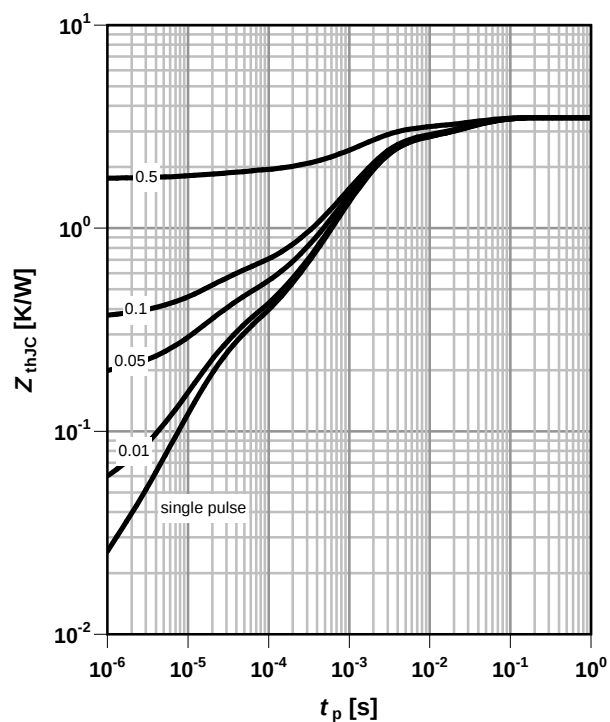
2 Drain current

 $I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}; \text{ one channel active}$


3 Safe operating area

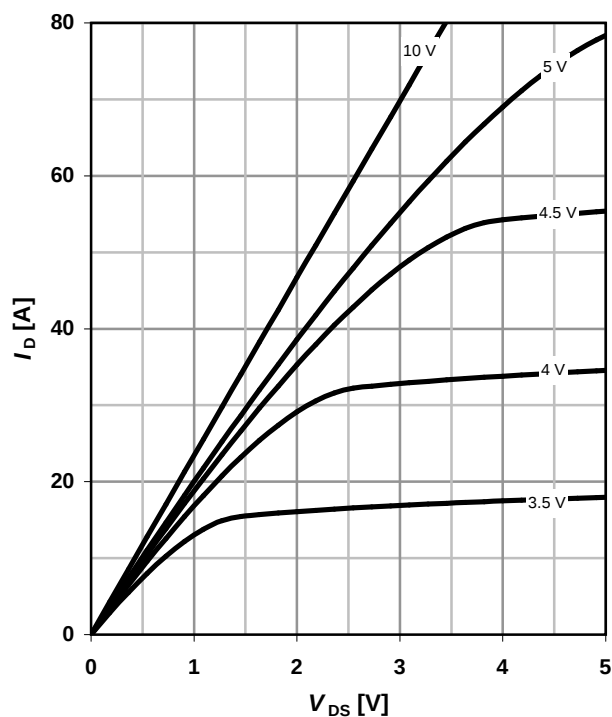
 $I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0; \text{ one channel active}$
parameter: t_p


4 Max. transient thermal impedance

 $Z_{\text{thJC}} = f(t_p)$
parameter: $D = t_p/T$


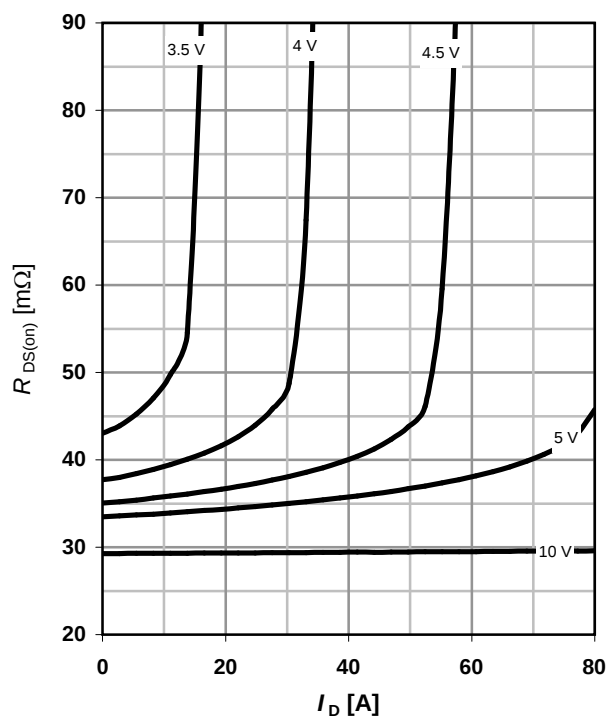
5 Typ. output characteristics⁵⁾

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


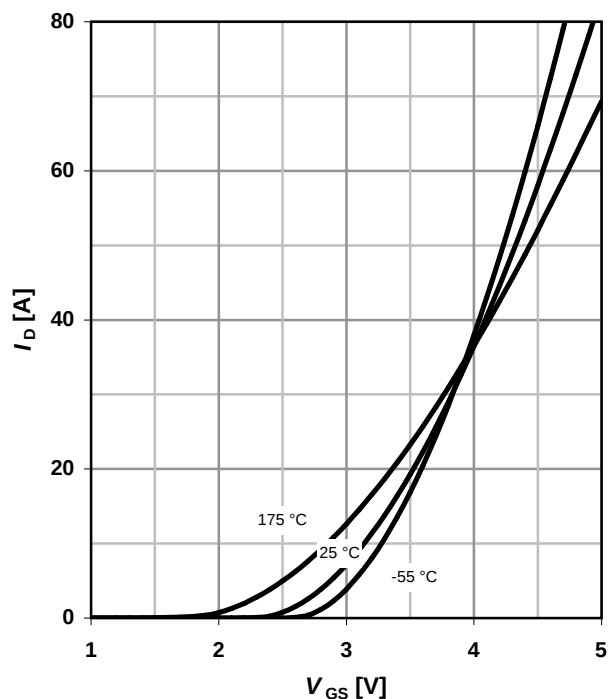
6 Typ. drain-source on-state resistance⁵⁾

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

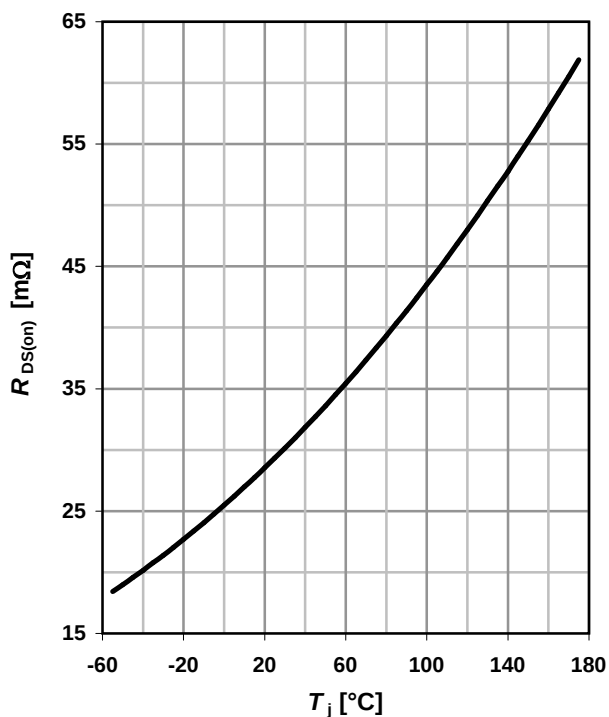
parameter: V_{GS}


7 Typ. transfer characteristics⁵⁾

 $I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j


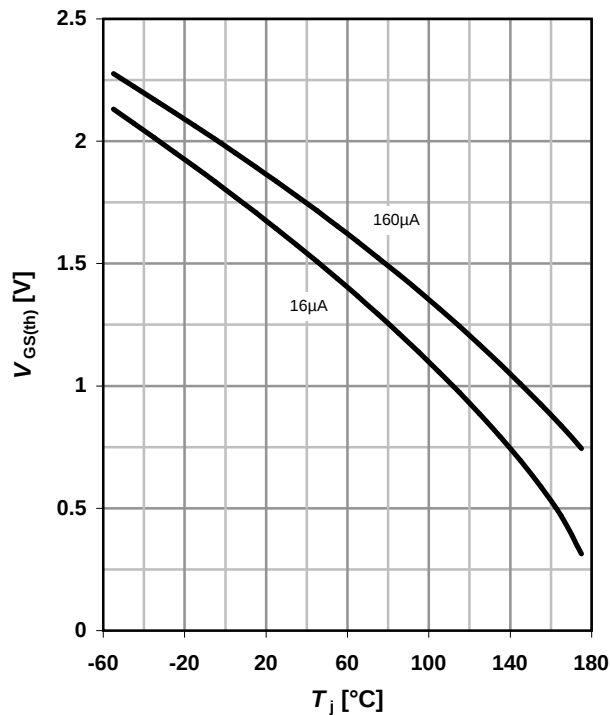
8 Typ. drain-source on-state resistance⁵⁾

 $R_{DS(on)} = f(T_j); I_D = 17\text{A}; V_{GS} = 10\text{V}$


9 Typ. gate threshold voltage

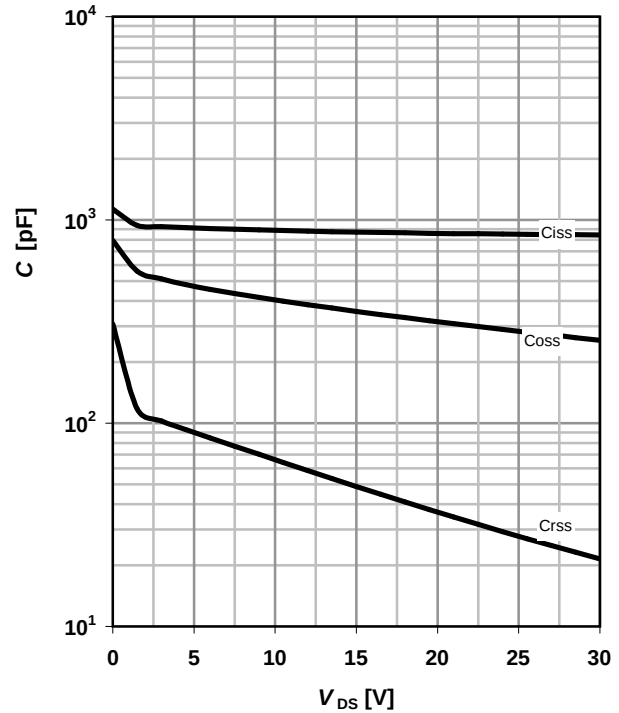
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. Capacitances⁵⁾

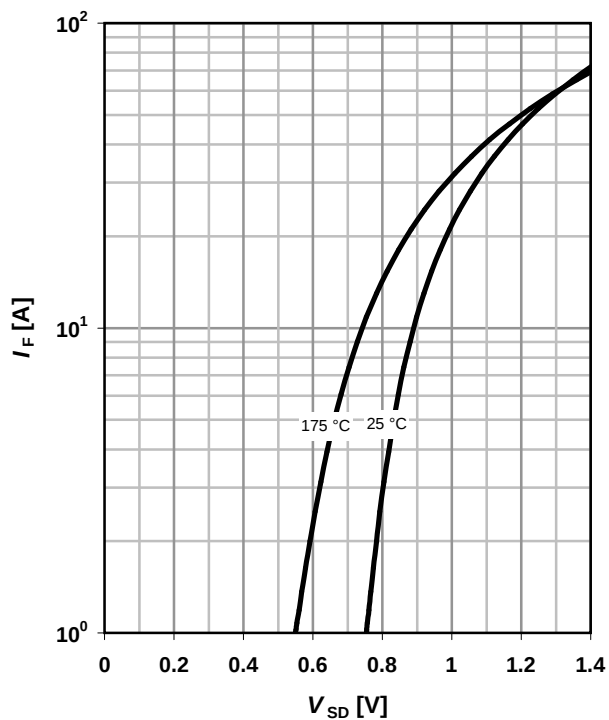
$$C = f(V_{DS}); V_{GS} = 0V; f = 1MHz$$



11 Typical forward diode characteristics⁵⁾

$$I_F = f(V_{SD})$$

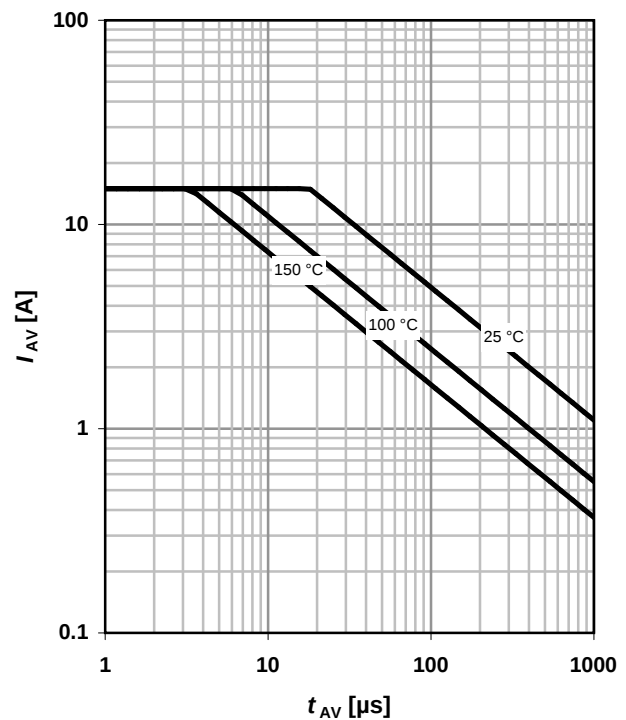
parameter: T_j



12 Avalanche characteristics⁵⁾

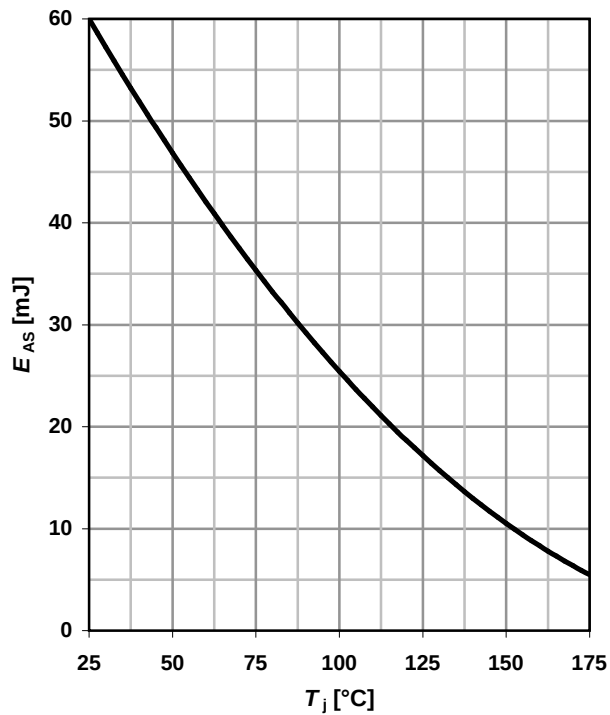
$$I_{AS} = f(t_{AV})$$

parameter: $T_{j(start)}$



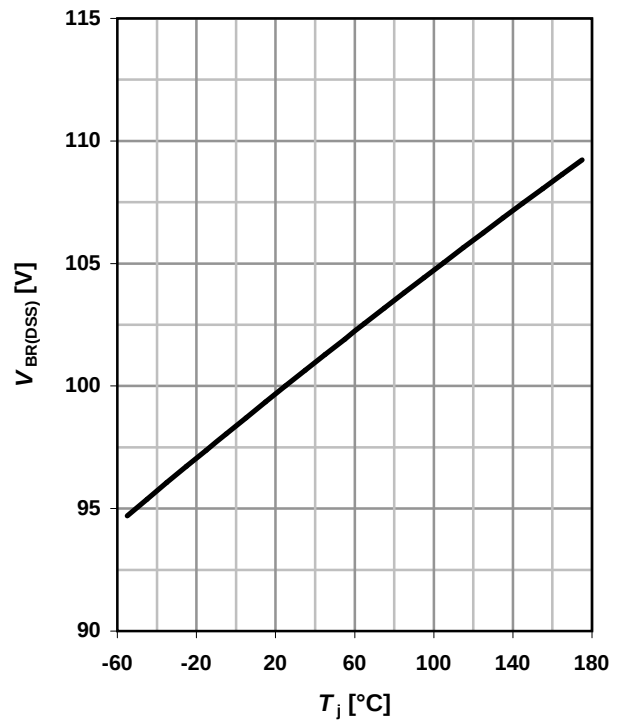
13 Avalanche energy⁵⁾

$$E_{AS}=f(T_j), I_D=10A$$



14 Drain-source breakdown voltage

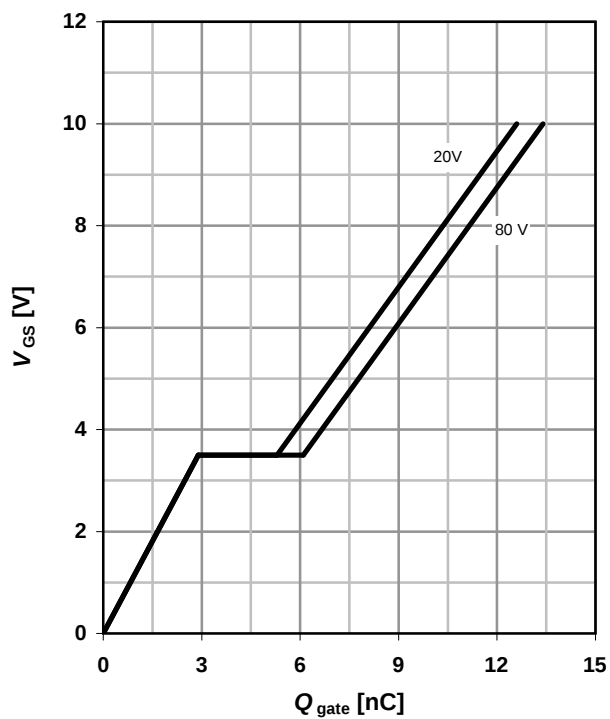
$$V_{BR(DSS)}=f(T_j); I_D=1mA$$



15 Typ. gate charge⁵⁾

$$V_{GS}=f(Q_{gate}); I_D=20A \text{ pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	29.11.2011	Final Data Sheet
Revision 1.1	15.05.2012	Update of product marking