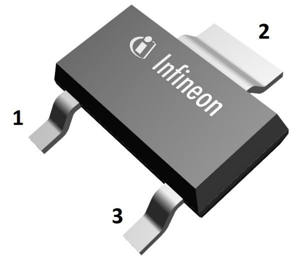
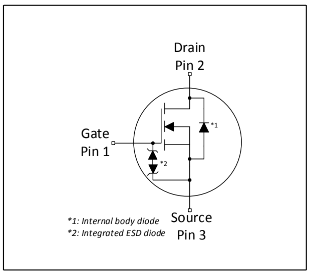
MOSFET

950V CoolMOS™ P7 SJ Power Device

The latest 950V CoolMOS™ P7 series sets a new benchmark in 950V super junction technologies and combines best-in-class performance with state of the art ease-of-use, resulting from Infineon's over 18 years pioneering super junction technology innovation.

PG-SOT223





Features

- Best-in-class FOM $R_{DS(on)}$ * E_{oss}; reduced Q_g, C_{iss}, and C_{oss}
- Best-in-class SOT-223 $R_{DS(on)}$
- Best-in-class $V_{(GS)th}$ of 3V and smallest $V_{(GS)th}$ variation of ±0.5V
- Integrated Zener Diode ESD protection
- Best-in-class CoolMOS™ quality and reliability
- Fully optimized portfolio

Benefits

- Best-in-class performance
- Enabling higher power density designs, BOM savings and lower assembly costs
- Easy to drive and to parallel
- Better production yield by reducing ESD related failures
- Less production issues and reduced field returns
- Easy to select right parts for fine tuning of designs

Potential applications

Recommended for flyback topologies for LED Lighting, low power Chargers and Adapters, Smart Meter, AUX power and Industrial power. Also suitable for PFC stage in Consumer and Solar applications.

Product Validation: Fully qualified acc. JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j=25°C}$	950	V
$R_{DS(on),max}$	3.7	Ω
$Q_{g,typ}$	6	nC
I_D	2	A
E_{oss} @ 500V	0.5	µJ
$V_{GS(th),typ}$	3	V
ESD class (HBM)	1C	-

Type / Ordering Code	Package	Marking	Related Links
IPN95R3K7P7	PG-SOT223	95R3K7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	2 1.4	A	T_C=25°C T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	5	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	2	mJ	I_D=0.2A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.04	mJ	I_D=0.2A; V_{DD}=50V; see table 10
Application (Flyback) relevant avalanche current, single pulse[3)]	I_{AS}	-	1.8	-	A	measured with standard leakage inductance of transformer of 10µH
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	6	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	0.8	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	5	A	T_C=25°C
Reverse diode dv/dt[4)]	dv/dt	-	-	1	V/ns	V_{DS}=0...400V, I_{SD}<=0.4A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	50	A/µs	V_{DS}=0...400V, I_{SD}<=0.4A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

1) Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.5; IPAK equivalent.
2) Pulse width t_p limited by $T_{j,max}$
3) For further explanation please read AN - CoolMOS™ 700V P7 & 950V P7
4) Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	19.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	160	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	75	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	950	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	2.5	3	3.5	V	V_{DS}=V_{GS}, I_D=0.04mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=950V, V_{GS}=0V, T_j=25°C V_{DS}=950V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	1000	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	3.11 6.86	3.7 -	Ω	V_{GS}=10V, I_D=0.8A, T_j=25°C V_{GS}=10V, I_D=0.8A, T_j=150°C
Gate resistance	R_G	-	1.5	-	Ω	f=250kHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	196	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	3	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	5	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	47	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.8A, R_G=50Ω; see table 9
Rise time	t_r	-	23	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.8A, R_G=50Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	46	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.8A, R_G=50Ω; see table 9
Fall time	t_f	-	40	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=0.8A, R_G=50Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1	-	nC	V_{DD}=760V, I_D=0.8A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	2	-	nC	V_{DD}=760V, I_D=0.8A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	6	-	nC	V_{DD}=760V, I_D=0.8A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	V_{DD}=760V, I_D=0.8A, V_{GS}=0 to 10V

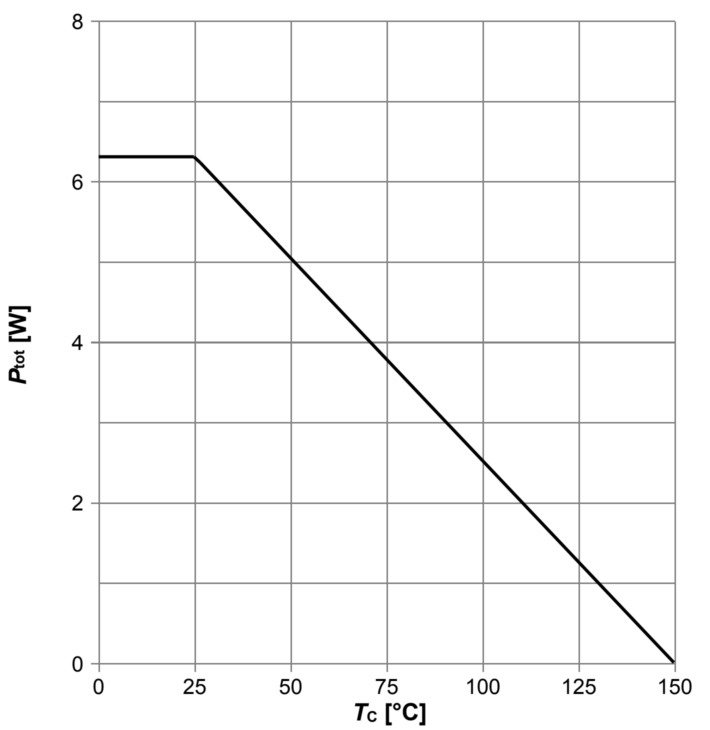
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=0.8A, T_j=25°C
Reverse recovery time	t_{rr}	-	320	-	ns	V_R=400V, I_F=0.4A, di_F/dt=50A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	1	-	µC	V_R=400V, I_F=0.4A, di_F/dt=50A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	5	-	A	V_R=400V, I_F=0.4A, di_F/dt=50A/µs; see table 8

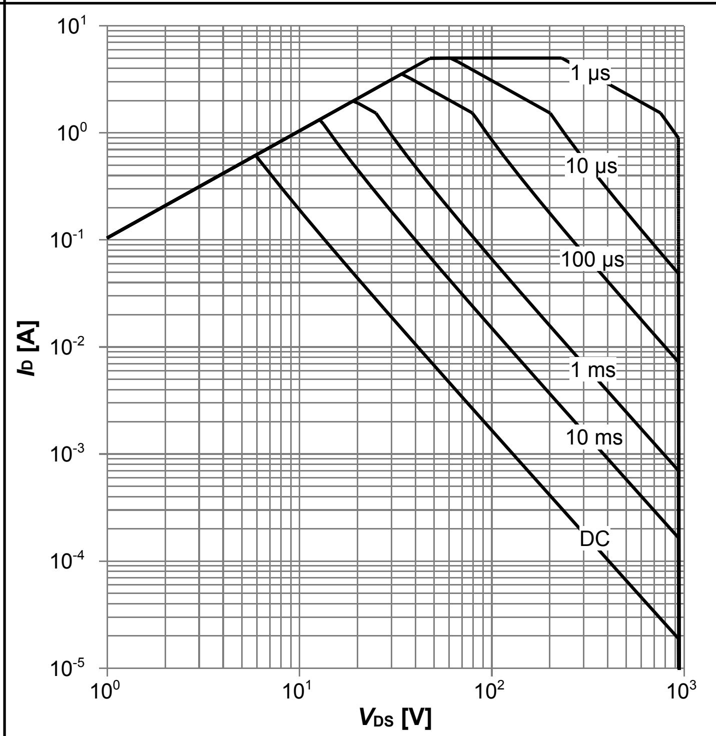
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



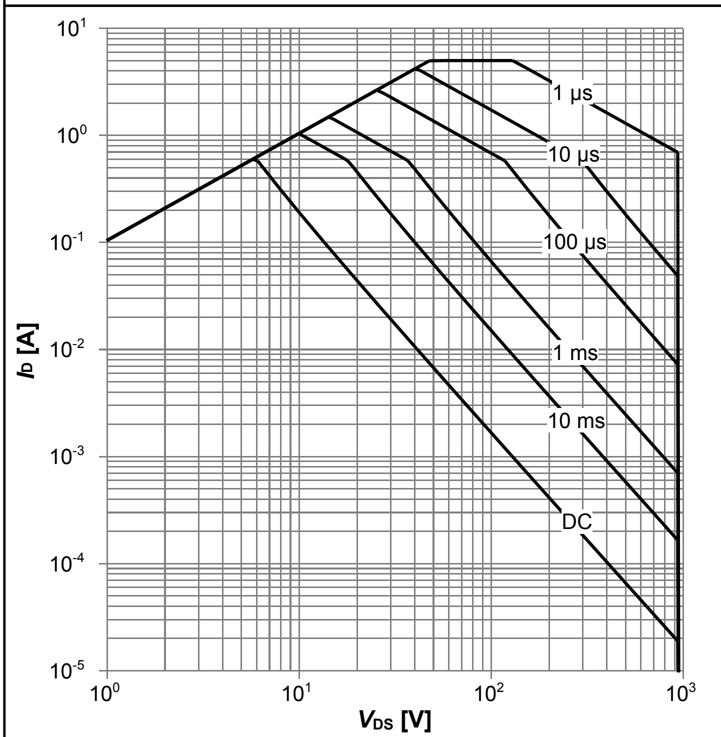
P_{tot}=f(T_C)

Diagram 2: Safe operating area



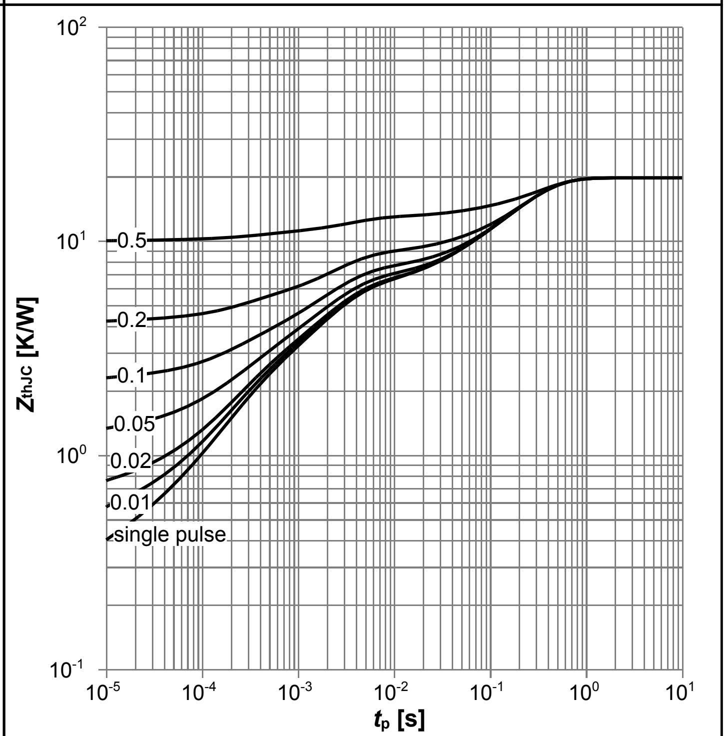
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



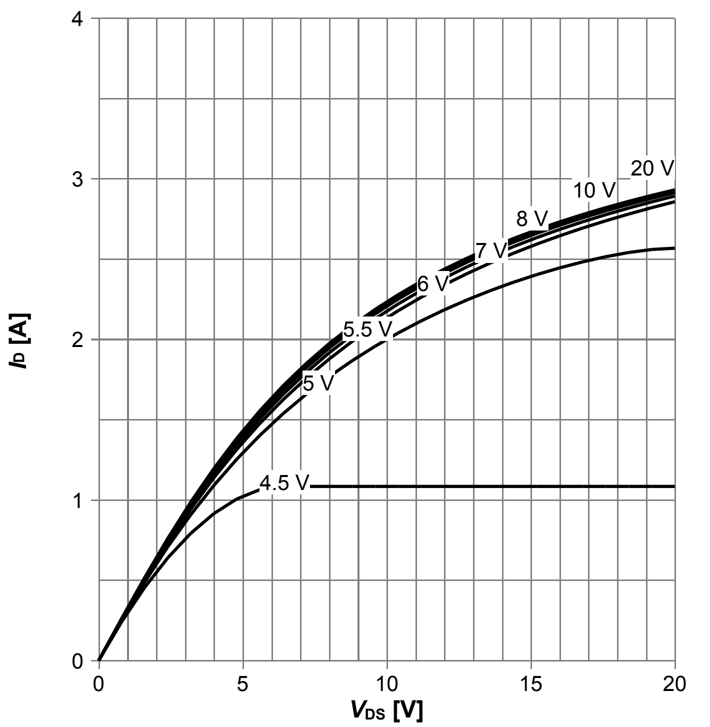
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



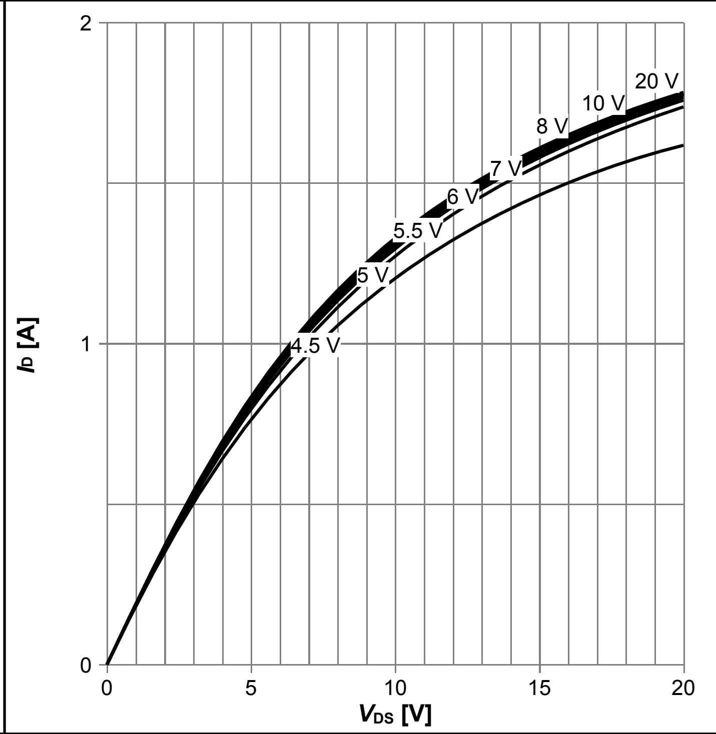
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



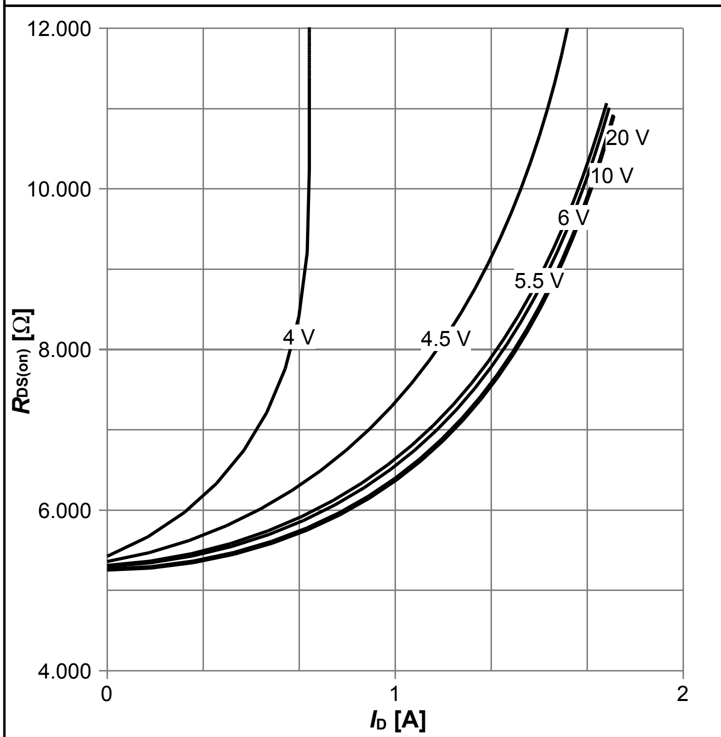
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



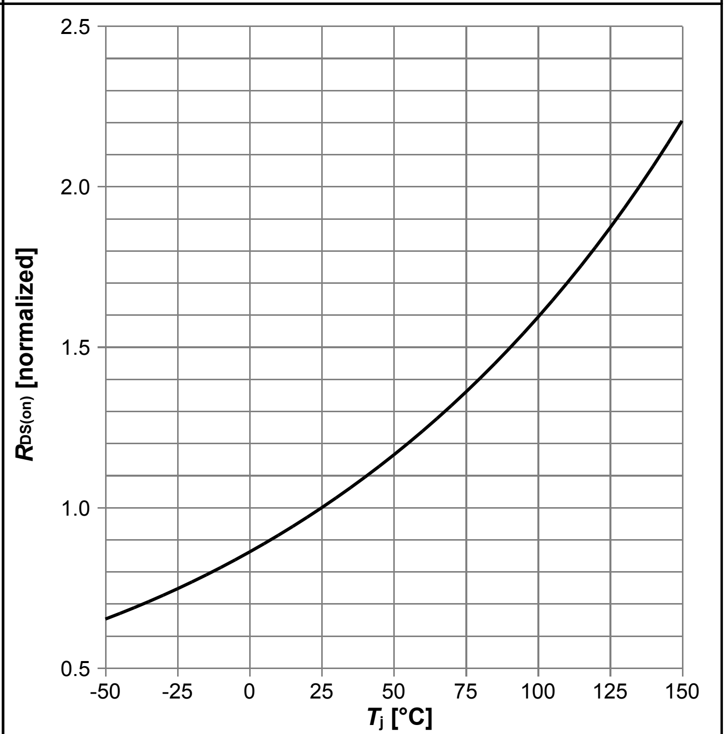
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



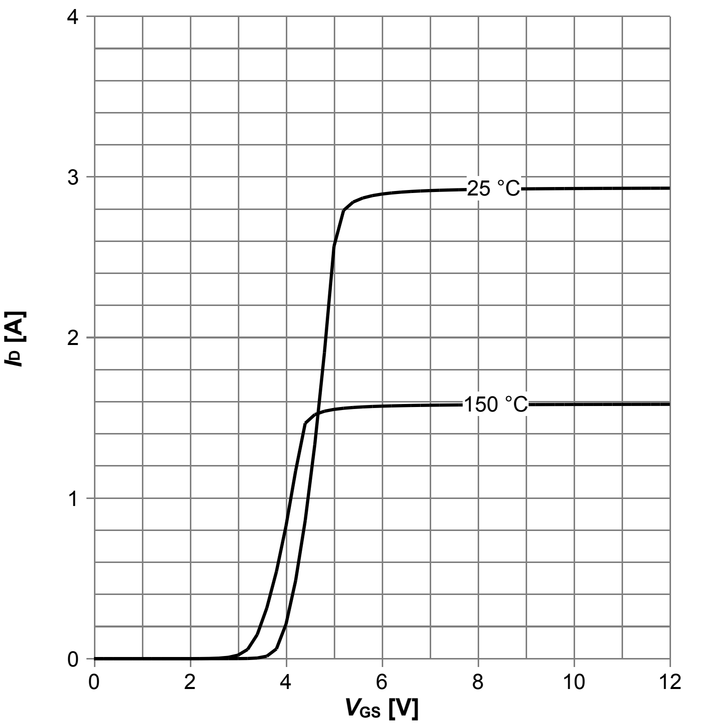
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



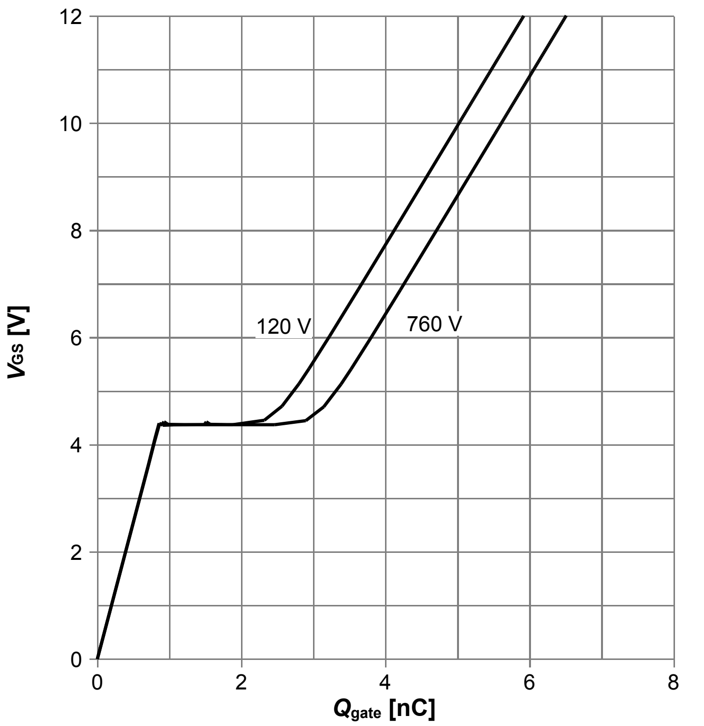
$R_{DS(on)}$=f(T_j); I_D=0.8 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



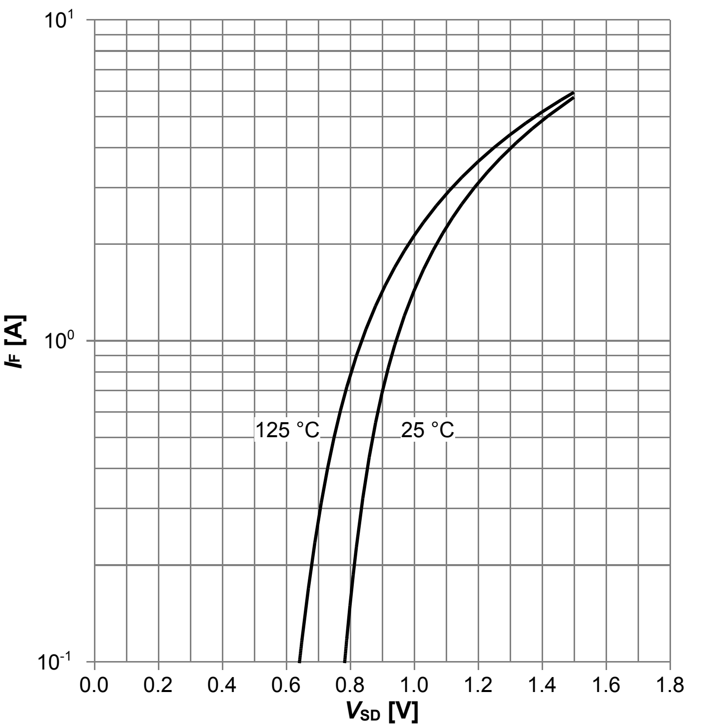
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



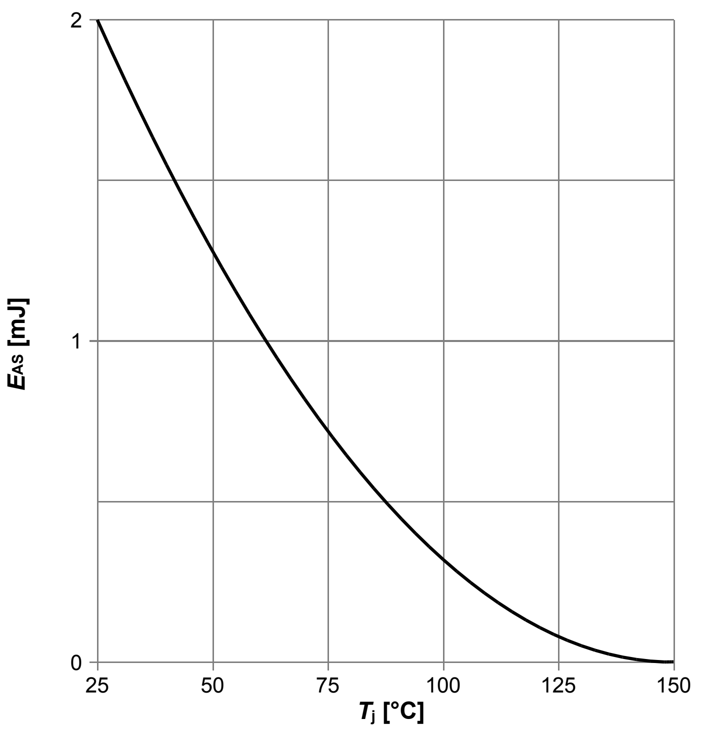
V_{GS}=f(Q_{gate}); I_D=0.8 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



E_{AS}=f(T_j); I_D=0.2 A; V_{DD}=50 V

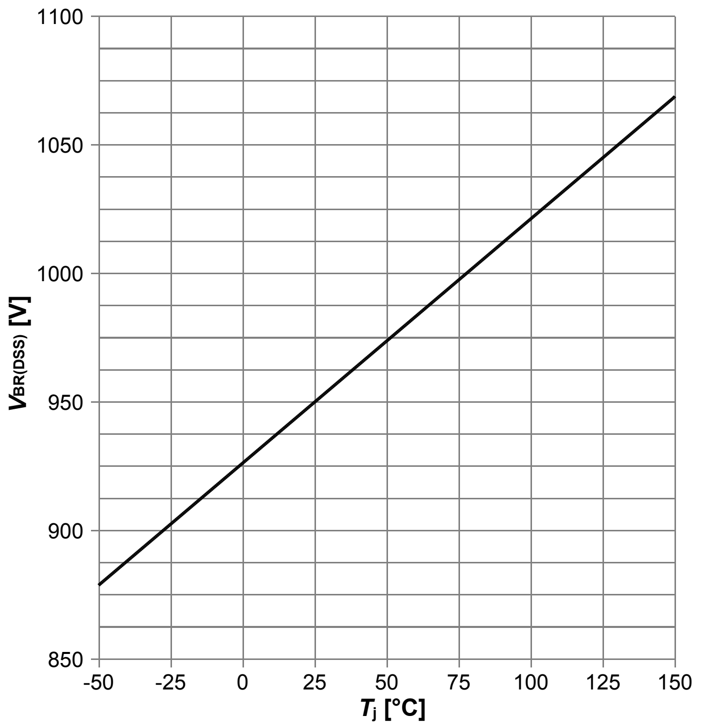
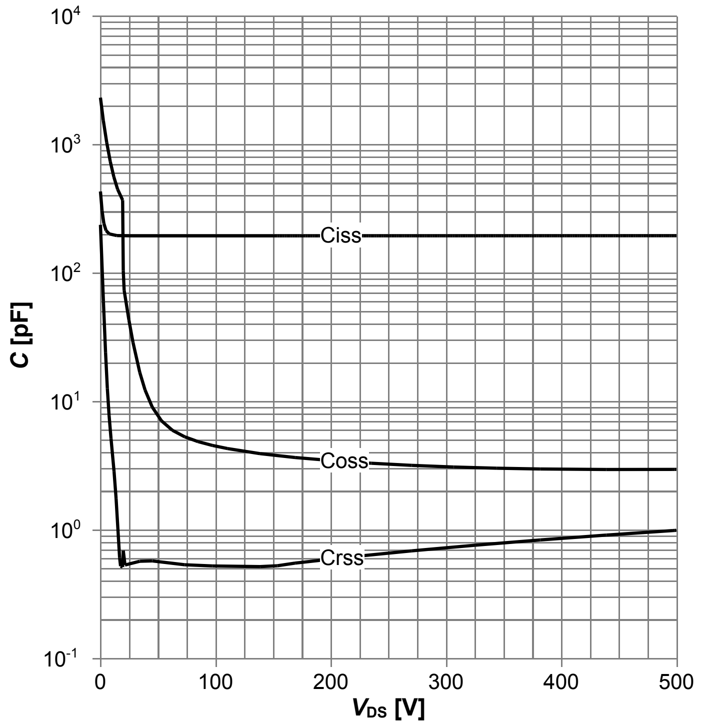
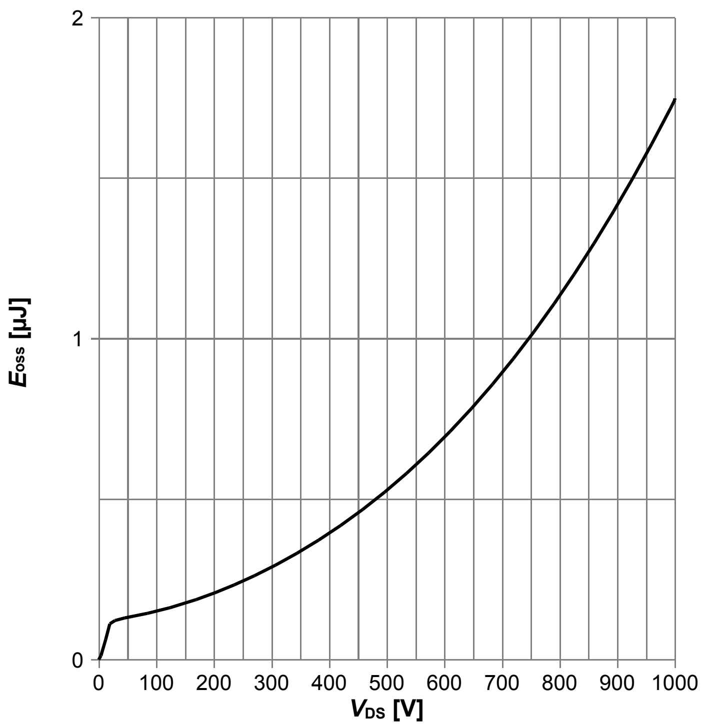
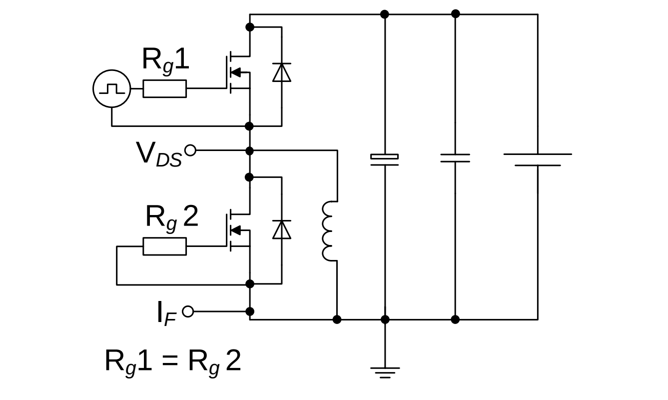
Diagram 13: Drain-source breakdown voltage	Diagram 14: Typ. capacitances
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy

E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

Test circuit for diode characteristics	Diode recovery waveform



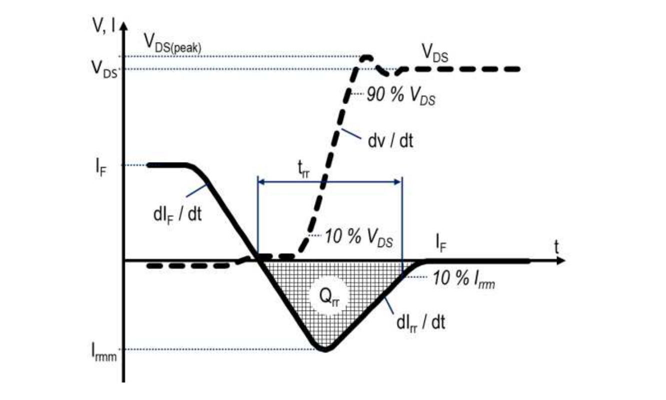
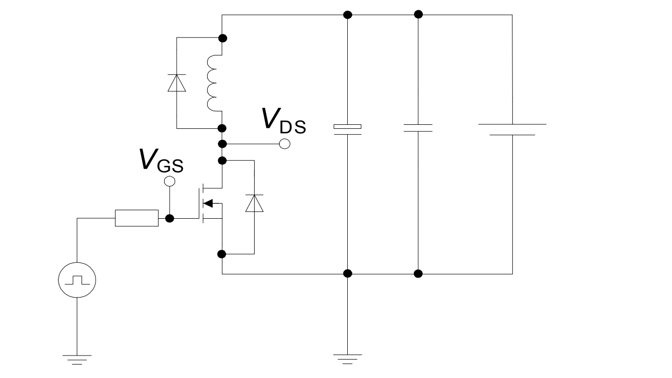


Table 9 Switching times

Switching times test circuit for inductive load	Switching times waveform



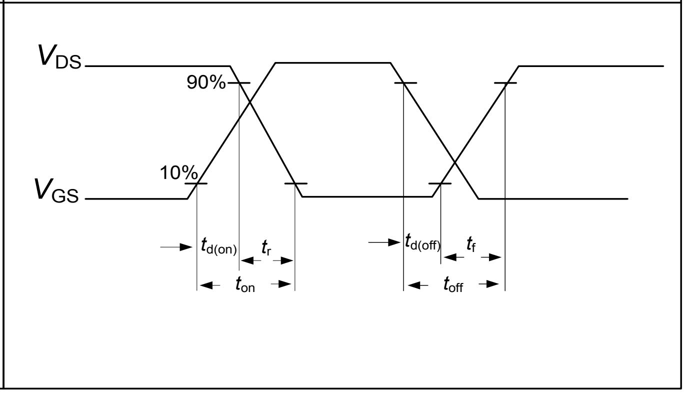
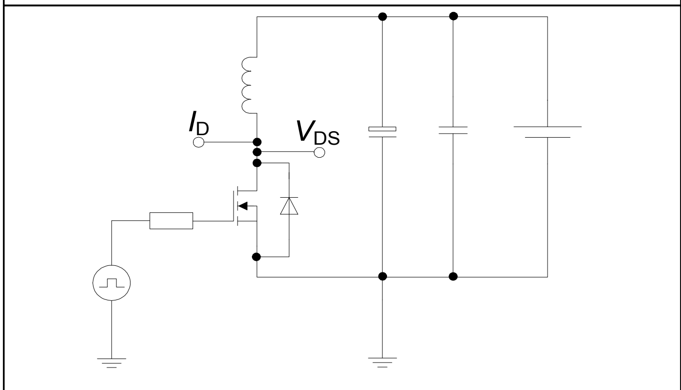
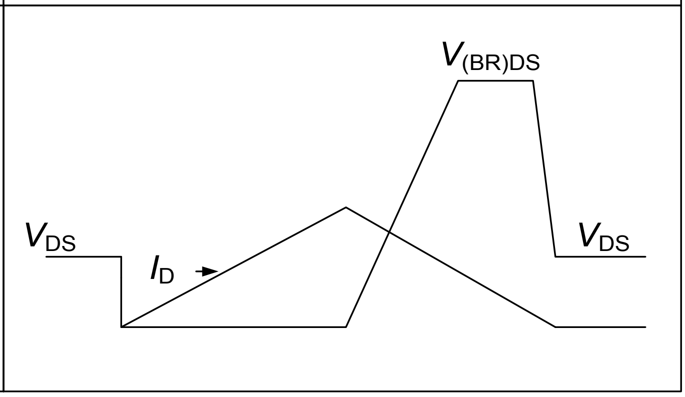


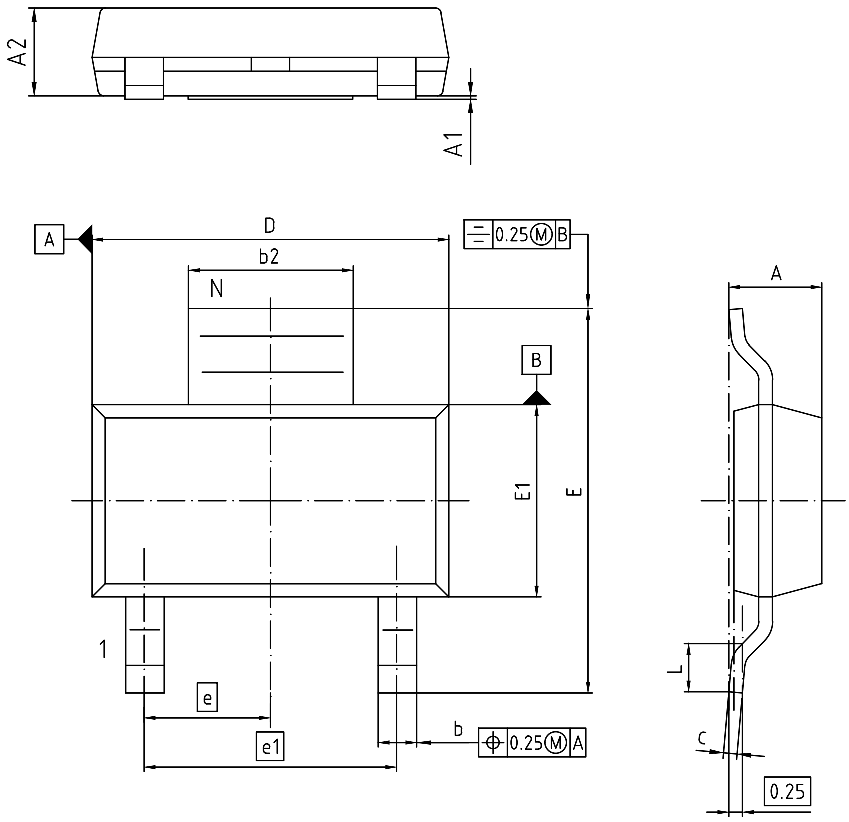
Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform





6 Package Outlines



NOTES:
1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-261

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	1.80	0.060	0.071
A1	-	0.10	-	0.004
A2	1,50	1.70	0.059	0.067
b	0.60	0.80	0.024	0.031
b2	2.95	3.10	0.116	0.122
c	0.24	0.32	0.009	0.013
D	6.30	6.70	0.248	0.264
E	6.70	7.30	0.264	0.287
E1	3.30	3.70	0.130	0.146
e	2.3 BASIC		0.091 BASIC	
e1	4.6 BASIC		0.181 BASIC	
L	0.75	1.10	0.030	0.043
N	3		3	
O	0°	10°	0°	10°

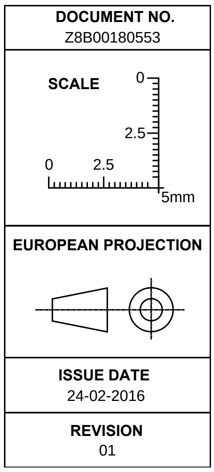


Figure 1 Outline PG-SOT223, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS P7 Webpage:** www.infineon.com
- **IFX CoolMOS P7 application note:** www.infineon.com
- **IFX CoolMOS P7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPN95R3K7P7

Revision: 2018-06-01, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2018-06-01	Release of final version

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