

OptiMOS[®]-T2 Power-Transistor

Product Summary

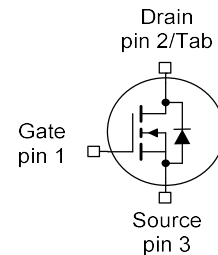
V_{DS}	100	V
$R_{DS(on),max}$ (SMD version)	5.0	m Ω
I_D	120	A

Features

- N-channel - Normal Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% Avalanche tested



Type	Package	Marking
IPB120N10S4-05	PG-TO263-3-2	4N1005
IPI120N10S4-05	PG-TO262-3-1	4N1005
IPP120N10S4-05	PG-TO220-3-1	4N1005


Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25^\circ\text{C}, V_{GS}=10\text{V}^{(1)}$	120	A
		$T_C=100^\circ\text{C}, V_{GS}=10\text{V}^{(2)}$	95	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	$T_C=25^\circ\text{C}$	480	
Avalanche energy, single pulse ⁽²⁾	E_{AS}	$I_D=60\text{A}$	330	mJ
Avalanche current, single pulse	I_{AS}	-	120	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation	P_{tot}	$T_C=25^\circ\text{C}$	190	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	$^\circ\text{C}$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	0.8	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=120\mu A$	2.0	2.7	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	0.1	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=100A$	-	4.5	5.3	m Ω
		$V_{GS}=10V, I_D=100A, \text{SMD version}$	-	4.2	5.0	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	5030	6540	pF
Output capacitance	C_{oss}		-	1600	2080	
Reverse transfer capacitance	C_{rss}		-	100	200	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V,$ $I_D=120A, R_G=3.5\Omega$	-	15	-	ns
Rise time	t_r		-	10	-	
Turn-off delay time	$t_{d(off)}$		-	30	-	
Fall time	t_f		-	35	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=80V, I_D=120A,$ $V_{GS}=0 \text{ to } 10V$	-	24	31	nC
Gate to drain charge	Q_{gd}		-	14	28	
Gate charge total	Q_g		-	70	91	
Gate plateau voltage	$V_{plateau}$		-	4.9	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	120	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	480	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=100A,$ $T_j=25^\circ C$	-	1.0	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=50V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	65	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	130	-	nC

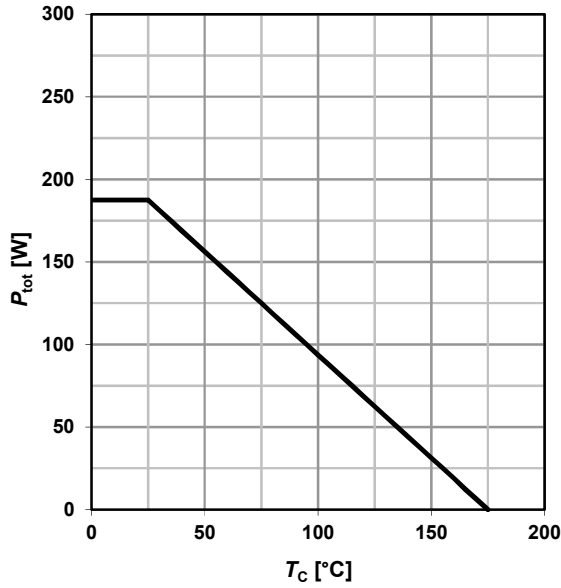
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.8K/W$ the chip is able to carry 134A at 25°C.

²⁾ Specified by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

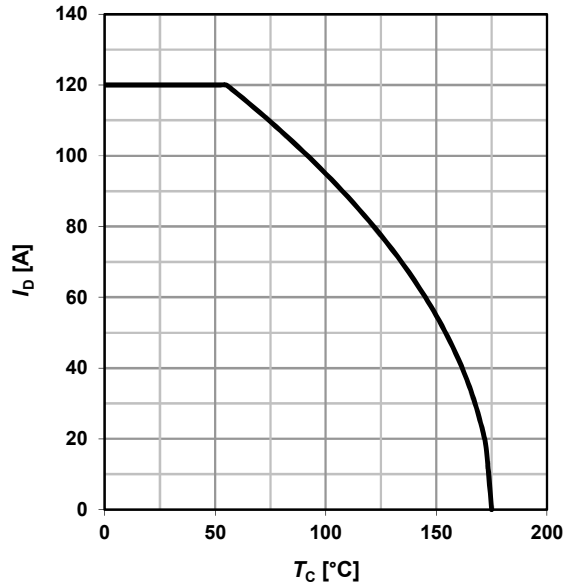
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} = 10\text{ V}$



2 Drain current

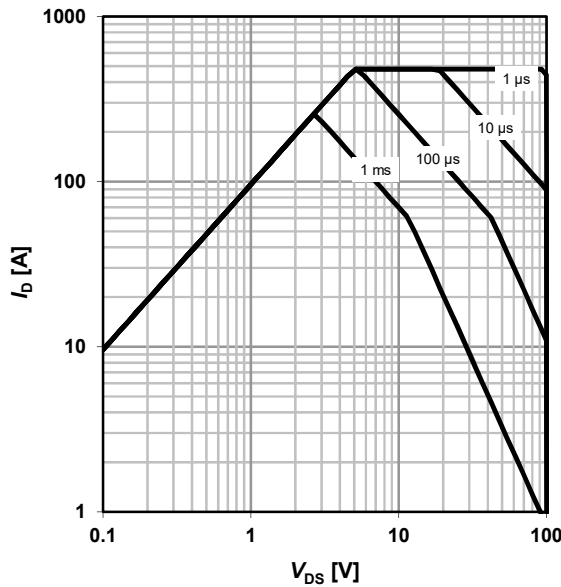
$I_D = f(T_C); V_{GS} = 10\text{ V}; \text{SMD}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0; \text{SMD}$

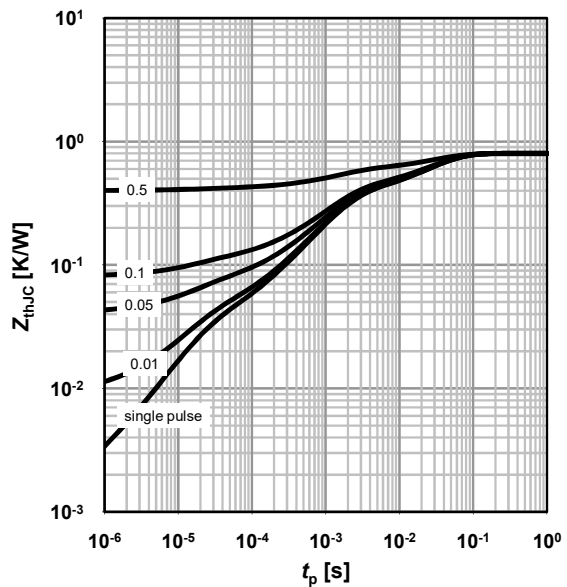
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

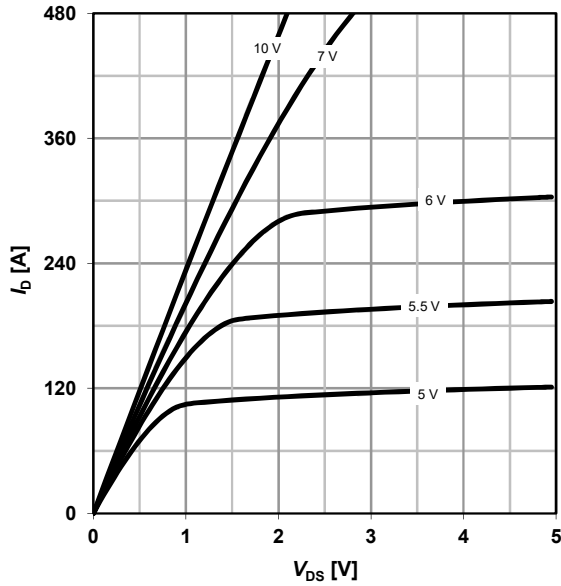
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}; \text{SMD}$

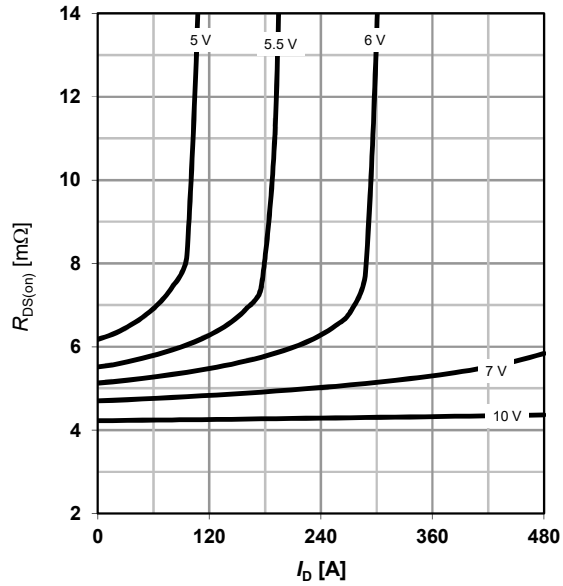
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}; \text{SMD}$

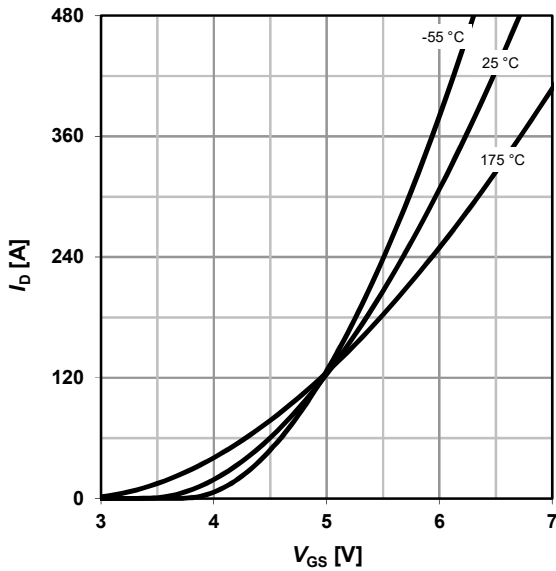
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{V}$

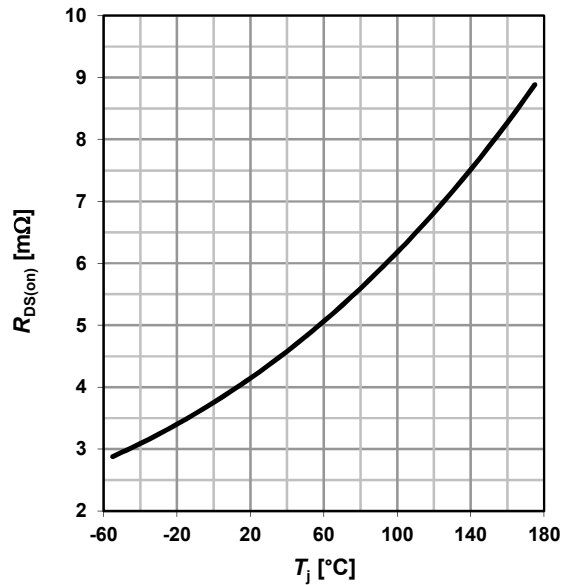
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); I_D = 100\text{ A}; V_{GS} = 10\text{ V}; \text{SMD}$

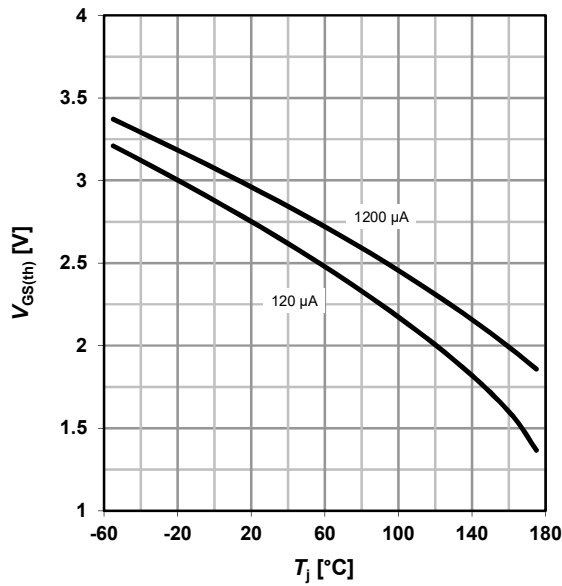
$\alpha = 0.4$



9 Typ. gate threshold voltage

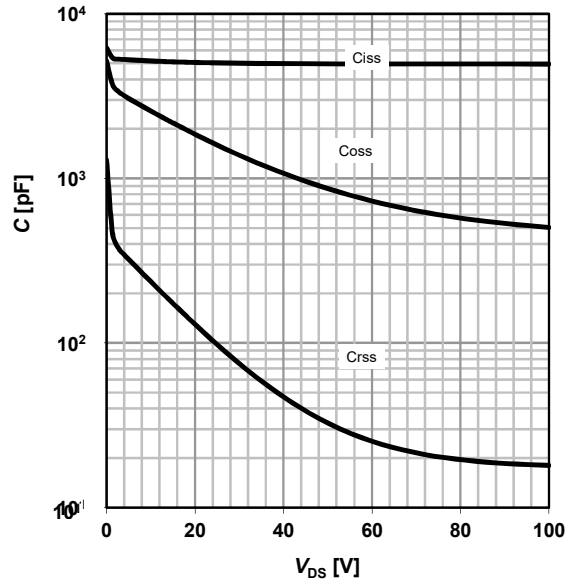
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

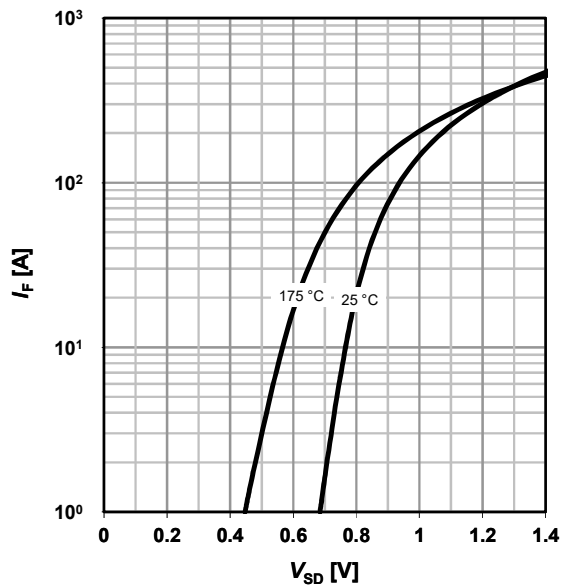
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

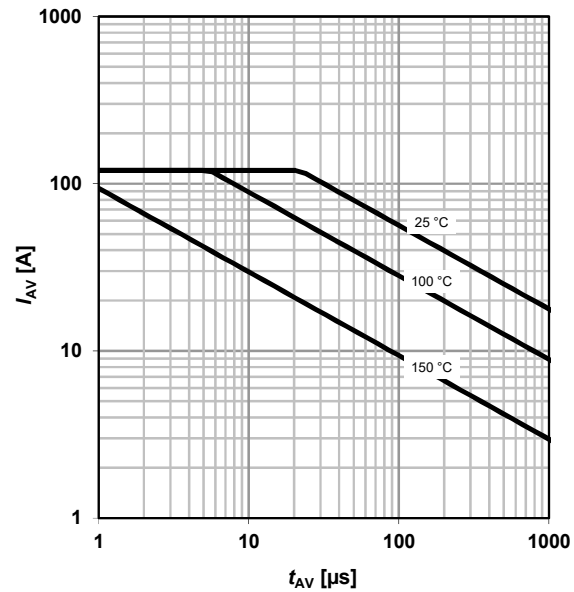
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

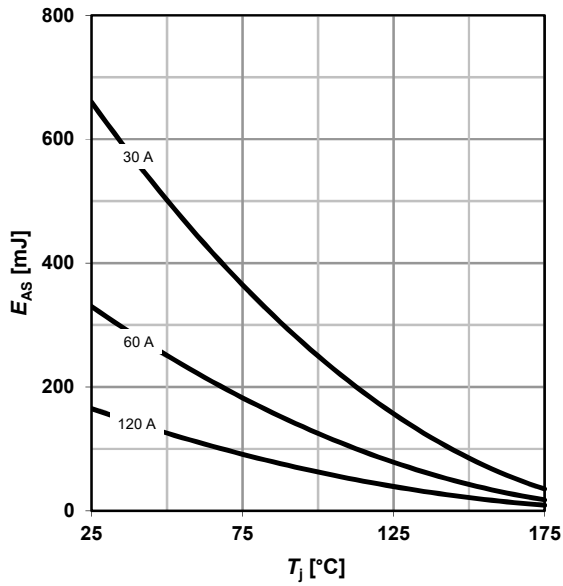
parameter: $T_{j(start)}$



13 Avalanche energy

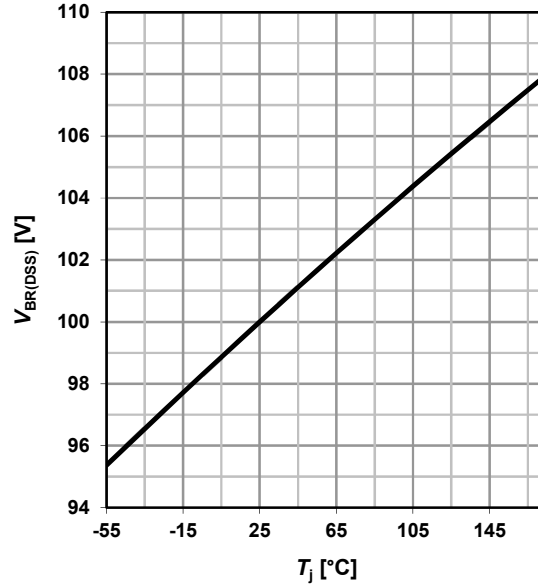
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

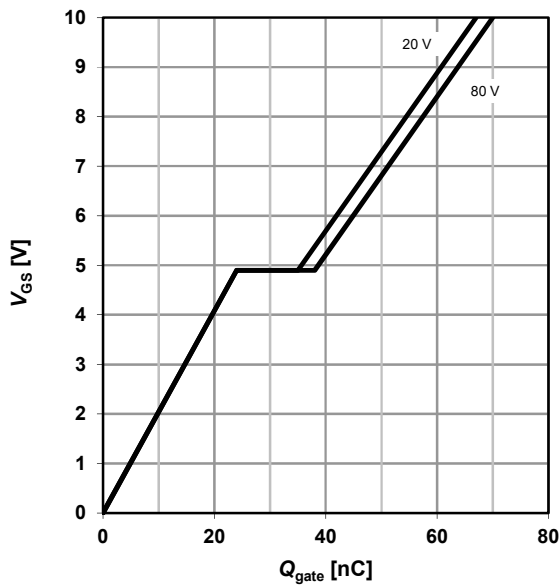
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



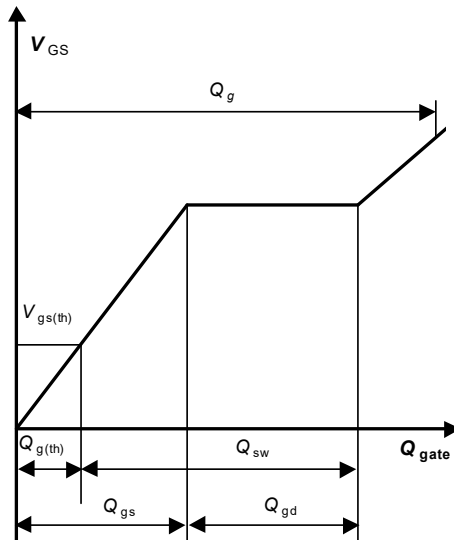
15 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = 120 \text{ A pulsed}$

parameter: V_{DD}

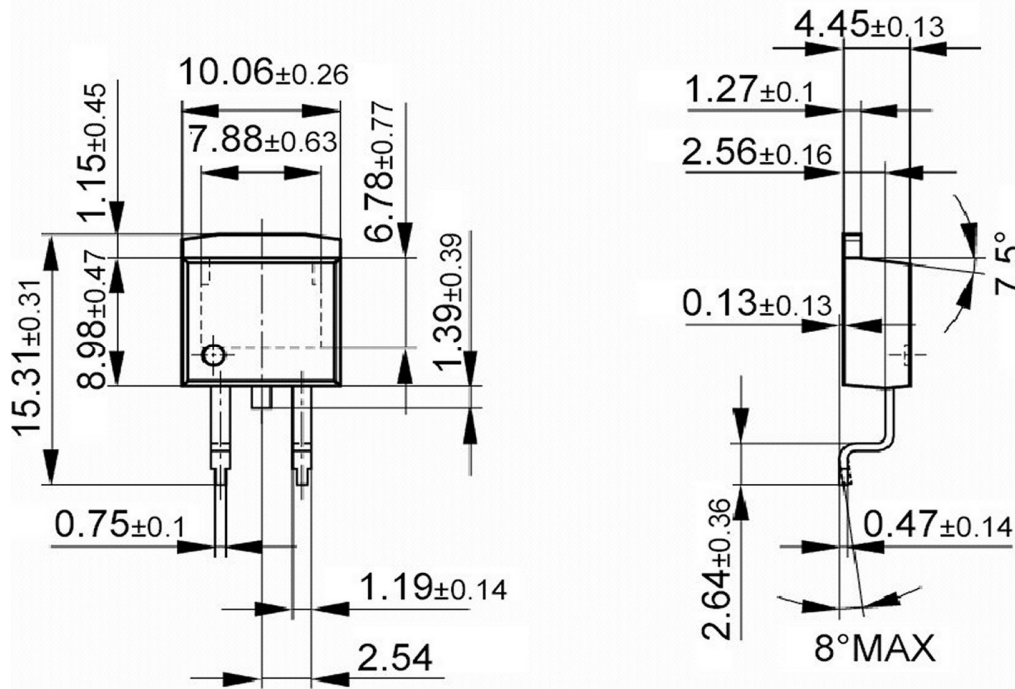


16 Gate charge waveforms

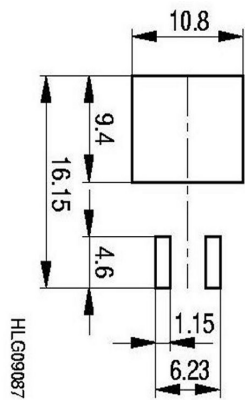


Package Outline

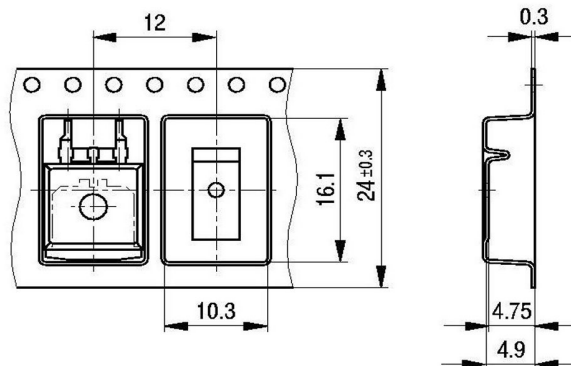
P-TO263-3-2: Outline



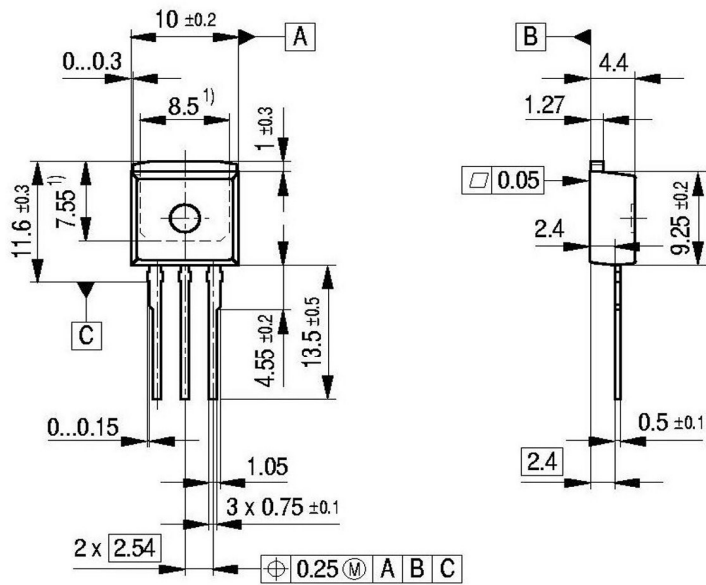
Footprint



Packaging

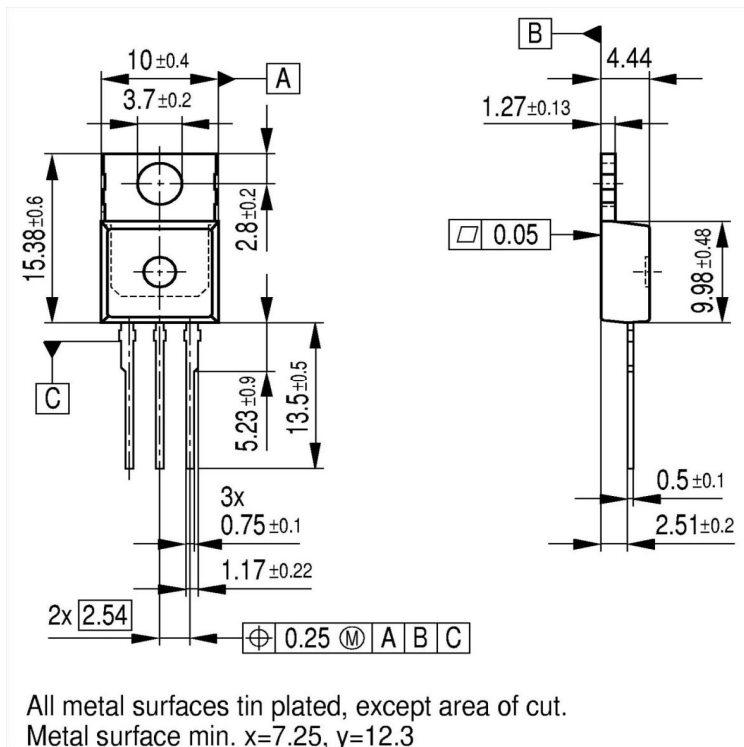


P-TO262-3-1: Outline



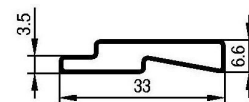
1) Typical
 Metal surface min. X = 7.25, Y = 6.9
 All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.
 Metal surface min. x=7.25, y=12.3

Packaging



Dimensions in mm

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Revision History

Version	Date	Changes
Revision 1.0	2014-07-01	Data Sheet Revision 1.0
Revision 1.1	2022-07-28	Diagram 8 Typ. drain-source on-state resistance: used α value clarified