

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ P6

600V CoolMOS™ P6 Power Transistor
IPx60R099P6

Data Sheet

Rev. 2.1
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

Features

- Increased MOSFET dv/dt ruggedness
- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

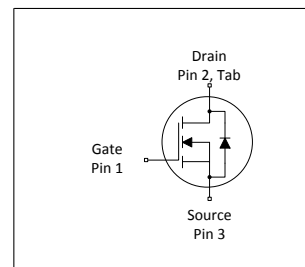
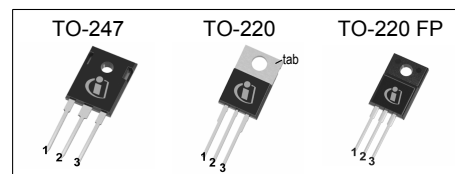


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	99	mΩ
$Q_{g,typ}$	70	nC
$I_{D,pulse}$	109	A
$E_{oss@400V}$	8.8	μJ
Body diode di/dt	300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPW60R099P6	PG-TO 247	6R099P6	see Appendix A
IPP60R099P6	PG-TO 220		
IPA60R099P6	PG-TO 220 FullPAK		

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	37.9 24.0	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	109	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	796	mJ	$I_D=6.6\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	1.21	mJ	$I_D=6.6\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, repetitive	I_{AR}	-	-	6.6	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation (Non FullPAK) TO-220, TO-247	P_{tot}	-	-	278	W	$T_C=25^\circ\text{C}$
Power dissipation (FullPAK) TO-220FP	P_{tot}	-	-	34	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque (Non FullPAK) TO-220, TO-247	-	-	-	60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220FP	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	32.9	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	109	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage for TO-220FP	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.75$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

3 Thermal characteristics

Table 3 Thermal characteristics (Non FullPAK) TO-220, TO-247

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.45	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics (FullPAK) TO-220FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.65	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3.5	4.0	4.5	V	$V_{DS}=V_{GS}$, $I_D=1.21\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	5	μA	$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.089 0.232	0.099 -	Ω	$V_{GS}=10\text{V}$, $I_D=14.5\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=14.5\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1	-	Ω	$f=1\text{MHz}$, open drain

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	3330	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Output capacitance	C_{oss}	-	140	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=100\text{V}$, $f=1\text{MHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	110	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	495	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	20	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=18.1\text{A}$, $R_G=1.7\Omega$; see table 9
Rise time	t_r	-	10	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=18.1\text{A}$, $R_G=1.7\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	50	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=18.1\text{A}$, $R_G=1.7\Omega$; see table 9
Fall time	t_f	-	5	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=18.1\text{A}$, $R_G=1.7\Omega$; see table 9

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	20	-	nC	$V_{DD}=400\text{V}$, $I_D=18.1\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	24	-	nC	$V_{DD}=400\text{V}$, $I_D=18.1\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	70	-	nC	$V_{DD}=400\text{V}$, $I_D=18.1\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	$V_{DD}=400\text{V}$, $I_D=18.1\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=18.1A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	470	-	ns	$V_R=400V$, $I_F=18.1A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	9	-	μC	$V_R=400V$, $I_F=18.1A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	37	-	A	$V_R=400V$, $I_F=18.1A$, $di_F/dt=100A/\mu s$; see table 8

5 Electrical characteristics diagrams

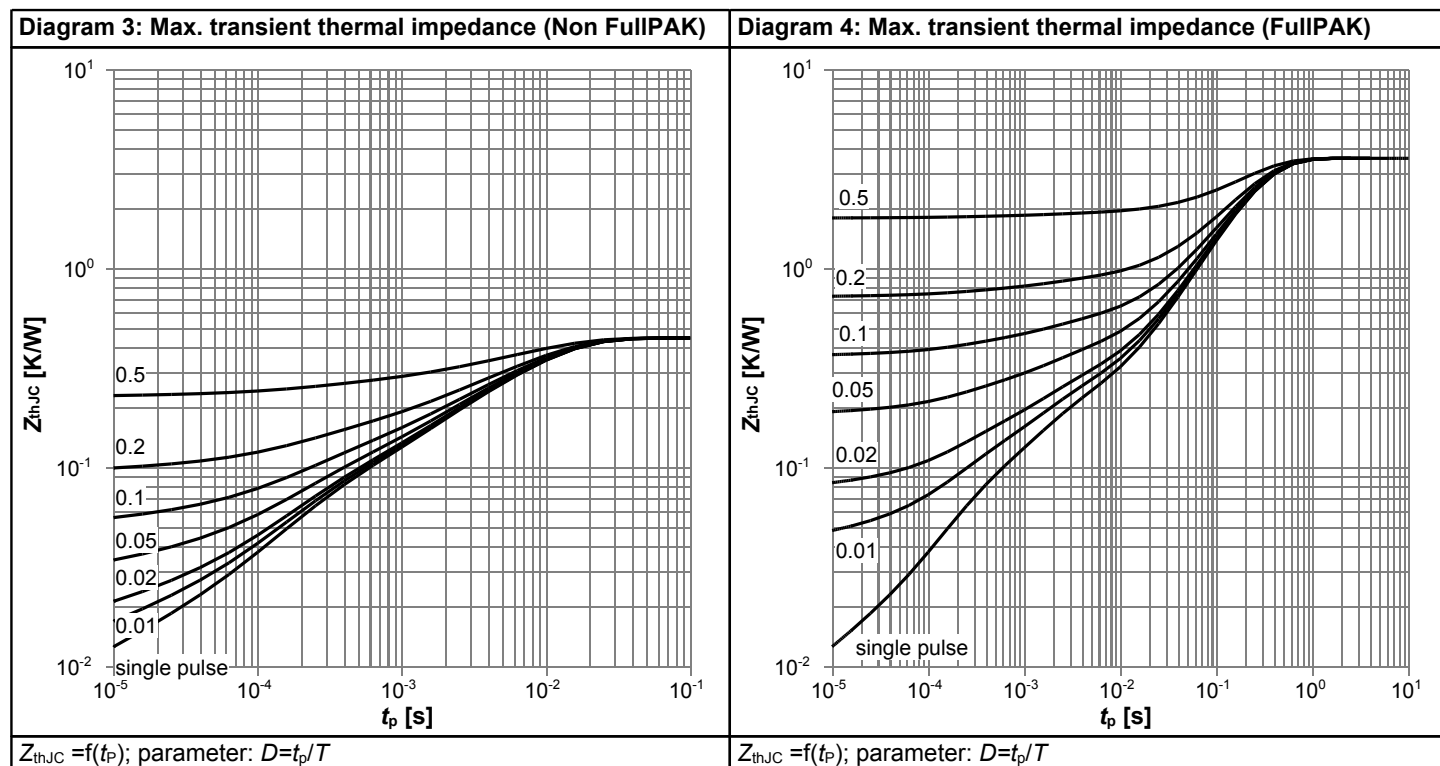
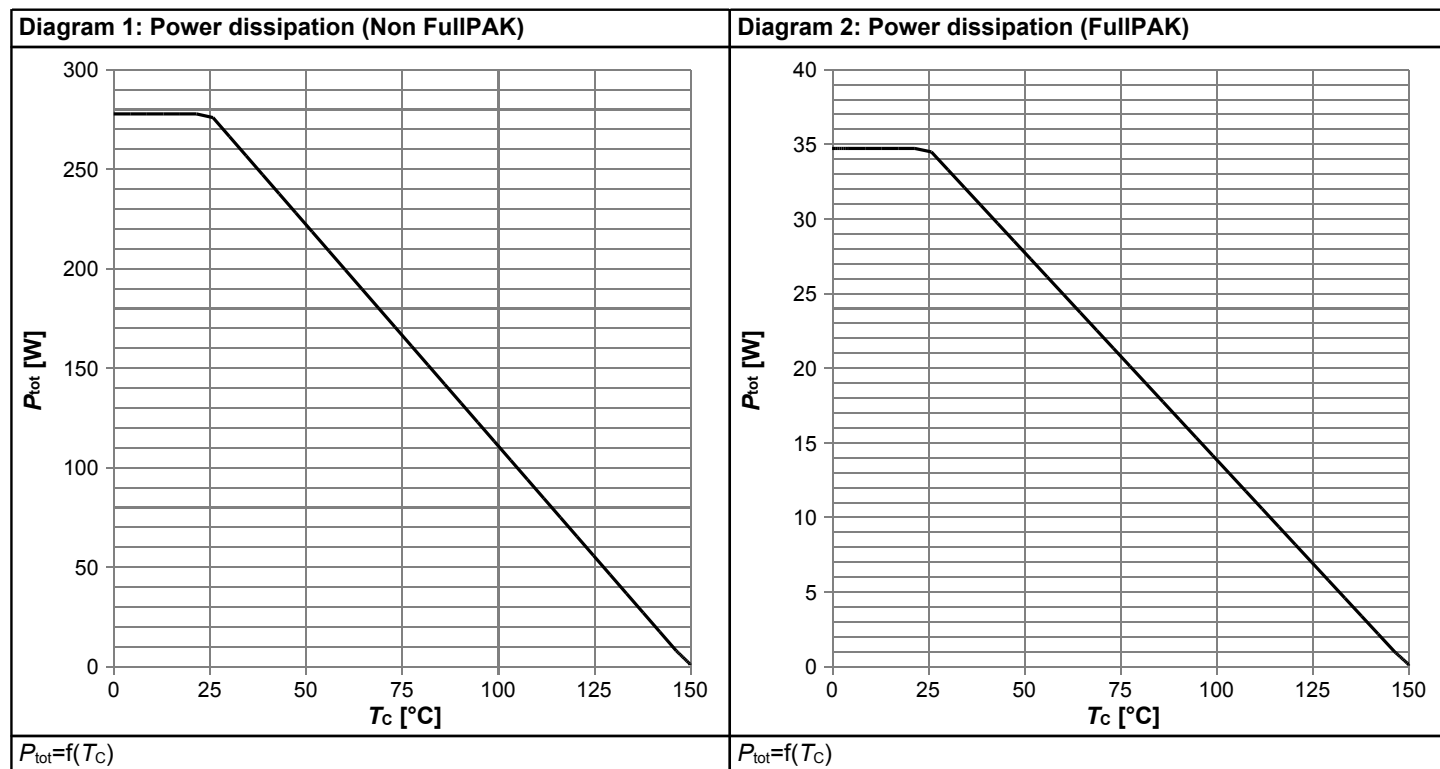
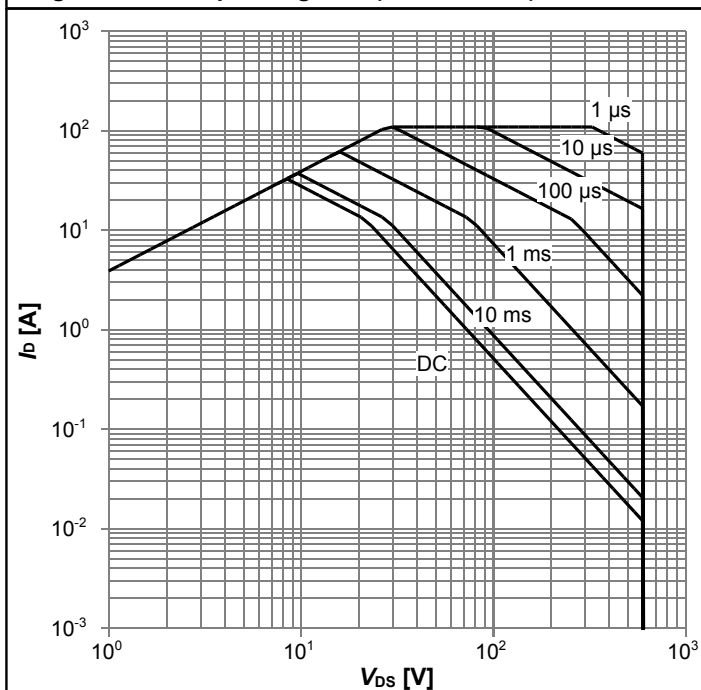
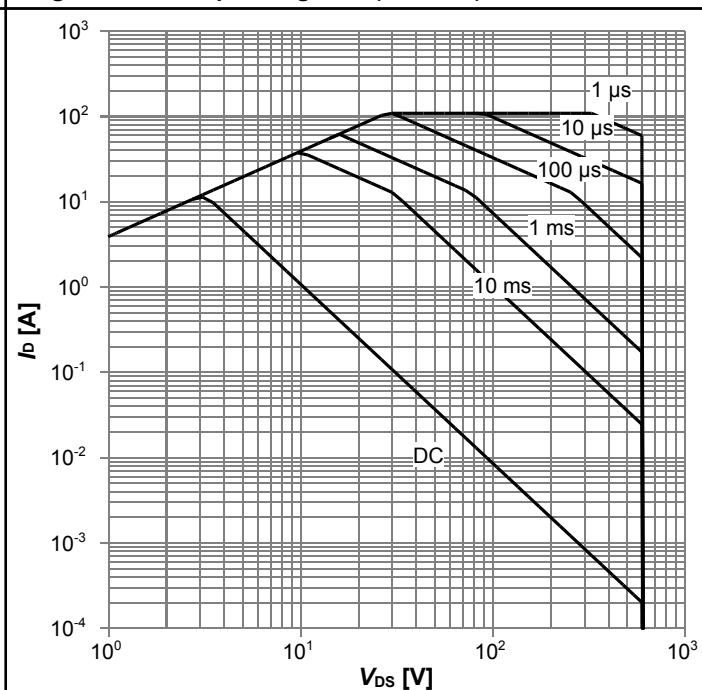


Diagram 5: Safe operating area (Non FullPAK)



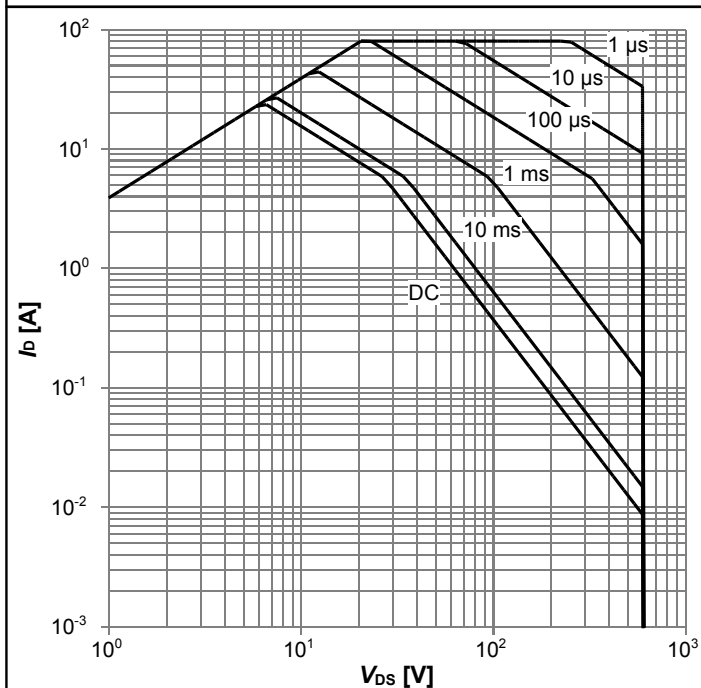
$I_D=f(V_{DS})$; $T_C=25\text{ °C}$; $D=0$; parameter: t_p

Diagram 6: Safe operating area (FullPAK)



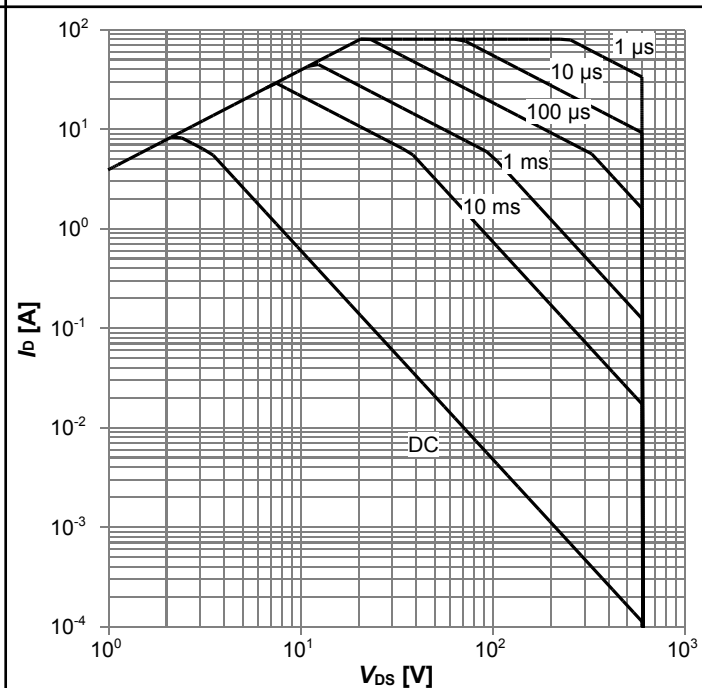
$I_D=f(V_{DS})$; $T_C=25\text{ °C}$; $D=0$; parameter: t_p

Diagram 7: Safe operating area (Non FullPAK)



$I_D=f(V_{DS})$; $T_C=80\text{ °C}$; $D=0$; parameter: t_p

Diagram 8: Safe operating area (FullPAK)



$I_D=f(V_{DS})$; $T_C=80\text{ °C}$; $D=0$; parameter: t_p

Diagram 9: Typ. output characteristics

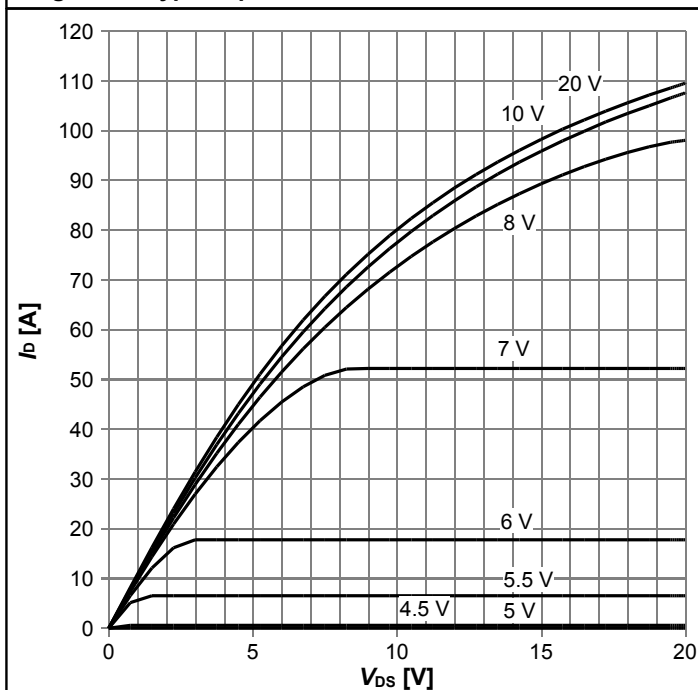

 $I_D = f(V_{DS}); T_J = 25^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 10: Typ. output characteristics

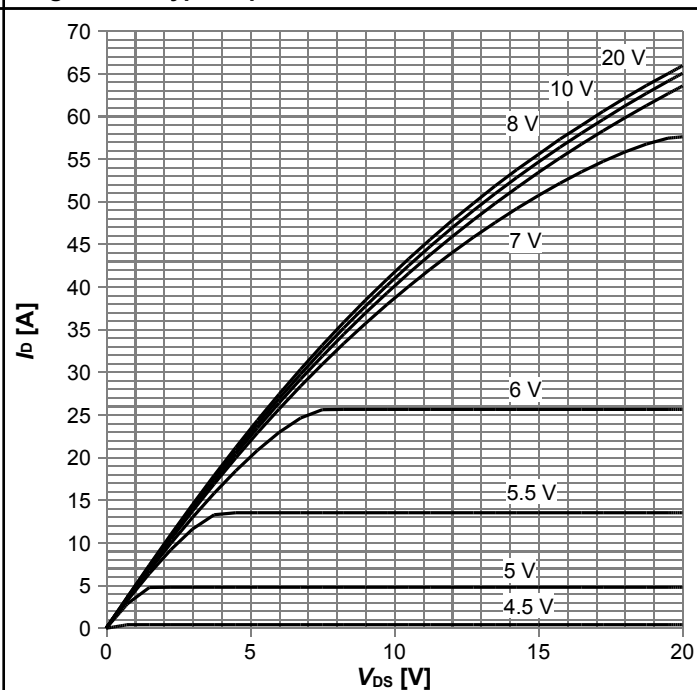

 $I_D = f(V_{DS}); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 11: Typ. drain-source on-state resistance

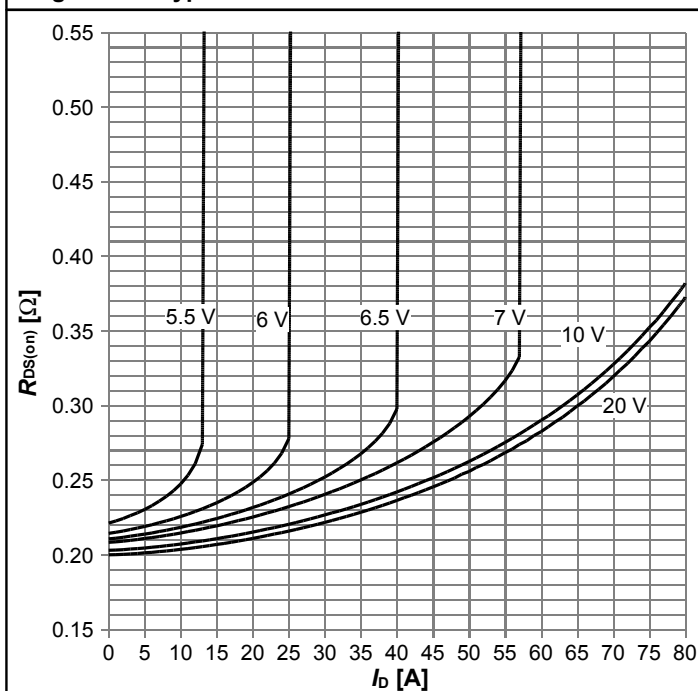

 $R_{DS(on)} = f(I_D); T_J = 125^\circ\text{C}; \text{parameter: } V_{GS}$

Diagram 12: Drain-source on-state resistance

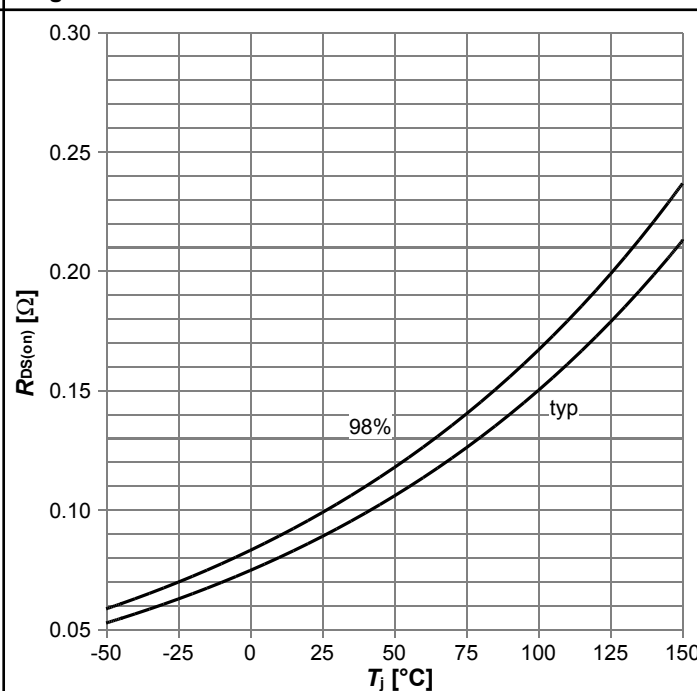

 $R_{DS(on)} = f(T_J); I_D = 14.5\text{ A}; V_{GS} = 10\text{ V}$

Diagram 13: Typ. transfer characteristics

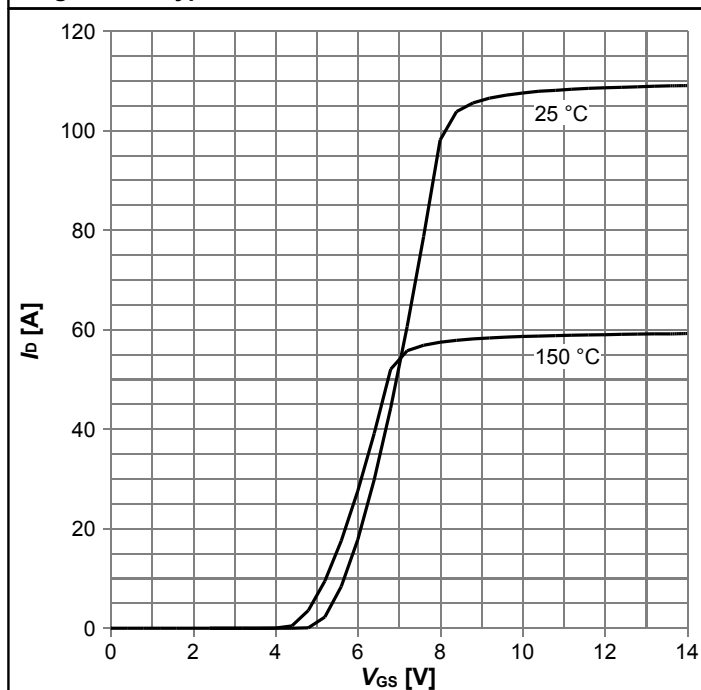

 $I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

Diagram 14: Typ. gate charge

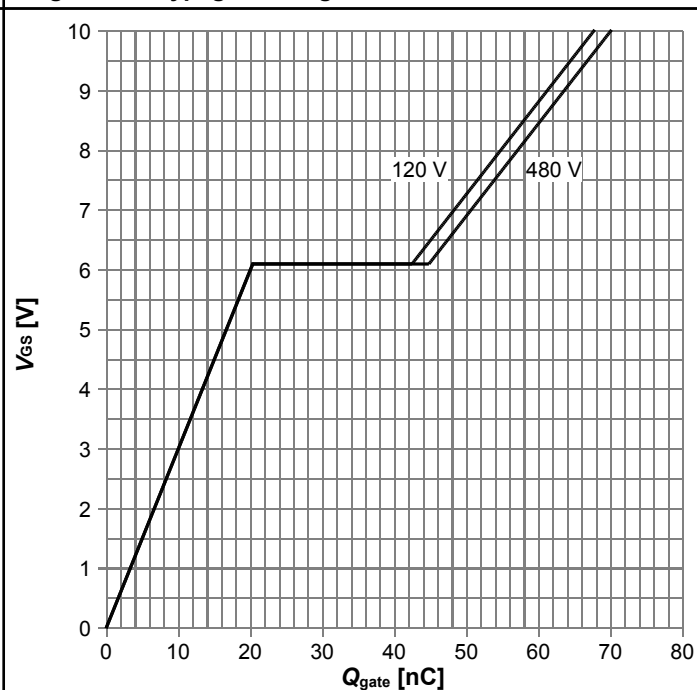

 $V_{GS} = f(Q_{gate}); I_D = 18.1 \text{ A pulsed}; \text{parameter: } V_{DD}$

Diagram 15: Forward characteristics of reverse diode

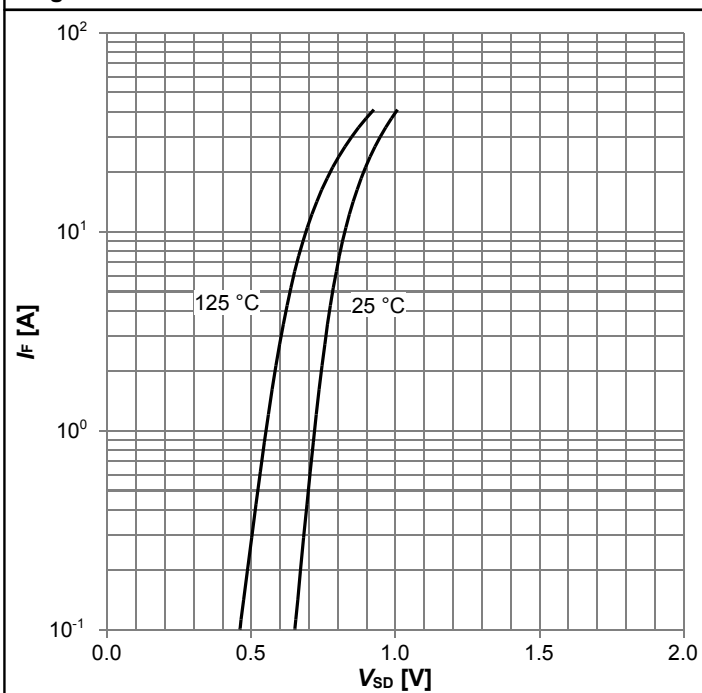

 $I_F = f(V_{SD}); \text{parameter: } T_j$

Diagram 16: Avalanche energy

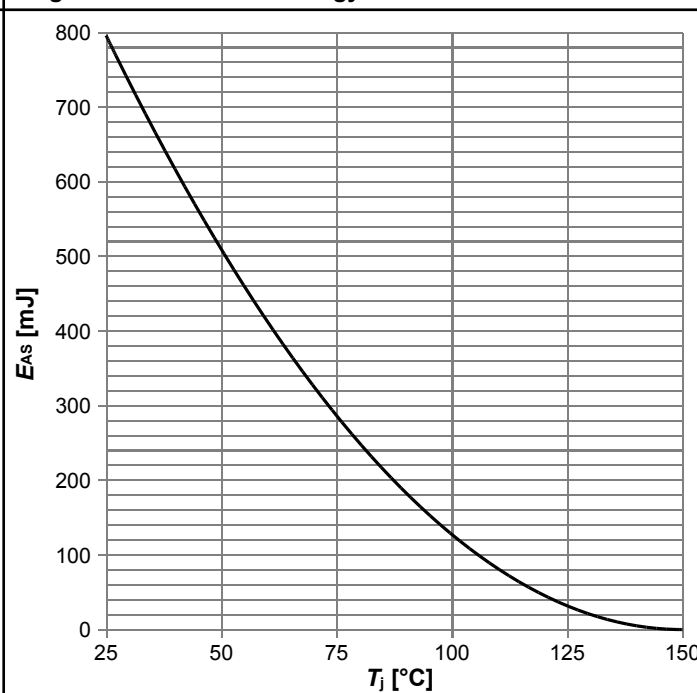
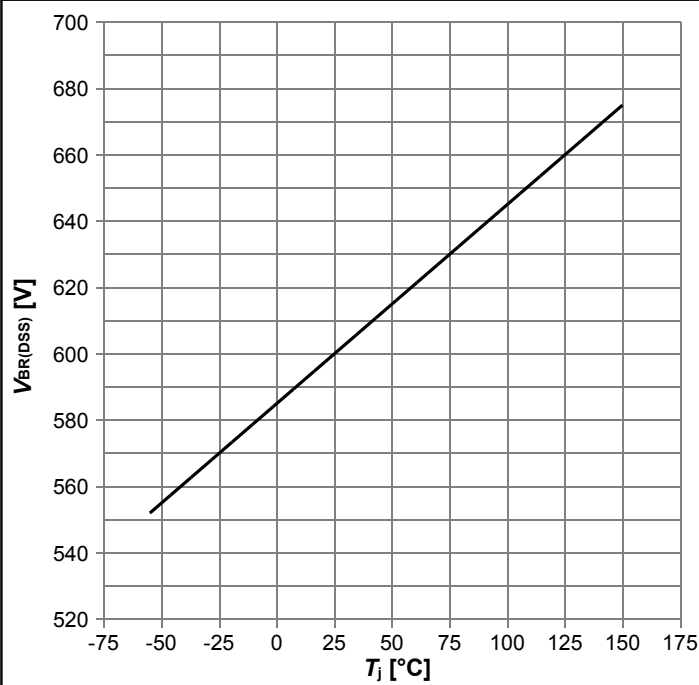
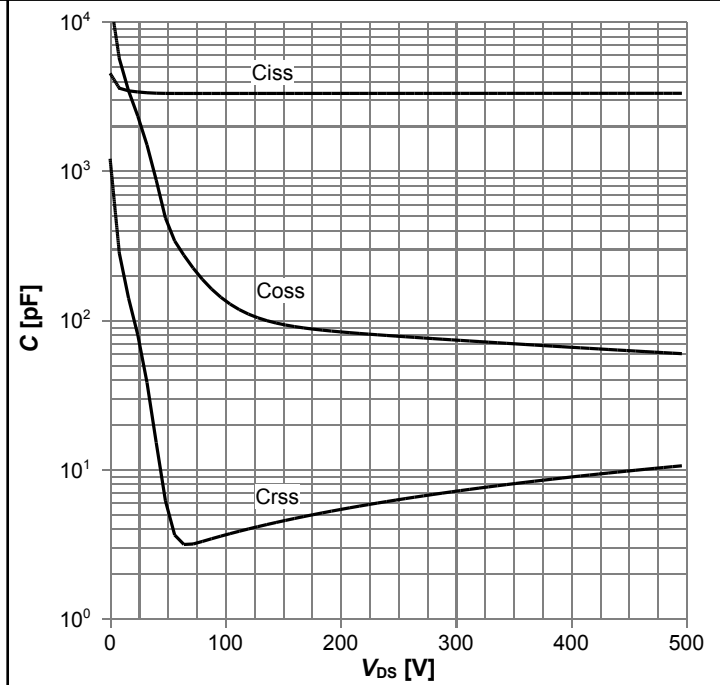

 $E_{AS} = f(T_j); I_D = 6.6 \text{ A}; V_{DD} = 50 \text{ V}$

Diagram 17: Drain-source breakdown voltage



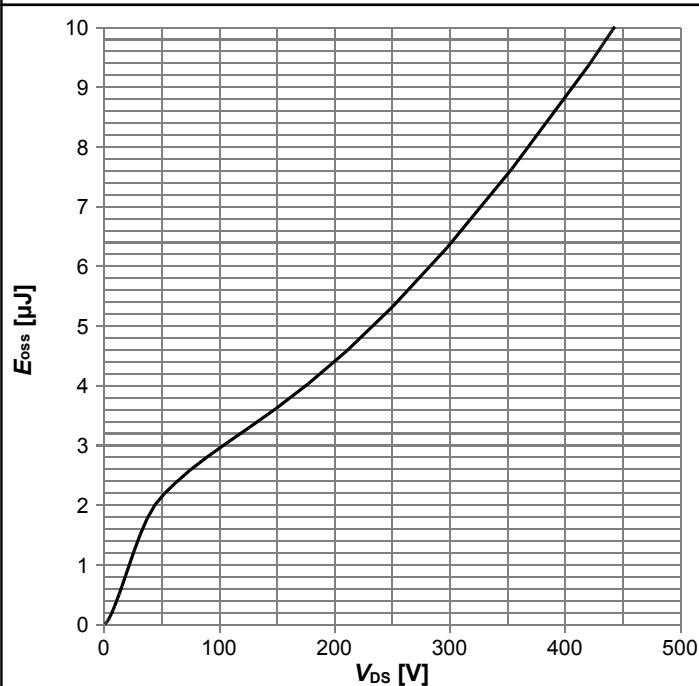
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$

Diagram 18: Typ. capacitances



$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 19: Typ. Coss stored energy



$$E_{oss} = f(V_{DS})$$

6 Test Circuits

Table 9 Diode characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$
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Table 10 Switching times

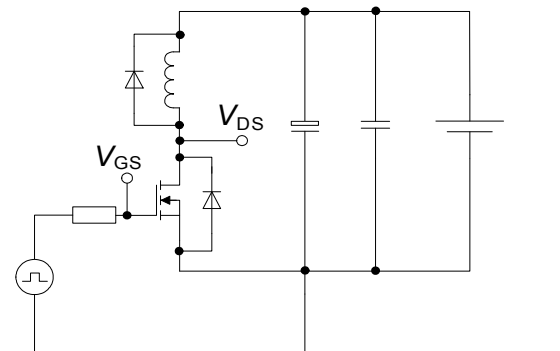
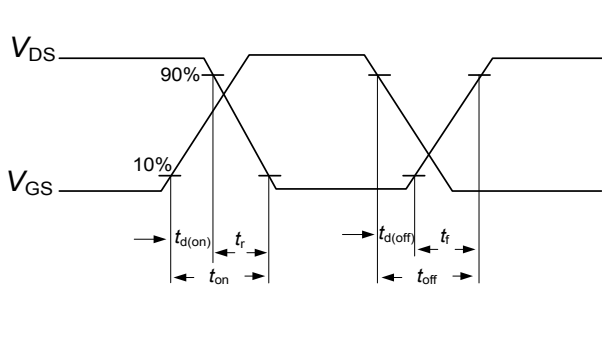
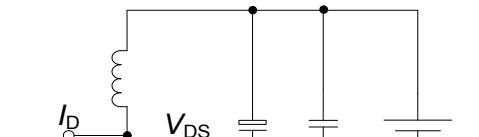
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a switching test setup for an inductive load. A MOSFET is driven by a pulse generator connected to its gate through a resistor. The gate voltage is labeled V_{GS}. The MOSFET's drain is connected to a DC source and an inductive load (represented by an inductor and a diode in parallel). The drain voltage is labeled V_{DS}. The load is connected to ground. The MOSFET's source is also connected to ground.	 The timing diagram shows the switching waveforms for V_{DS} and V_{GS}. The V_{GS} waveform is a square wave that transitions between a low level and a high level. The V_{DS} waveform shows the voltage across the MOSFET during these transitions. Key time intervals are labeled: $t_{d(on)}$ (delay to turn on), t_r (rise time), t_{on} (total turn-on time), $t_{d(off)}$ (delay to turn off), t_f (fall time), and t_{off} (total turn-off time). The V_{DS} waveform shows a 90% voltage level during the on-state and a 10% voltage level during the off-state.

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines

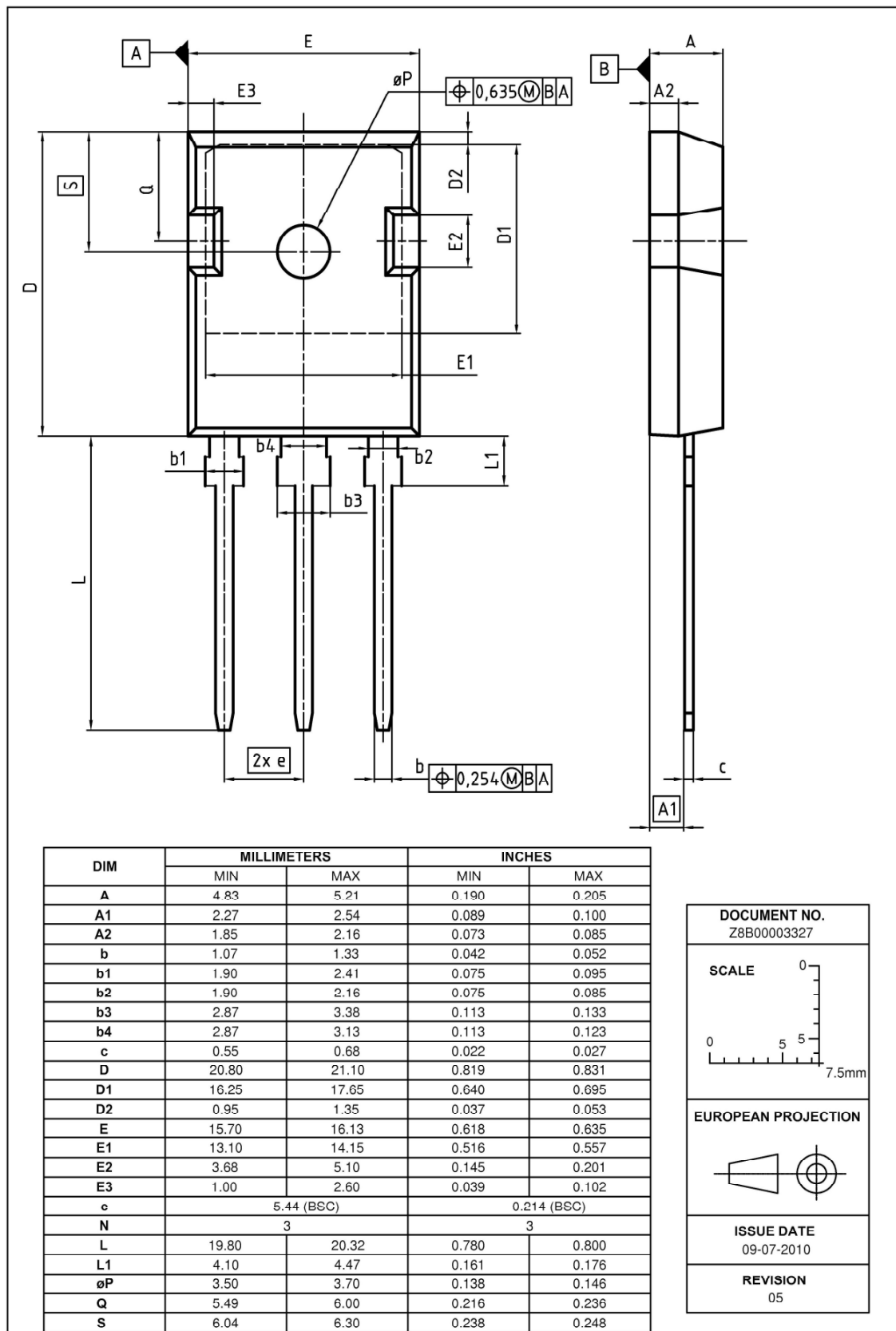


Figure 1 Outline PG-TO 247, dimensions in mm/inches

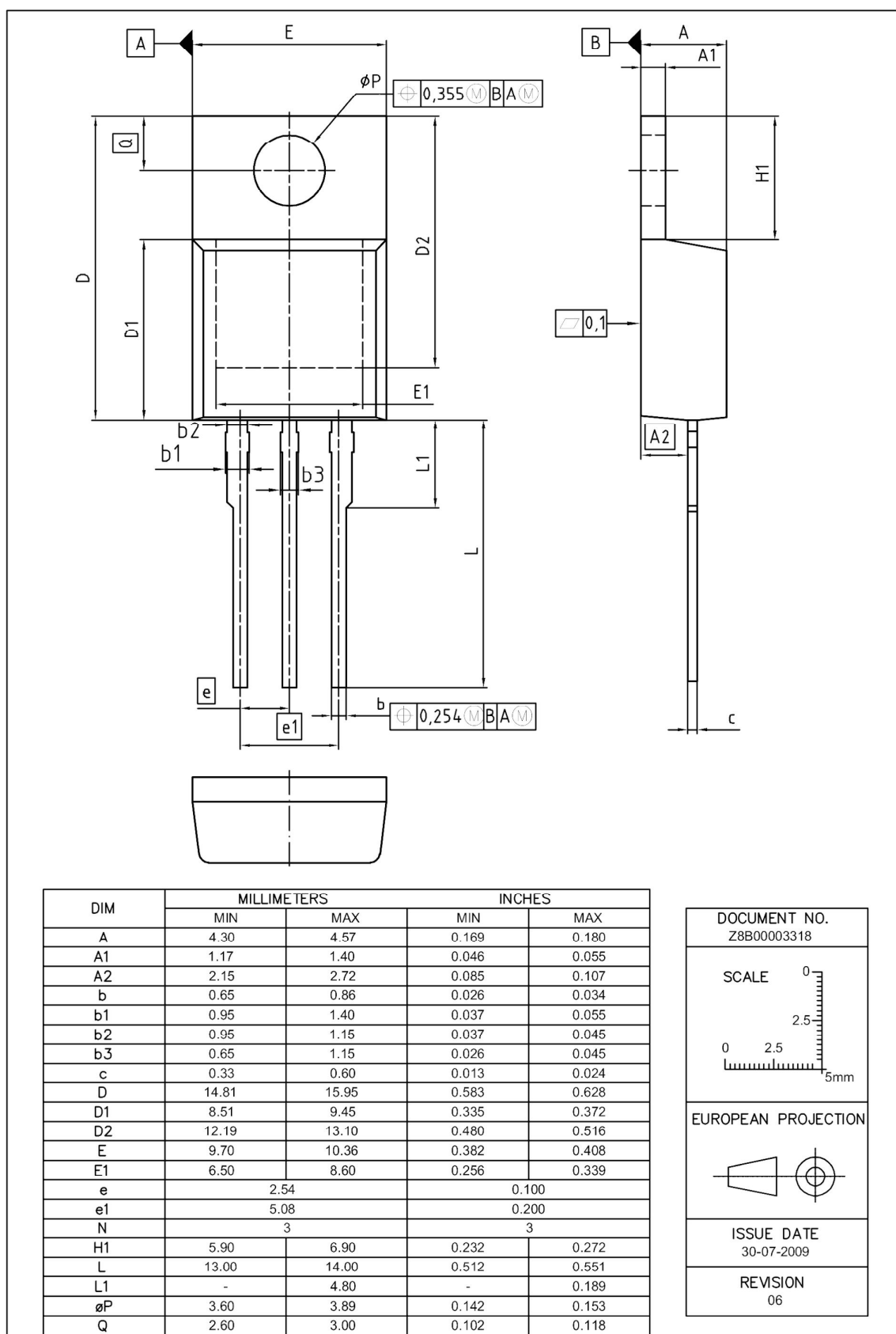
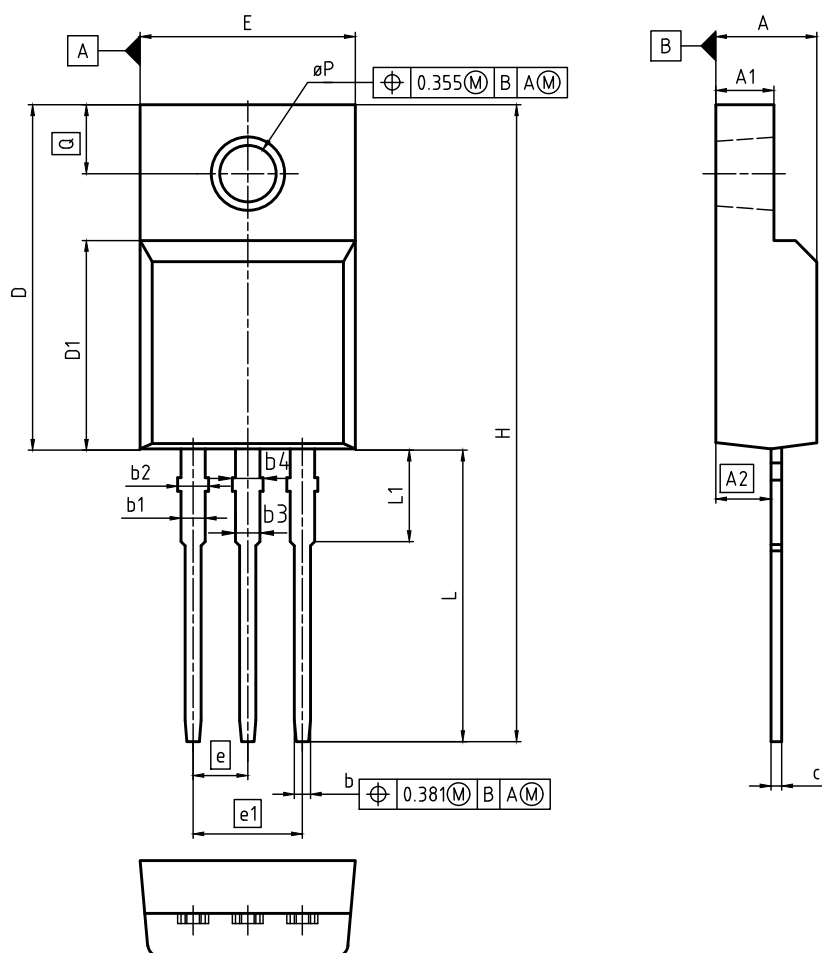


Figure 2 Outline PG-TO 220, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

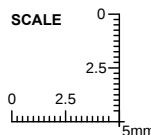
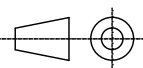
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EUROPEAN PROJECTION 	
ISSUE DATE 05-05-2014	
REVISION 04	

Figure 3 Outline PG-TO 220 FullPAK, dimensions in mm/inches

8 Appendix A

Table 12 Related Links

- IFX CoolMOS™ P6 Webpage: www.infineon.com
- IFX CoolMOS™ P6 application note: www.infineon.com
- IFX CoolMOS™ P6 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPW60R099P6, IPP60R099P6, IPA60R099P6

Revision: 2015-05-18, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2014-03-07	Release of final version
2.1	2015-05-18	Rdson max change from 105 to 99mOhm

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