OptiMOS™-T2 Power-Transistor

Product Summary

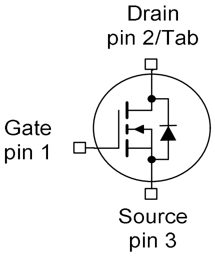
V_{DS}	80	V
$R_{DS(on),max}$ (SMD version)	5.5	mΩ
I_D	80	A

Features

- N-channel - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TO263-3-2	PG-TO262-3-1	PG-TO220-3-1
		

Type	Package	Marking
IPB80N08S4-06	PG-TO263-3-2	4N0806
IPI80N08S4-06	PG-TO262-3-1	4N0806
IPP80N08S4-06	PG-TO220-3-1	4N0806



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25°C, V_{GS}=10V[1]	80	A
		T_C=100°C, V_{GS}=10V[2]	80	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25°C	320	
Avalanche energy, single pulse[2]	E_{AS}	I_D=40A	270	mJ
Avalanche current, single pulse	I_{AS}	-	75	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25°C	150	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2)]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.0	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3)]	-	-	40	

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=90µA	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=80V, V_{GS}=0V	-	0.01	1	µA
		V_{DS}=80V, V_{GS}=0V, T_j=125°C[2)]	-	5	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=80A	-	5.0	5.8	mΩ
		V_{GS}=10V, I_D=80A, SMD version	-	4.7	5.5	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	3600	4800	pF
Output capacitance	C_{oss}		-	1400	1860	
Reverse transfer capacitance	C_{rss}		-	75	150	
Turn-on delay time	$t_{d(on)}$	V_{DD}=40V, V_{GS}=10V, I_D=80A, R_G=3.5Ω	-	12	-	ns
Rise time	t_r		-	7	-	
Turn-off delay time	$t_{d(off)}$		-	20	-	
Fall time	t_f		-	25	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=64V, I_D=80A, V_{GS}=0 to 10V	-	18	24	nC
Gate to drain charge	Q_{gd}		-	12	24	
Gate charge total	Q_g		-	52	70	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25°C	-	-	80	A
Diode pulse current[2]	$I_{S,pulse}$		-	-	320	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=80A, T_j=25°C	-	0.9	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=40V, I_F=50A, di_F/dt=100A/µs	-	90	-	ns
Reverse recovery charge[2]	Q_{rr}		-	60	-	nC

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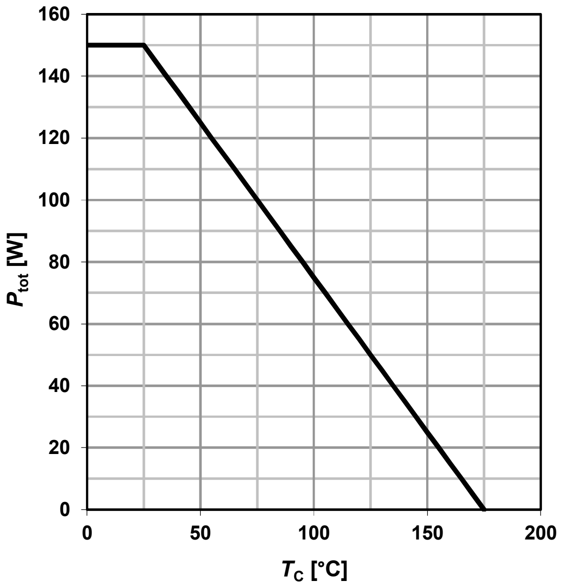
[1] Current is limited by bondwire; with an R_{thJC} = 1.0K/W the chip is able to carry 118A at 25°C.

[2] Specified by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

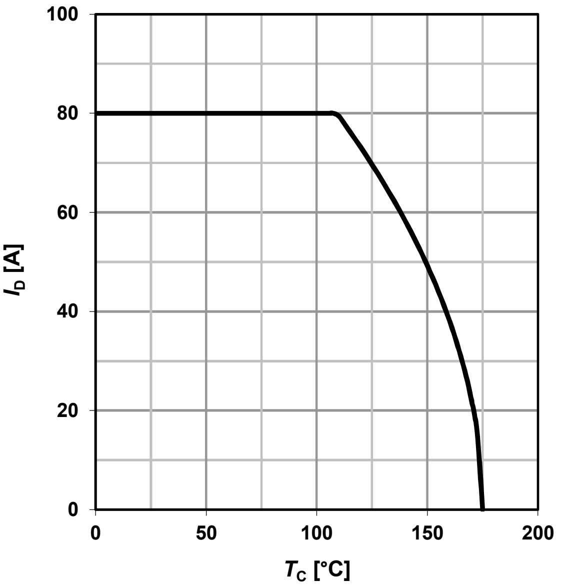
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

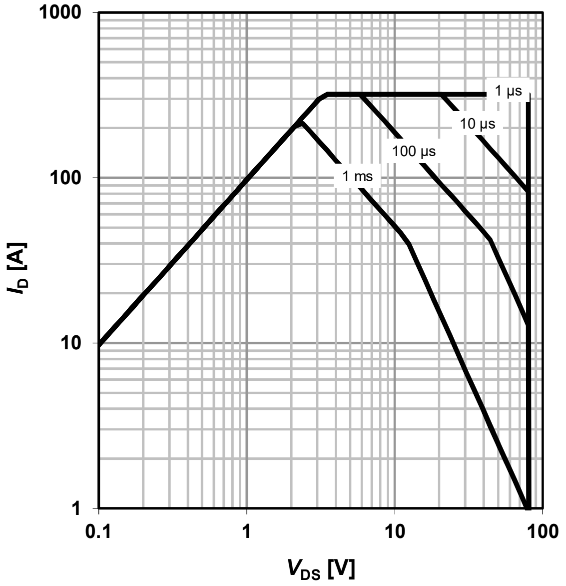
$I_D = f(T_C)$; $V_{GS} = 10$ V; SMD



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; SMD

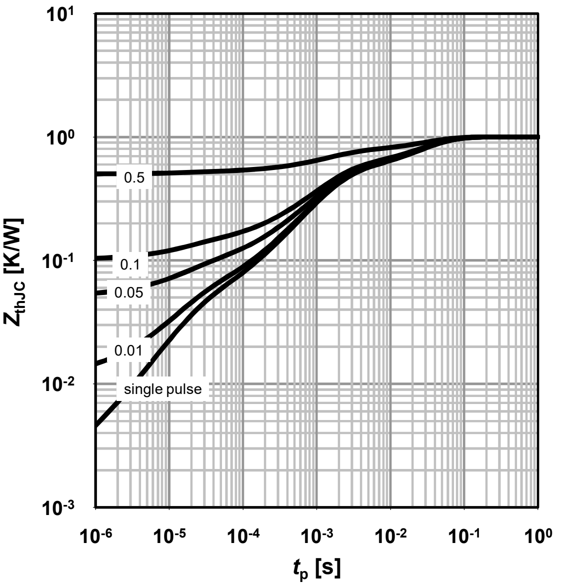
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

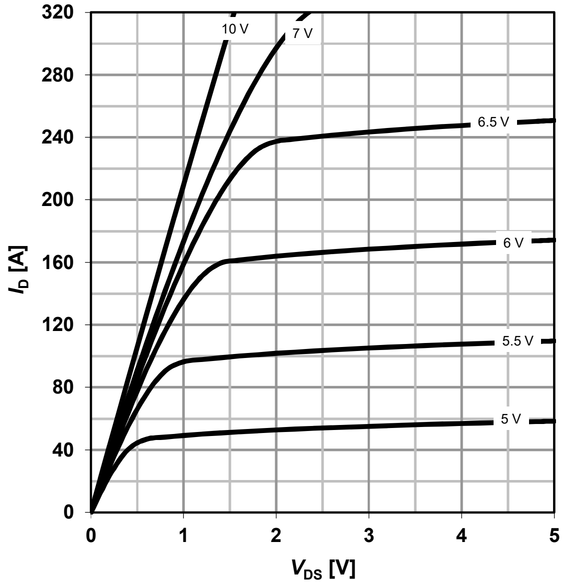
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; SMD

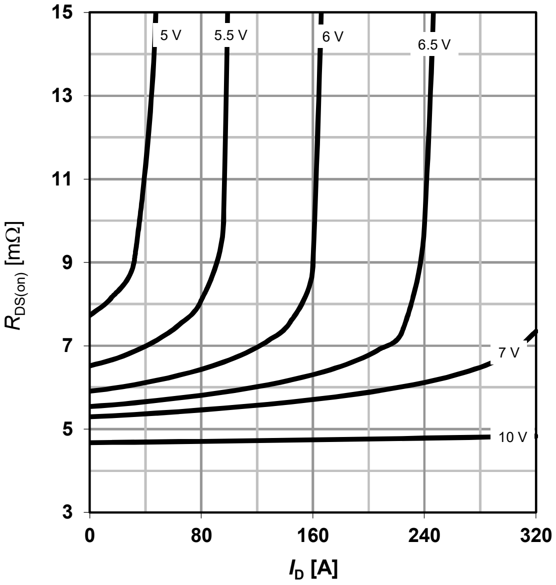
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; SMD

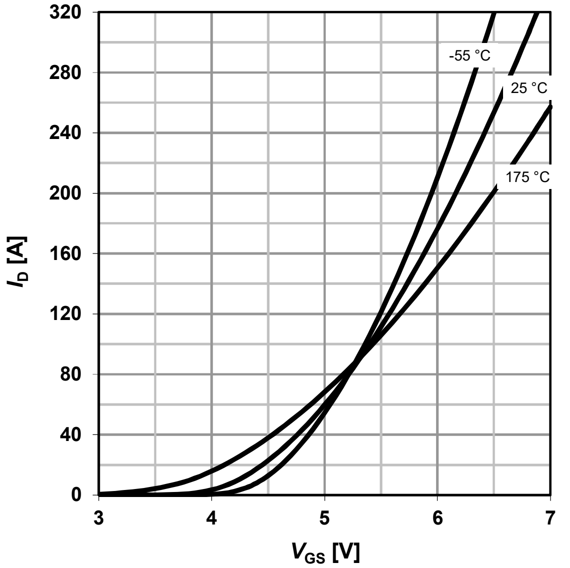
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V

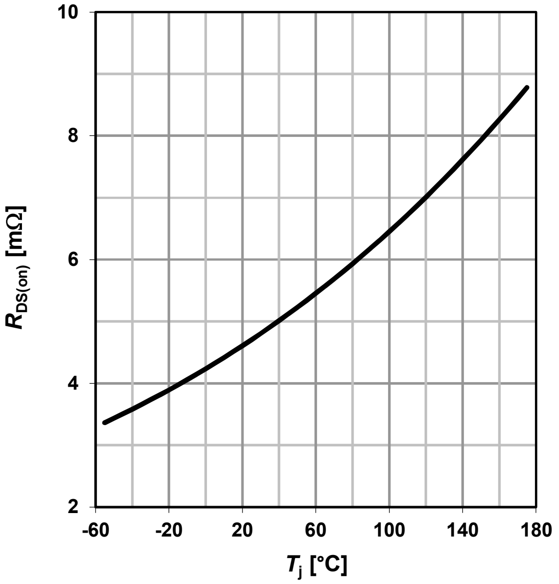
parameter: T_j



8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; $I_D = 80$ A; $V_{GS} = 10$ V; SMD

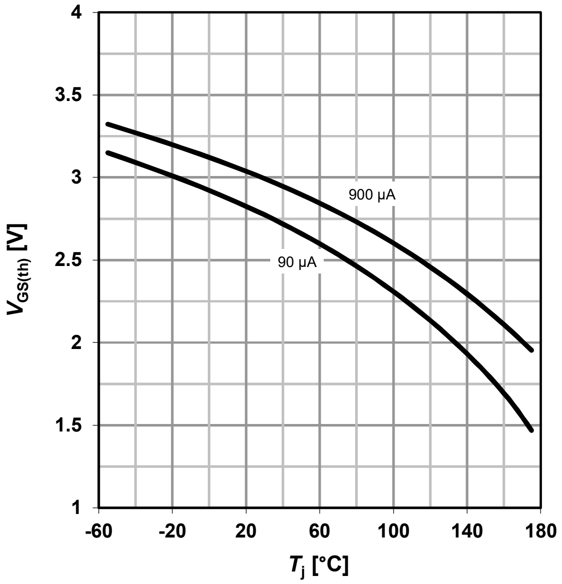
α = 0.4



9 Typ. gate threshold voltage

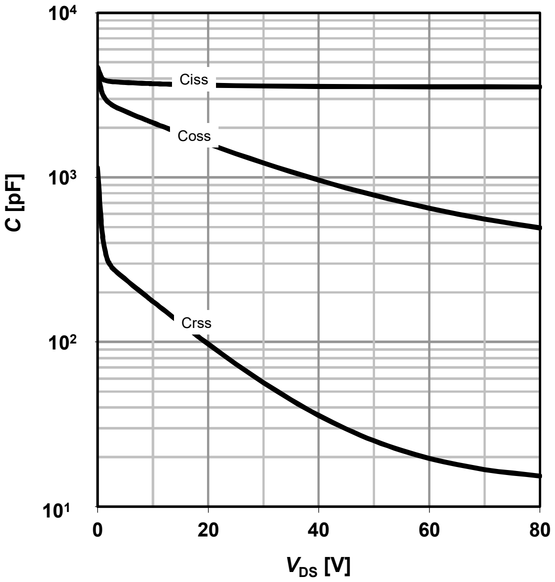
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

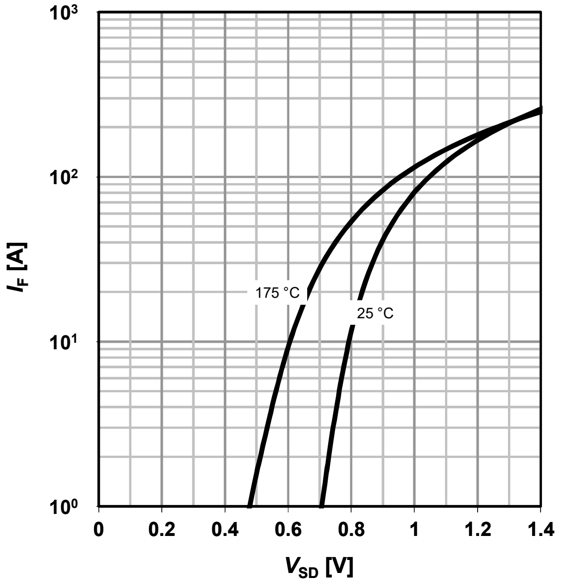
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = $f(V_{SD})$

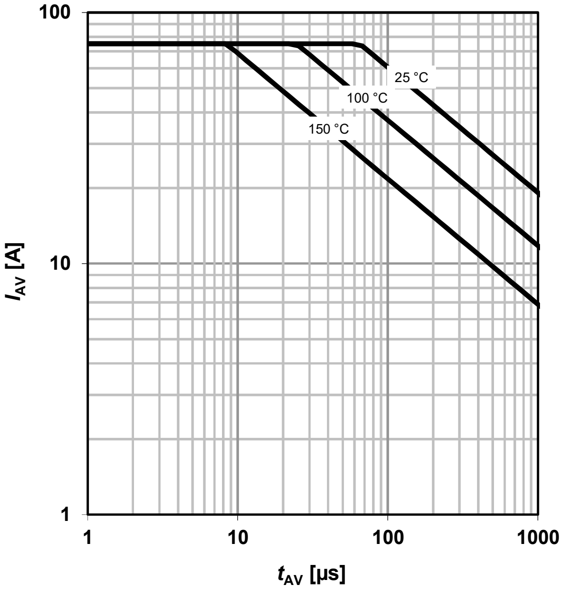
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

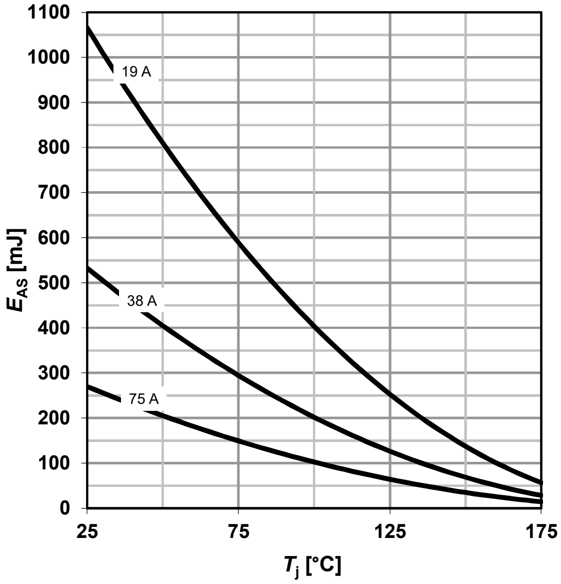
parameter: $T_{j(start)}$



13 Avalanche energy

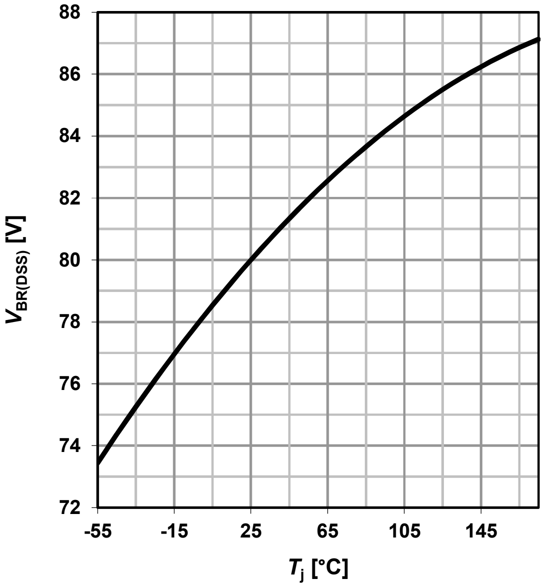
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

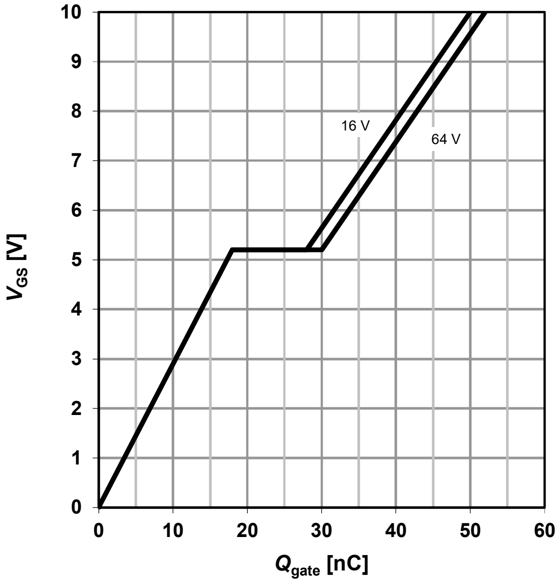
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



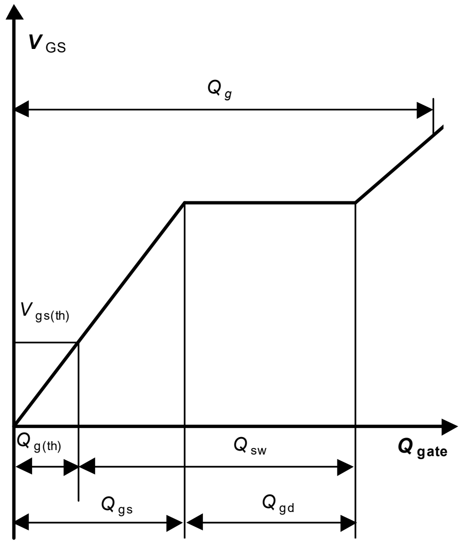
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 80$ A pulsed

parameter: V_{DD}

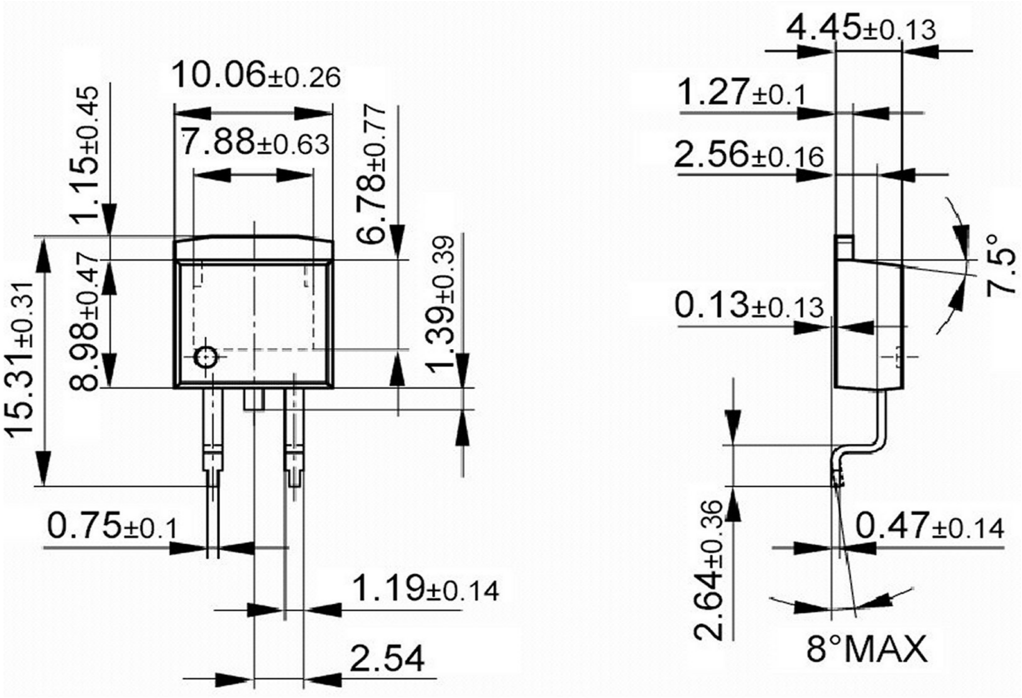


16 Gate charge waveforms

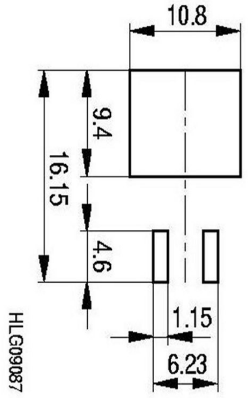


Package Outline

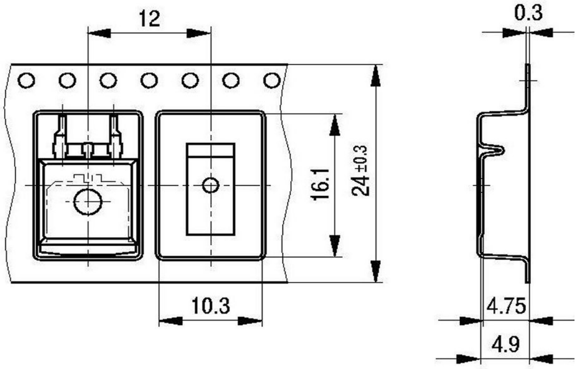
P-TO263-3-2: Outline



Footprint

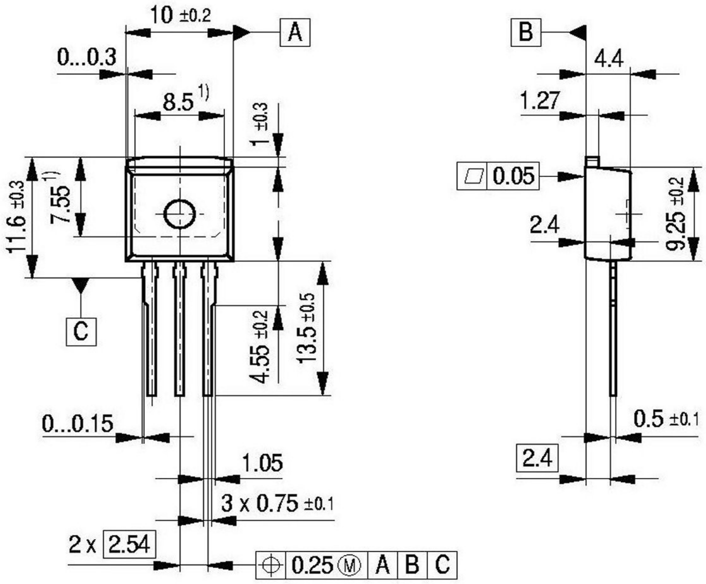


Packaging



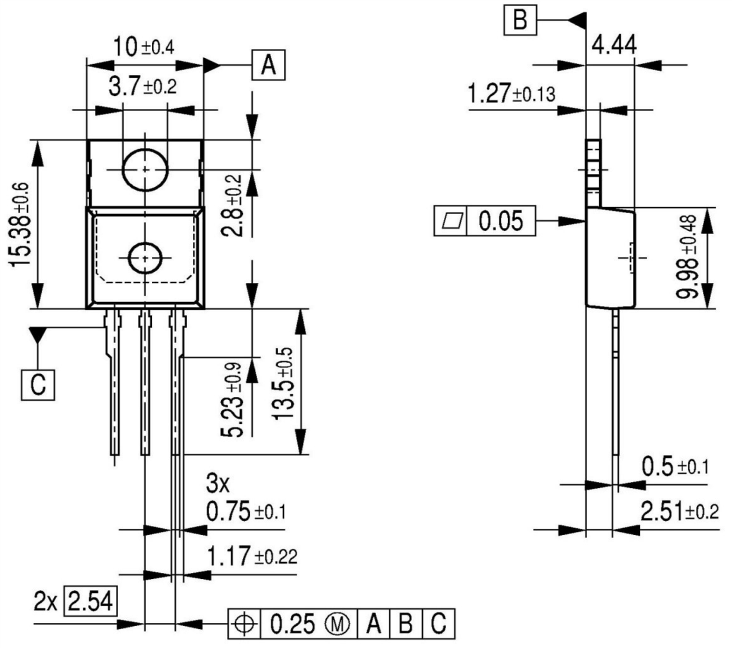
Dimensions in mm

P-TO262-3-1: Outline



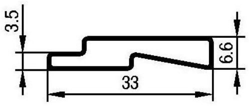
[1] Typical
Metal surface min. X = 7.25, Y = 6.9
All metal surfaces tin plated, except area of cut.

P-TO220-3-1: Outline



All metal surfaces tin plated, except area of cut.
Metal surface min. x=7.25, y=12.3

Packaging



Dimensions in mm

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Edition 2022-08-24

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference IPP_B_I80N08S4-06-Data-Sheet-11-Infineon

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Revision History

Version	Date	Changes
Revision 1.0	2014-06-20	Final data sheet
Revision 1.1	2022-08-24	Diagram 8 Typ. drain-source on-state resistance: used α value clarified