

MOSFET

700V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications
- Standoff isolation between leads

Applications

Adapter, LCD & PDP TV and Indoor lighting

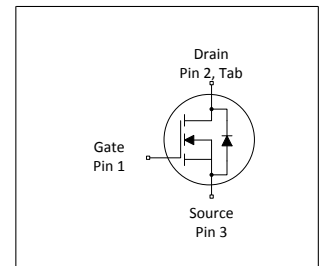


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	750	V
$R_{DS(on),max}$	1400	mΩ
$Q_{g,typ}$	10.5	nC
I_D	5.4	A
$I_{D,pulse}$	8.3	A
$E_{oss}@400V$	1.15	μJ

Type / Ordering Code	Package	Marking	Related Links
IPSA70R1K4CE	PG-TO 251	70S1K4CE	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	5.4 3.4	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	8.3	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	26	mJ	$I_D=0.6\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.10	mJ	$I_D=0.6\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, repetitive	I_{AR}	-	-	0.6	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	53	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	I_S	-	-	3.8	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	8.3	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	500	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8

¹⁾ Limited by $T_{j,max}$. Maximum duty cycle $D=0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.37	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	lead
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}$, $I_D=0.1mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=700V$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=700V$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.26 3.28	1.40 -	Ω	$V_{GS}=10V$, $I_D=1A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=1A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	6.5	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	225	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Output capacitance	C_{oss}	-	18	-	pF	$V_{GS}=0V$, $V_{DS}=100V$, $f=1MHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	10	-	pF	$V_{GS}=0V$, $V_{DS}=0...480V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	42	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...480V$
Turn-on delay time	$t_{d(on)}$	-	7.7	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.5A$, $R_G=10.2\Omega$; see table 9
Rise time	t_r	-	5.9	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.5A$, $R_G=10.2\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.5A$, $R_G=10.2\Omega$; see table 9
Fall time	t_f	-	18.2	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=1.5A$, $R_G=10.2\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	1.3	-	nC	$V_{DD}=480V$, $I_D=1.5A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	5.8	-	nC	$V_{DD}=480V$, $I_D=1.5A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	10.5	-	nC	$V_{DD}=480V$, $I_D=1.5A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480V$, $I_D=1.5A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 480V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 480V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=1.5A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	200	-	ns	$V_R=400V$, $I_F=1.5A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.9	-	μC	$V_R=400V$, $I_F=1.5A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	8	-	A	$V_R=400V$, $I_F=1.5A$, $di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

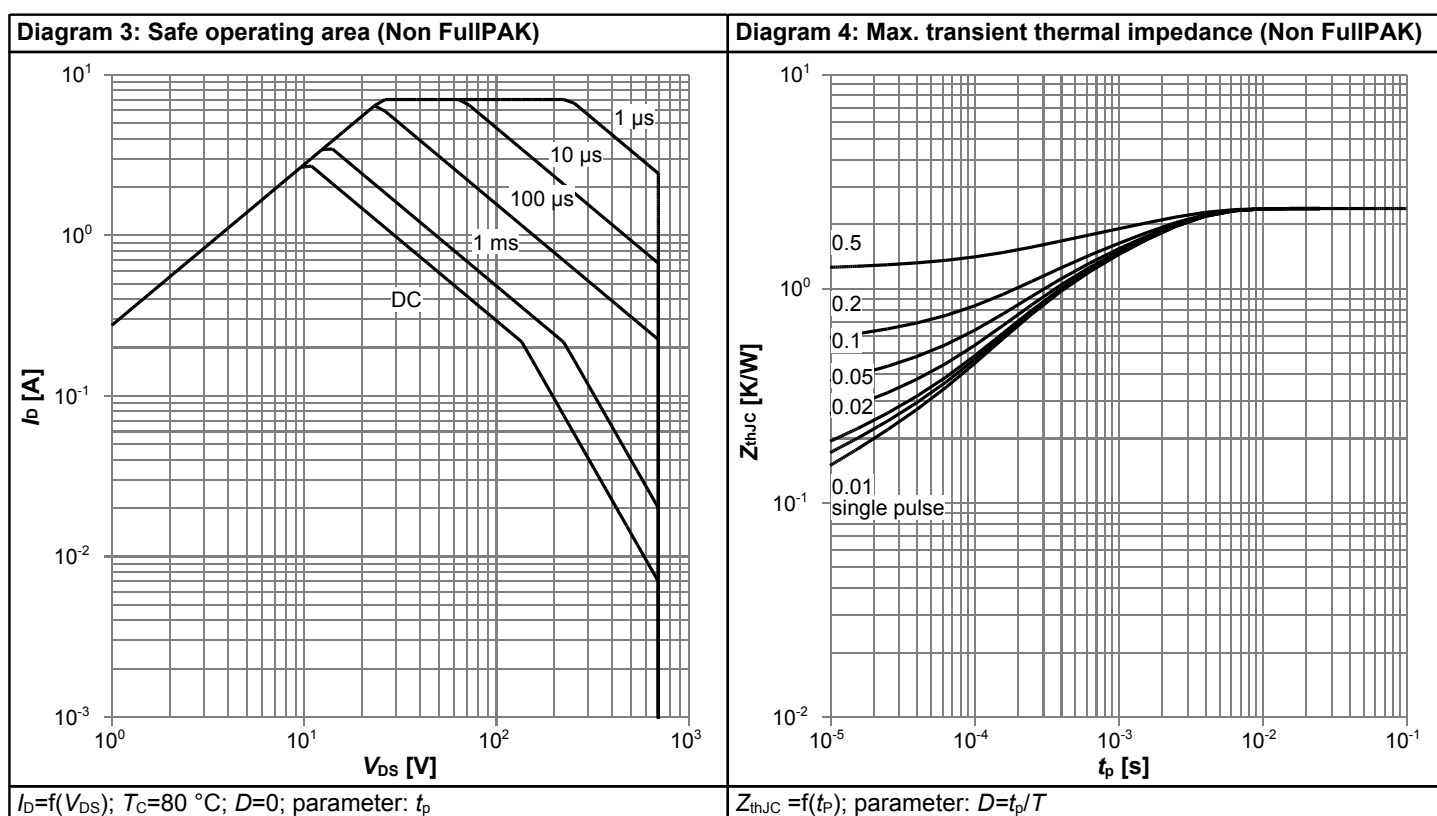
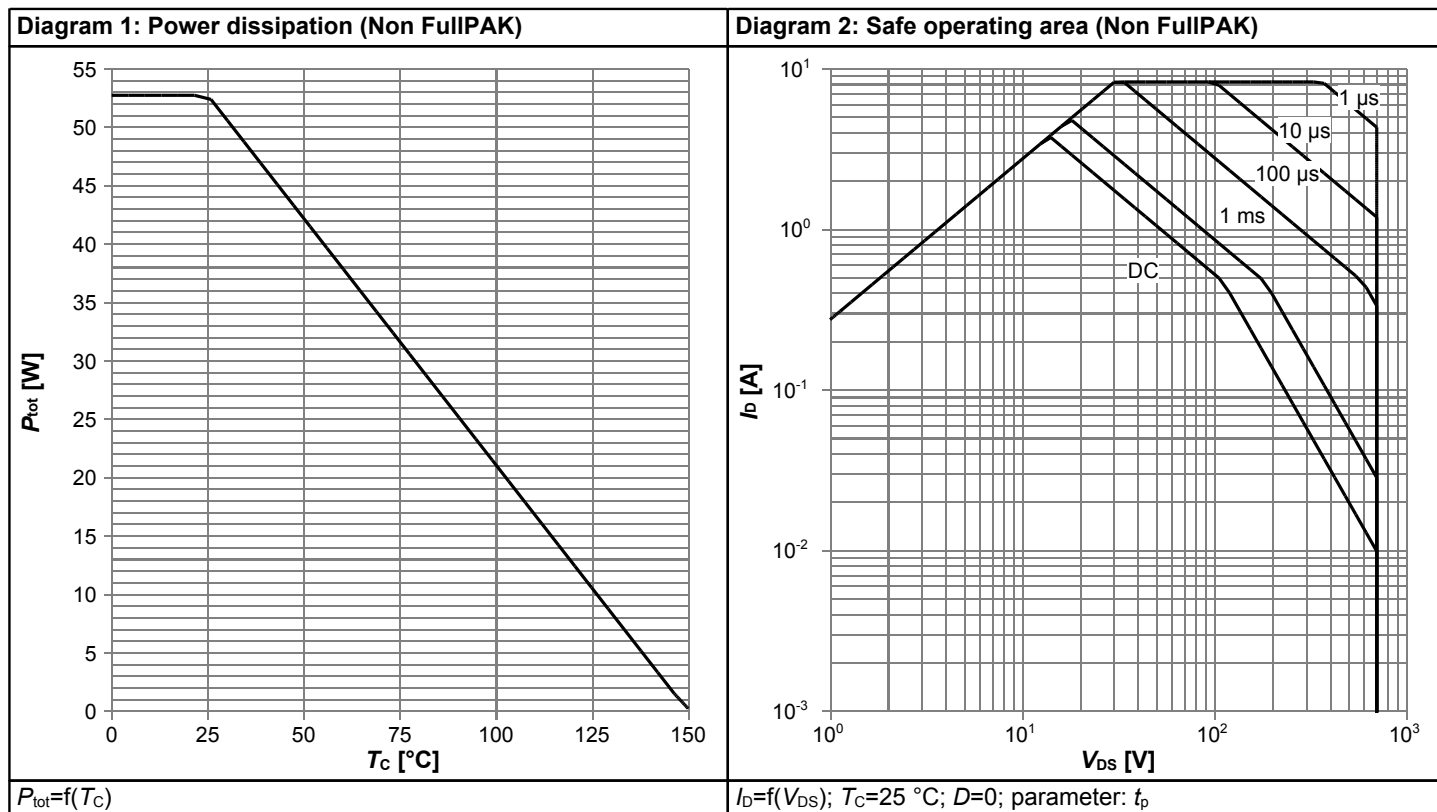
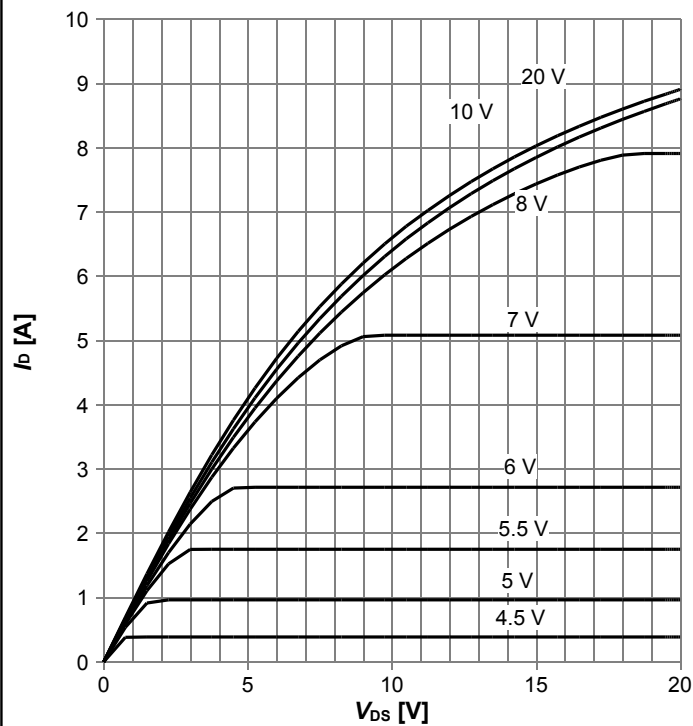
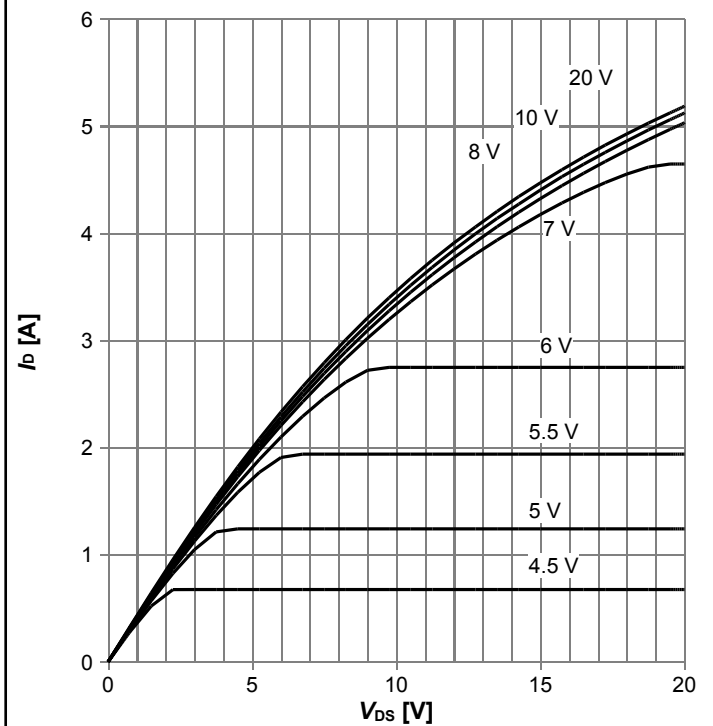


Diagram 5: Typ. output characteristics



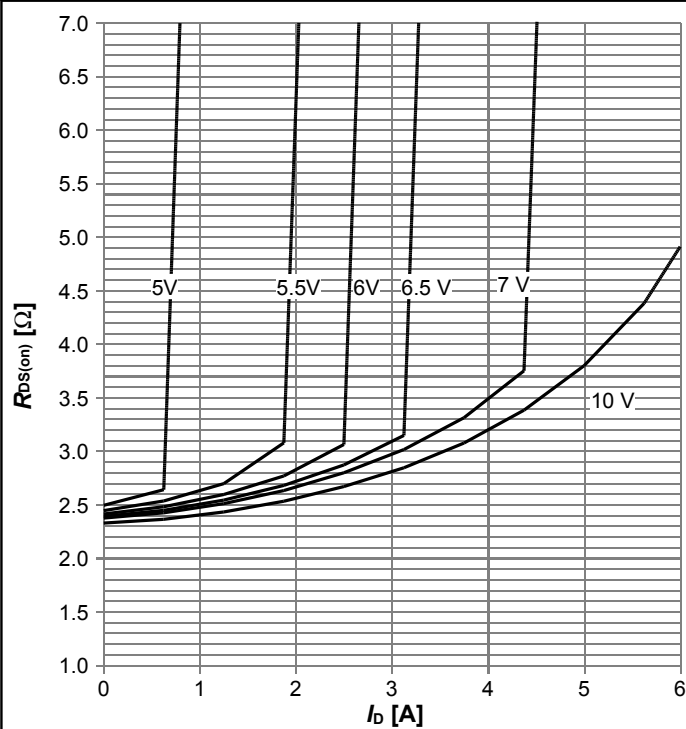
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



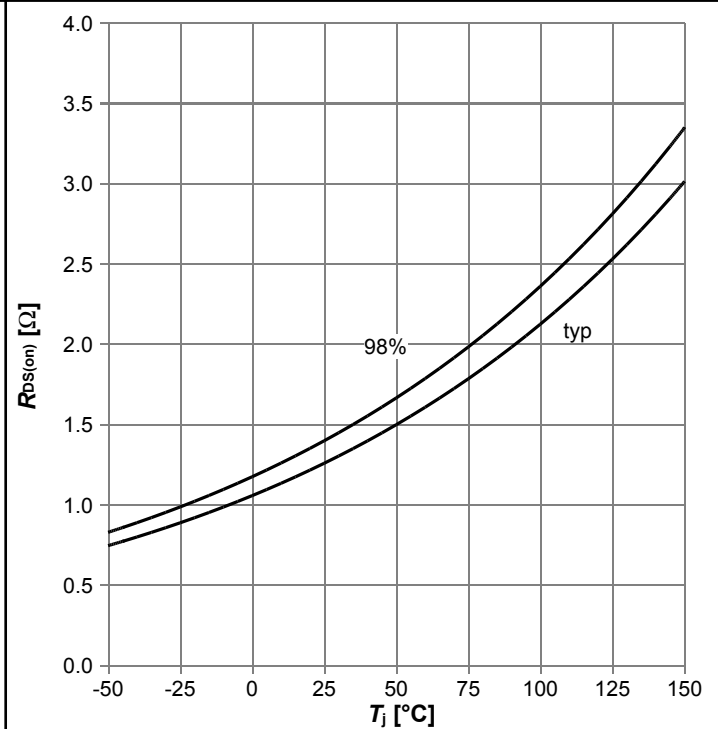
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



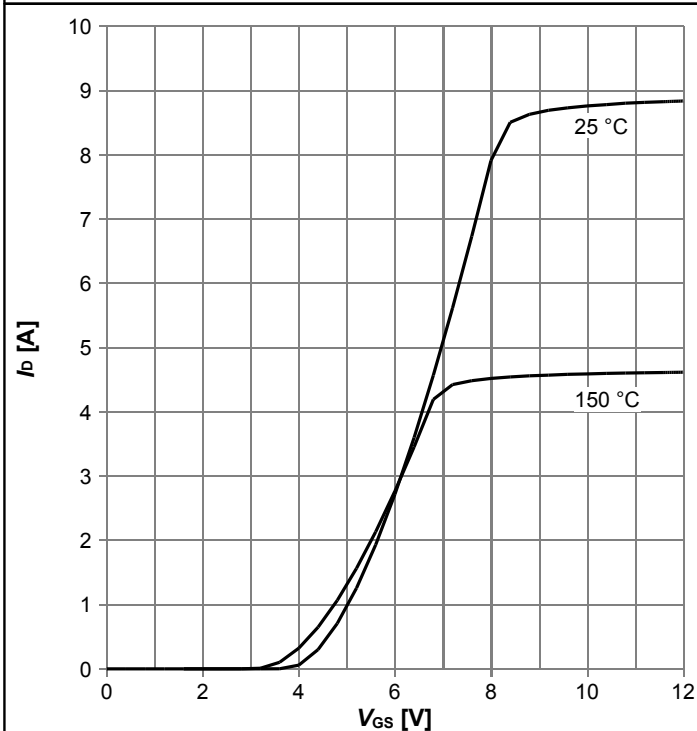
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



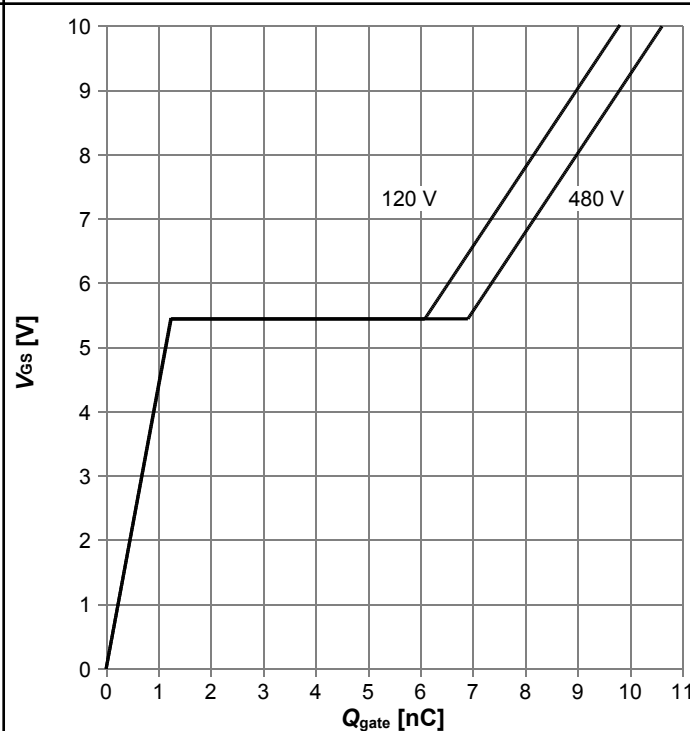
$R_{DS(on)} = f(T_j)$; $I_D = 1.2\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



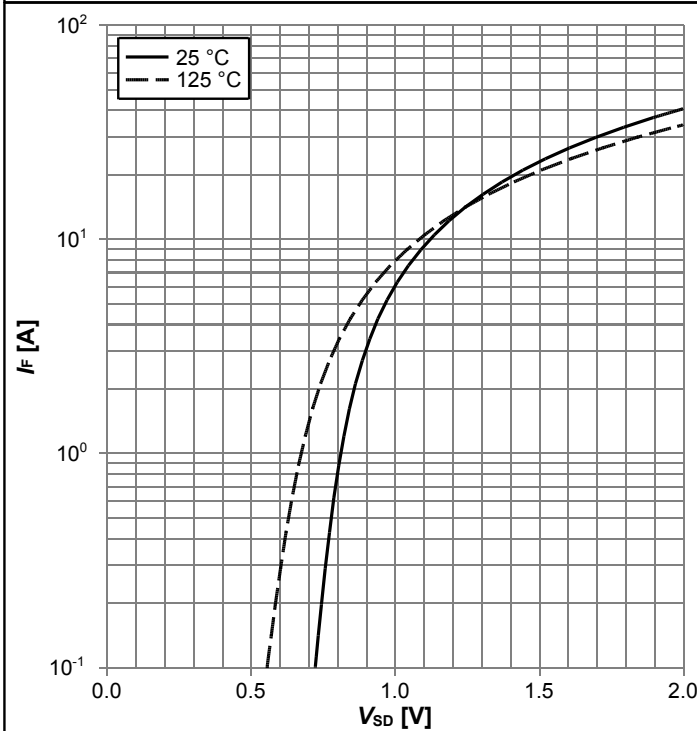
$I_D=f(V_{GS})$; $V_{DS}=20V$; parameter: T_j

Diagram 10: Typ. gate charge



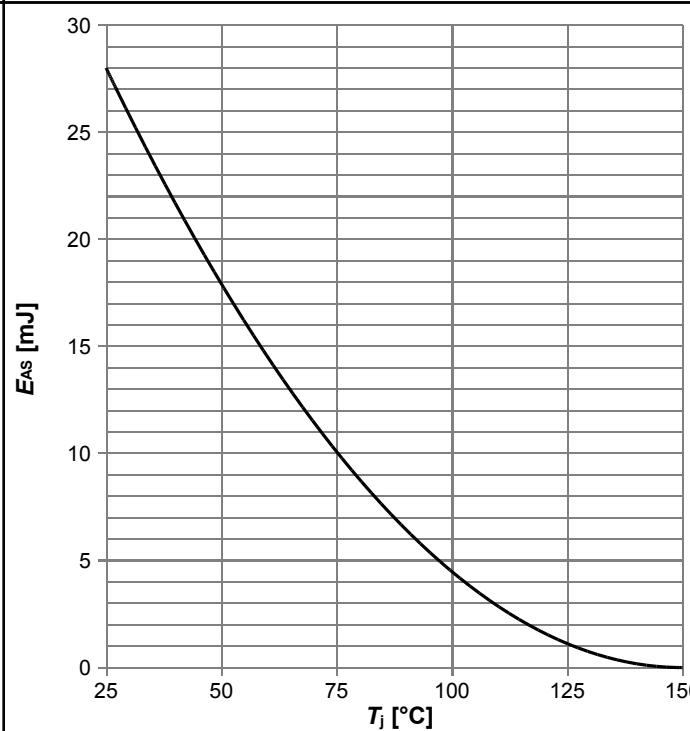
$V_{GS}=f(Q_{gate})$; $I_D=1.5 A$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



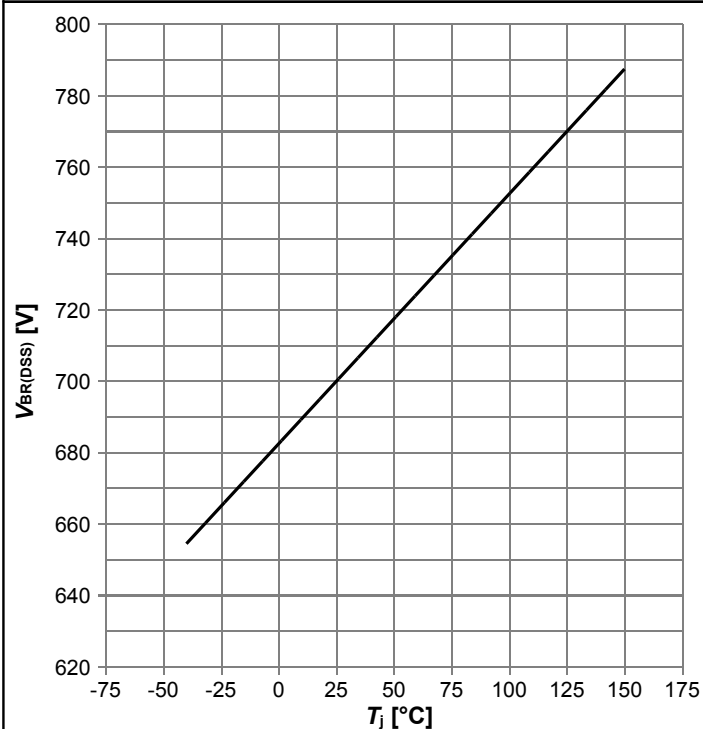
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



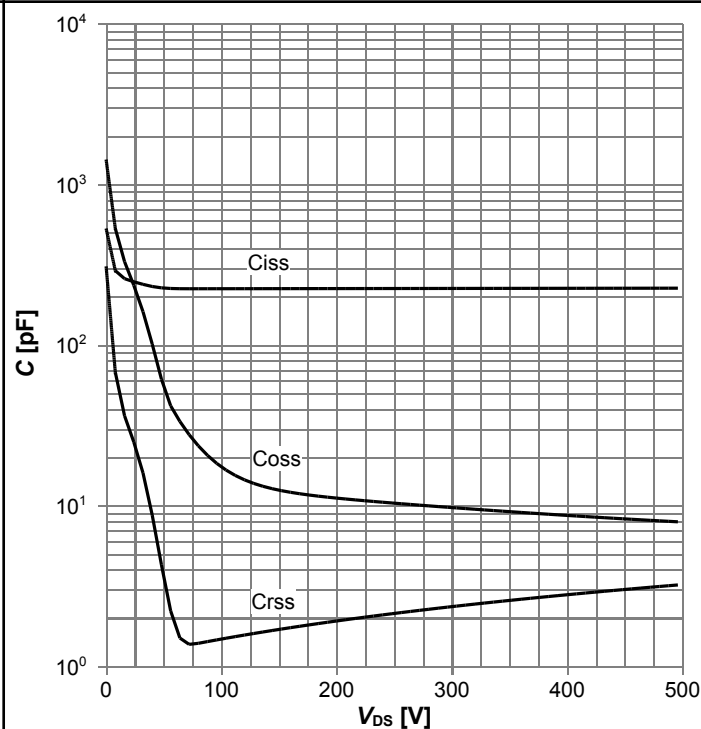
$E_{AS}=f(T_j)$; $I_D=0.5 A$; $V_{DD}=50 V$

Diagram 13: Drain-source breakdown voltage



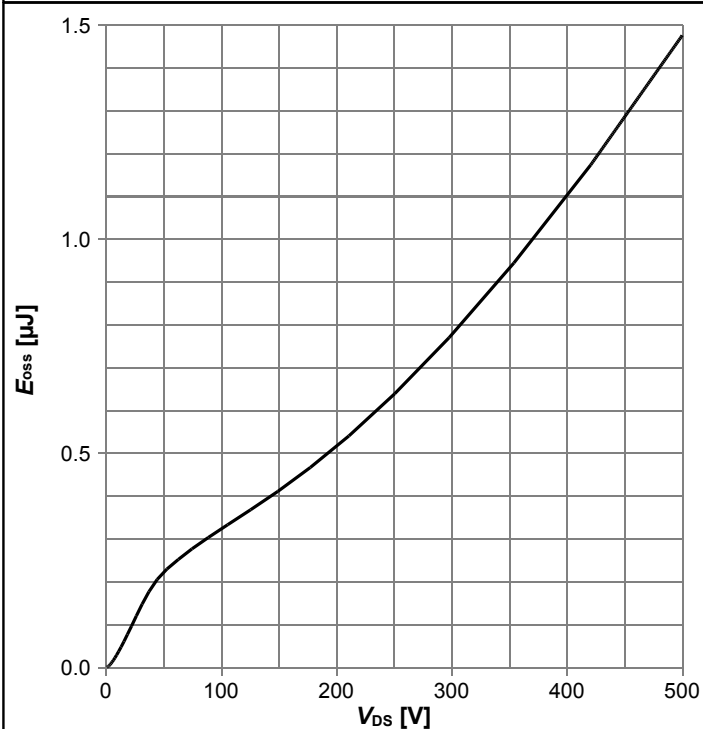
$V_{BR(DSS)} = f(T_J); I_D = 1.0 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

6 Package Outlines

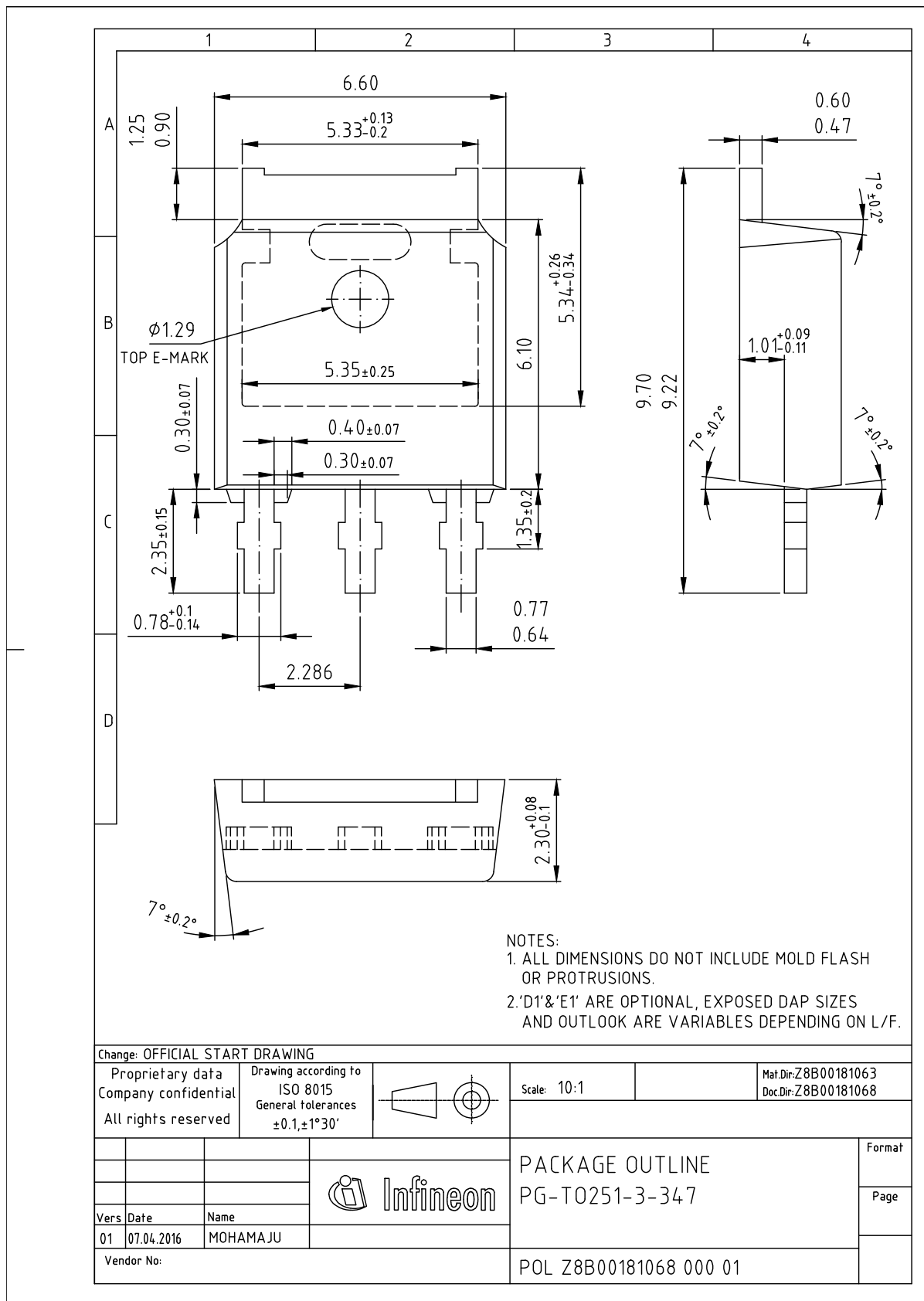


Figure 1 Outline PG-TO 251, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPSA70R1K4CE

Revision: 2016-09-07, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-09-07	Release of final version

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