

# MOSFET

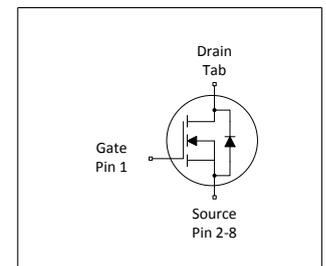
## OptiMOS™ Power-Transistor, 60 V

### Features

- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Fully qualified according to JEDEC for Industrial Applications



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	1.2	mΩ
$I_D$	313	A
$Q_{oss}$	119	nC
$Q_G(0V..10V)$	106	nC



Type / Ordering Code	Package	Marking	Related Links
IPT012N06N	PG-HSOF-8	012N06N	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	313 221 41	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ , $R_{thJA}=40\text{ K/W}^2)$
Pulsed drain current <sup>3)</sup>	$I_{D,pulse}$	-	-	1252	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>4)</sup>	$E_{AS}$	-	-	420	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	214	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.4	0.7	K/W	-
Device on PCB, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>2)</sup>	$R_{thJA}$	-	-	40	K/W	-

<sup>1)</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher Tcase please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> See Diagram 3 for more detailed information

<sup>4)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$ , $I_D=143\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.5 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.0 1.4	1.2 2.0	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=50\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.6	2.4	$\Omega$	-
Transconductance	$g_{fs}$	120	240	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=100\text{ A}$

**Table 5 Dynamic characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	7800	9750	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	1800	2250	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	69	138	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.8\text{ }\Omega$
Rise time	$t_r$	-	27	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.8\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	48	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.8\text{ }\Omega$
Fall time	$t_f$	-	23	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_{G,ext}=1.8\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>3)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	35	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	22	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>2)</sup>	$Q_{gd}$	-	19	25	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	32	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>2)</sup>	$Q_g$	-	106	124	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	94	-	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>2)</sup>	$Q_{oss}$	-	119	149	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> See figure 16 for gate charge parameter definition

<sup>2)</sup> Defined by design. Not subject to production test

<sup>3)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	179	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1252	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	90	180	ns	$V_R=30\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	237	474	nC	$V_R=30\text{ V}, I_F=100\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test

### 4 Electrical characteristics diagrams

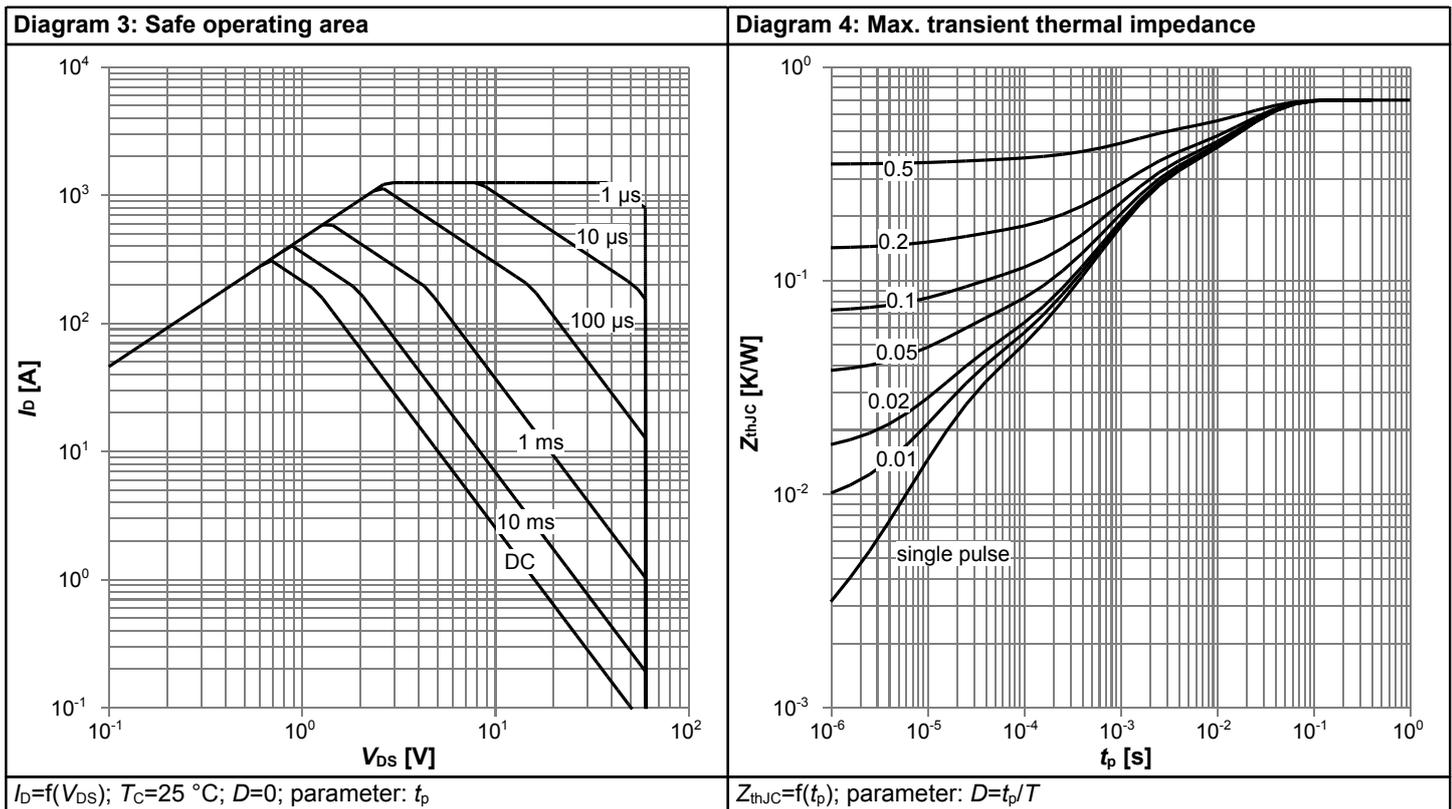
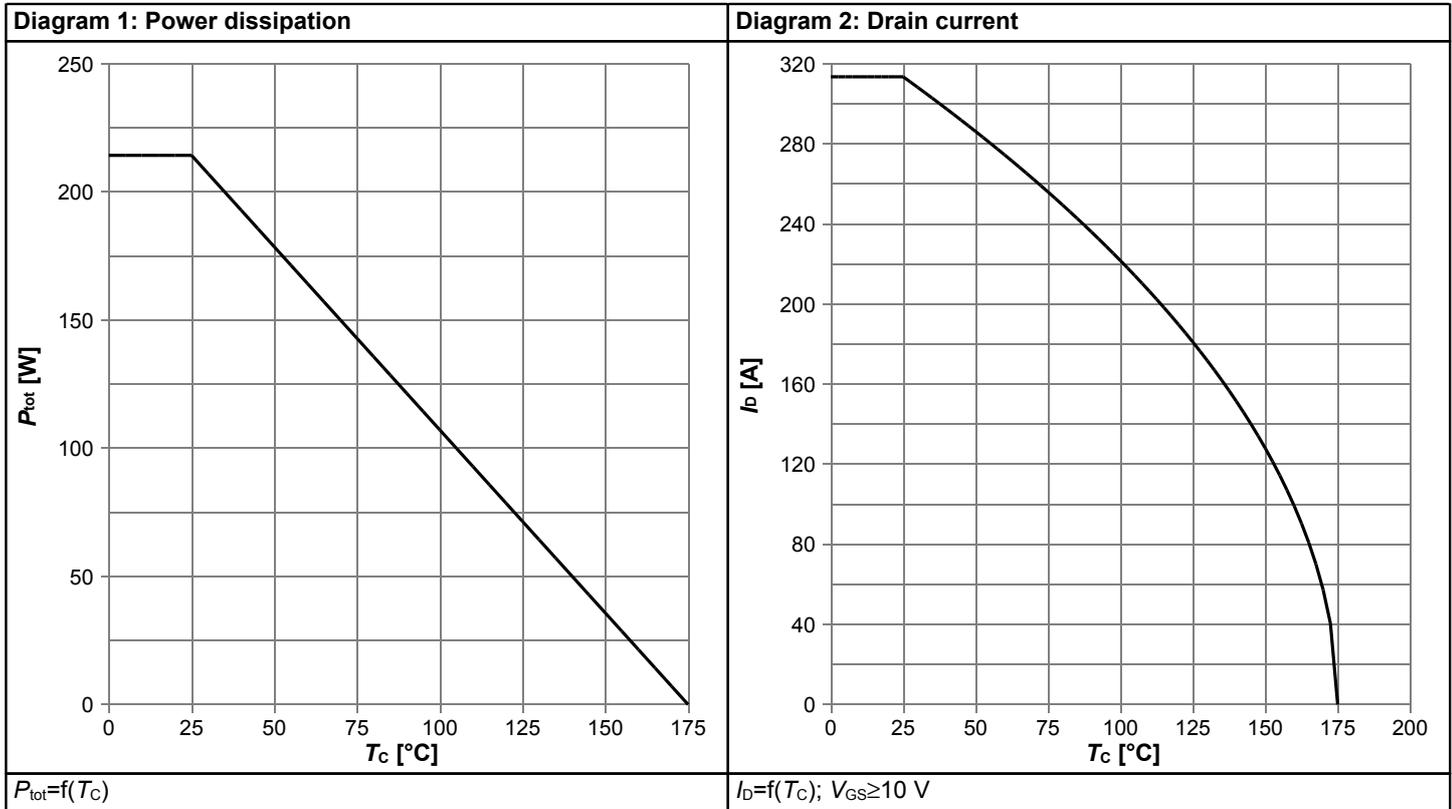
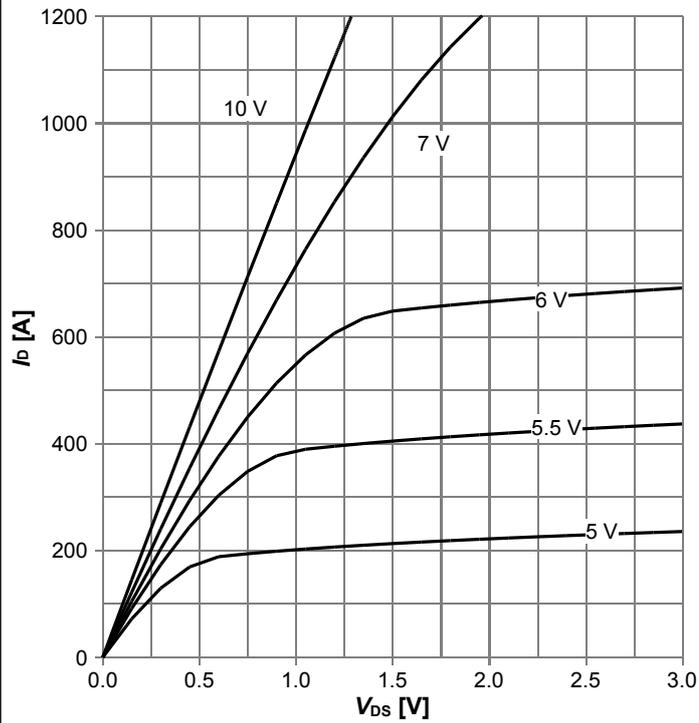
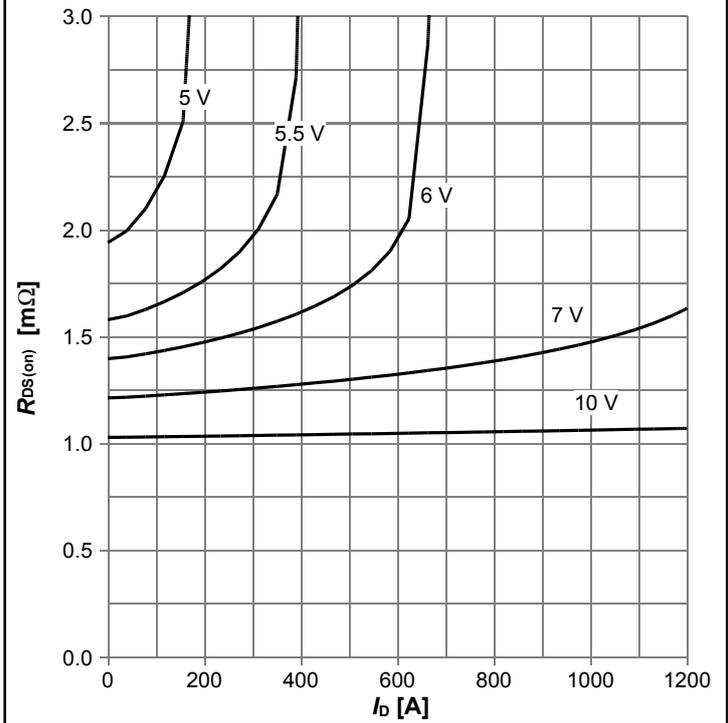


Diagram 5: Typ. output characteristics



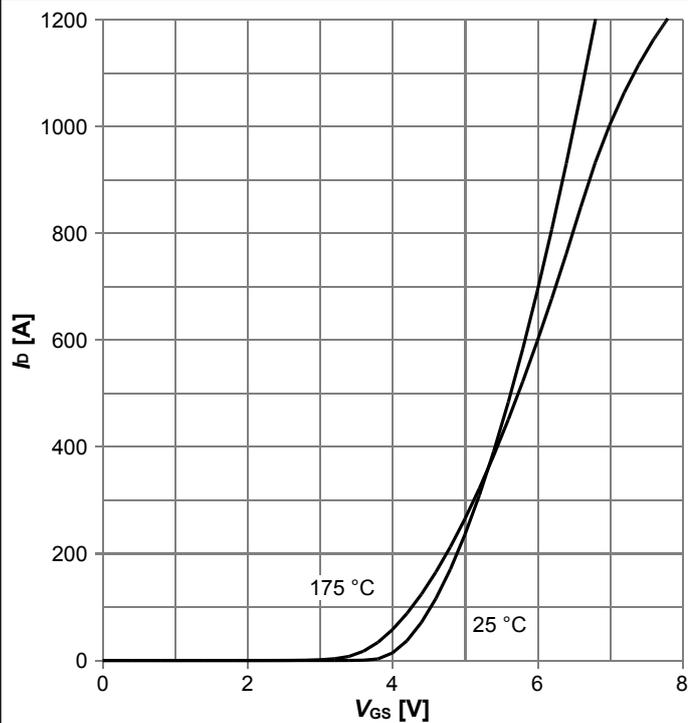
$I_D = f(V_{DS}); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



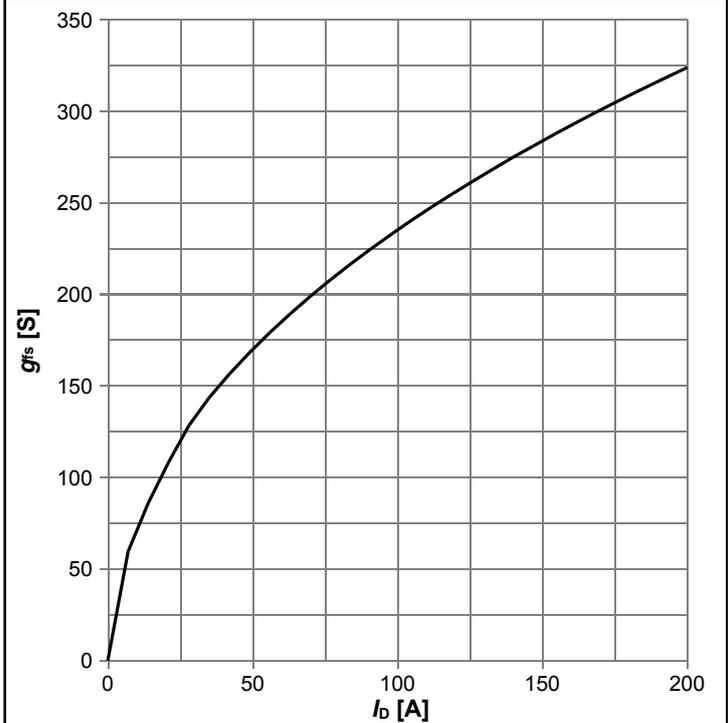
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



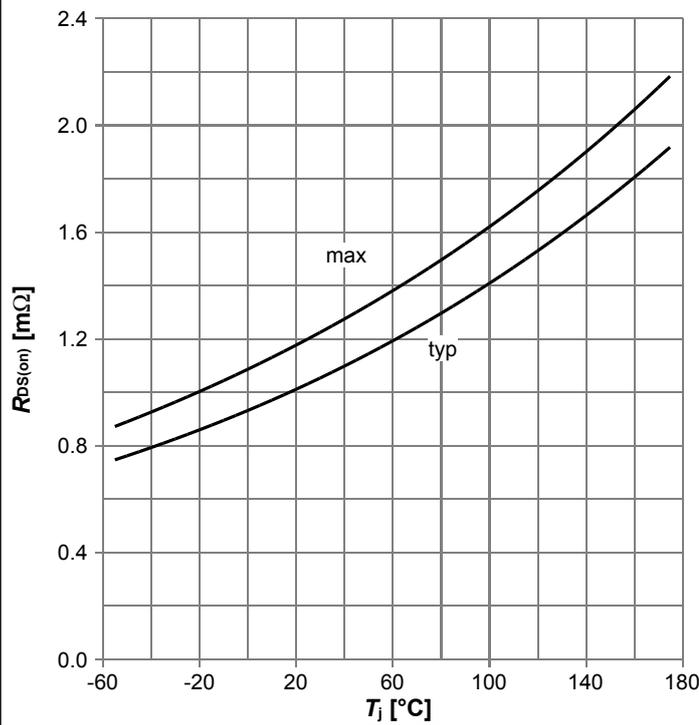
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



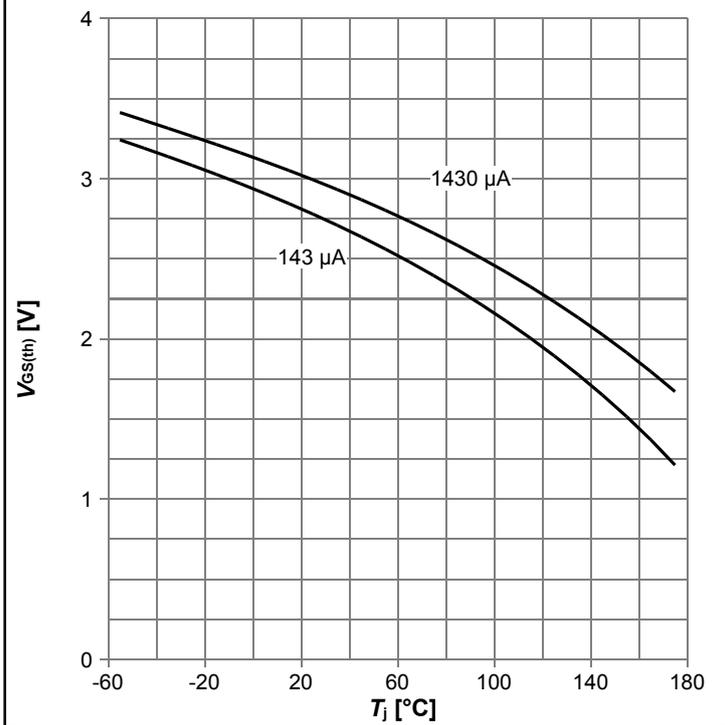
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



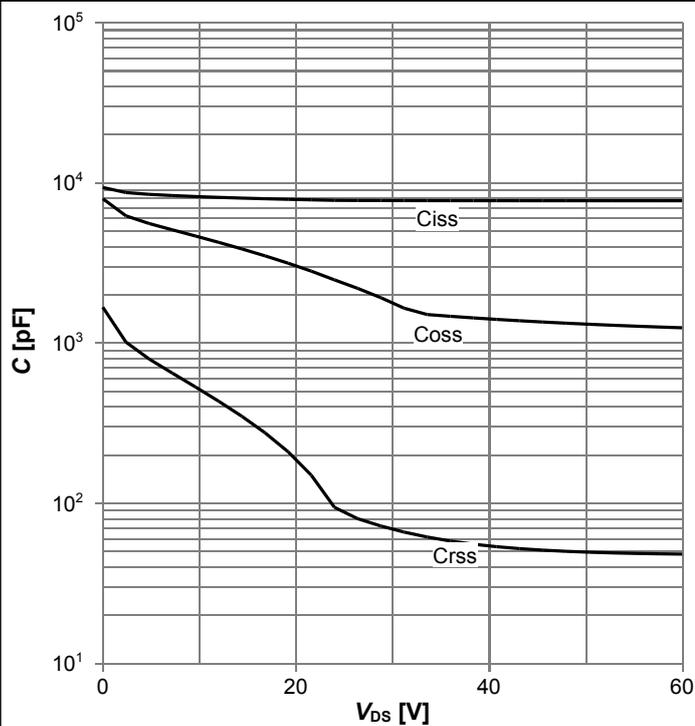
$R_{DS(on)}=f(T_j)$ ;  $I_D=100\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



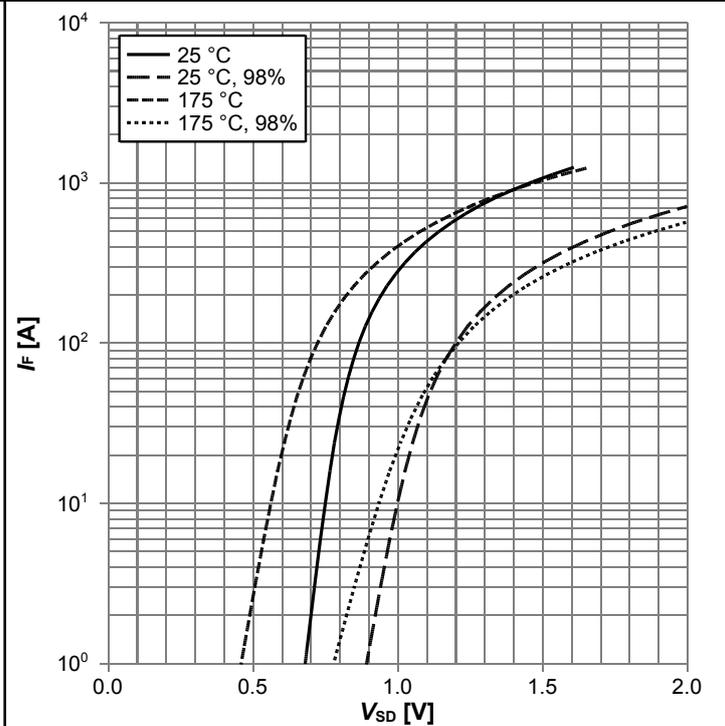
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



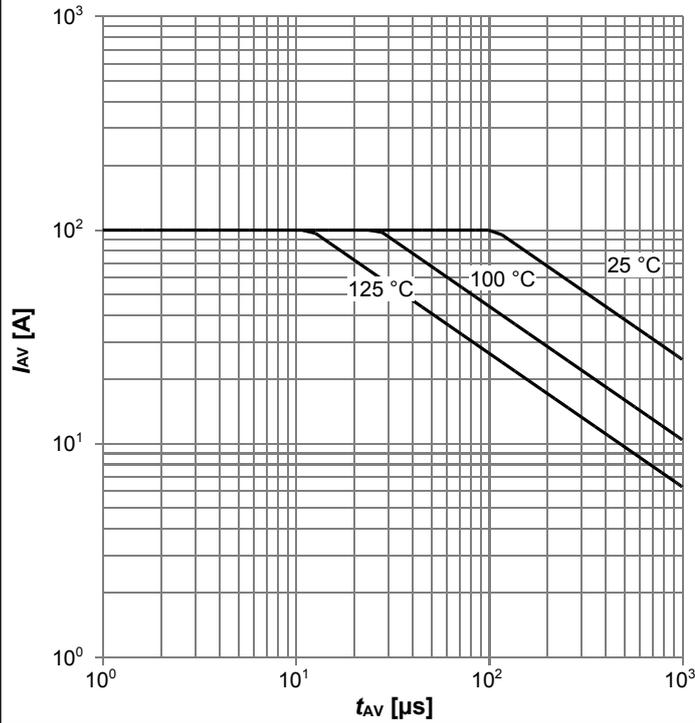
$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



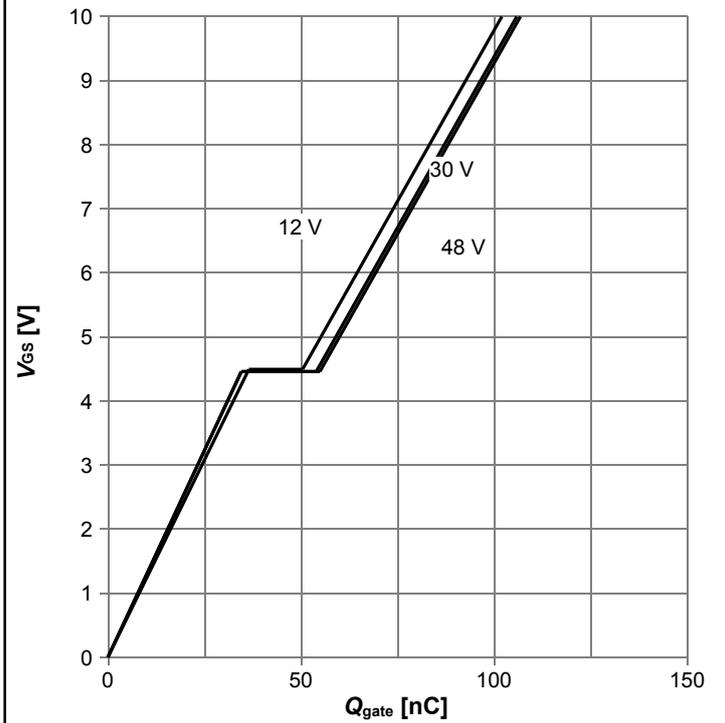
$I_F=f(V_{SD})$ ; parameter:  $T_j$

**Diagram 13: Avalanche characteristics**



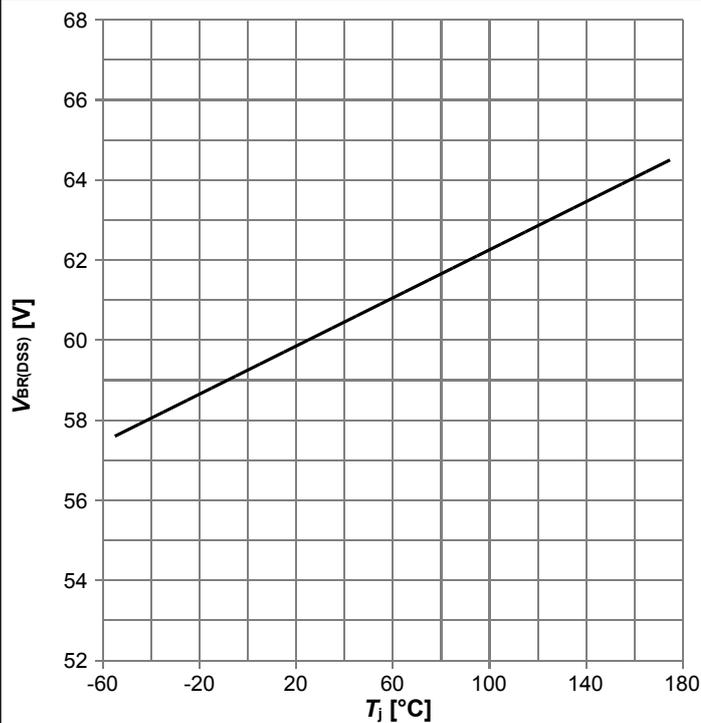
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

**Diagram 14: Typ. gate charge**



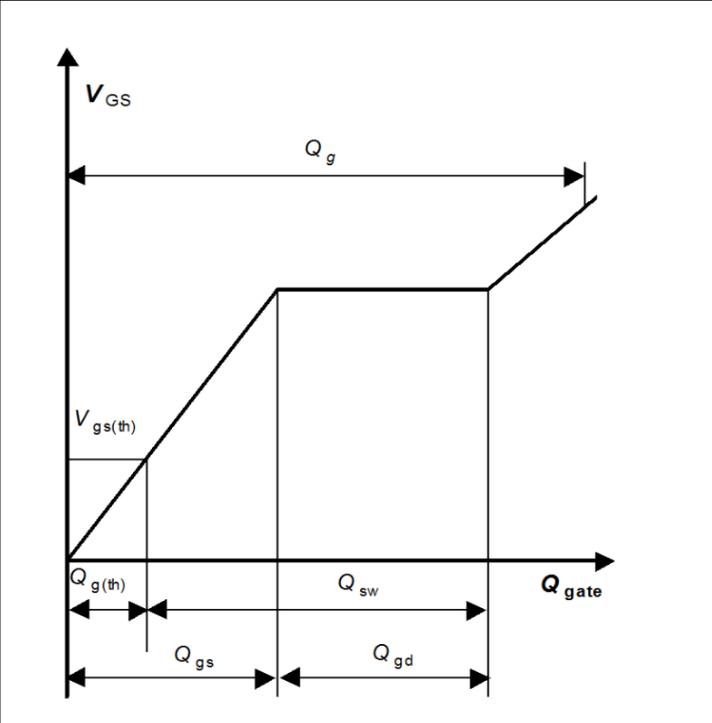
$V_{GS}=f(Q_{gate}); I_D=100$  A pulsed; parameter:  $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

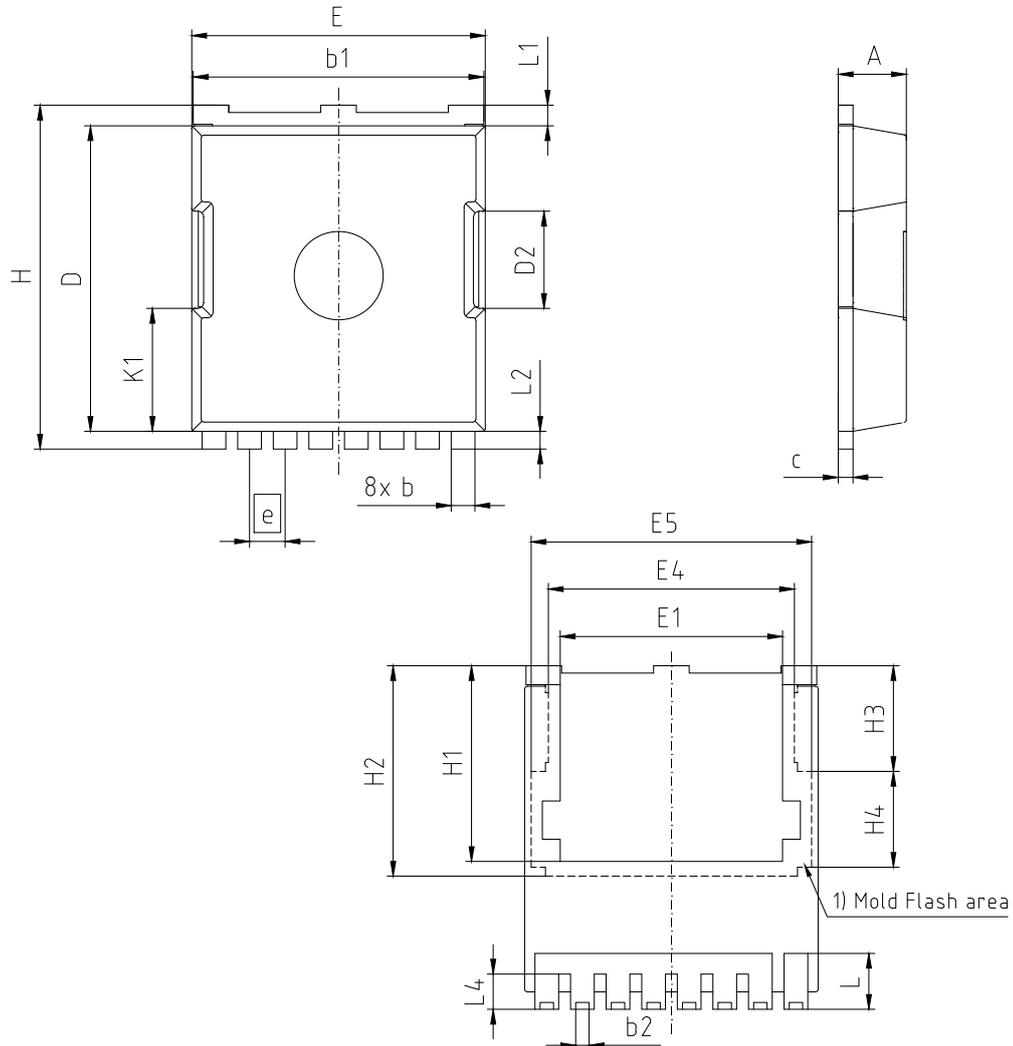


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

**Diagram Gate charge waveforms**



## 5 Package Outlines



1) partially covered with Mold Flash

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
b1	9.70	9.90	0.382	0.390
b2	0.42	0.50	0.017	0.020
c	0.40	0.60	0.016	0.024
D	10.28	10.58	0.405	0.416
D2	3.30		0.130	
E	9.70	10.10	0.382	0.398
E1	7.50		0.295	
E4	8.50		0.335	
E5	9.46		0.372	
e	1.20 (BSC)		0.047 (BSC)	
H	11.48	11.88	0.452	0.468
H1	6.55	6.75	0.258	0.266
H2	7.15		0.281	
H3	3.59		0.141	
H4	3.26		0.128	
N	8		8	
K1	4.18		0.165	
L	1.60	2.10	0.063	0.083
L1	0.70		0.028	
L2	0.60		0.024	
L4	1.00	1.30	0.039	0.051

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Figure 1 Outline PG-HSOF-8, dimensions in mm/inches

## Revision History

IPT012N06N

**Revision: 2019-07-15, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-12-09	Release of final version
2.1	2019-07-15	Update Continuous Current

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