

HEXFET® Power MOSFET

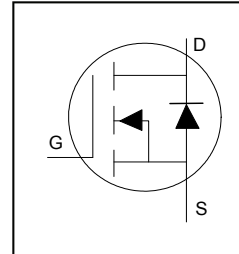
**Applications**

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free

$V_{DSS}$	<b>60V</b>
$R_{DS(on)}$ <b>typ.</b>	<b>3.3m<math>\Omega</math></b>
<b>max.</b>	<b>4.2m<math>\Omega</math></b>
$I_D$	<b>71A</b>



TO-220 Full-Pak

G	D	S
Gate	Drain	Source

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFI3306GPbF	TO-220 Full-Pak	Tube	50	IRFI3306GPbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	71	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	50	
$I_{DM}$	Pulsed Drain Current ①	300	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	46	W
	Linear Derating Factor	0.31	W/ $^\circ\text{C}$
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	311	mJ
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ\text{C}$
$T_{STG}$			
		Soldering Temperature, for 10 seconds (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10lb•in (1.1N•m)	

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	3.23	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ④	—	65	

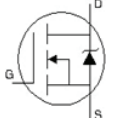
**Static Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.068	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5.0mA <sup>③</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	3.3	4.2	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 43A <sup>③</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 150μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G(int)</sub>	Internal Gate Resistance	—	0.72	—	Ω	

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	89	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 43A
Q <sub>g</sub>	Total Gate Charge	—	90	135	nC	I <sub>D</sub> = 43A
Q <sub>gs</sub>	Gate-to-Source Charge	—	22	—		V <sub>DS</sub> = 30V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	26	—		V <sub>GS</sub> = 10V <sup>③</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	116	—		I <sub>D</sub> = 43A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	15	—	ns	V <sub>DD</sub> = 39V
t <sub>r</sub>	Rise Time	—	30	—		I <sub>D</sub> = 43A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	45	—		R <sub>G</sub> = 2.7Ω
t <sub>f</sub>	Fall Time	—	33	—		V <sub>GS</sub> = 10V <sup>③</sup>
C <sub>iss</sub>	Input Capacitance	—	4685	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	506	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	310	—		f = 1.0 MHz
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related) <sup>⑥</sup>	—	733	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑥</sup>
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related) <sup>⑤</sup>	—	822	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 48V <sup>⑤</sup>

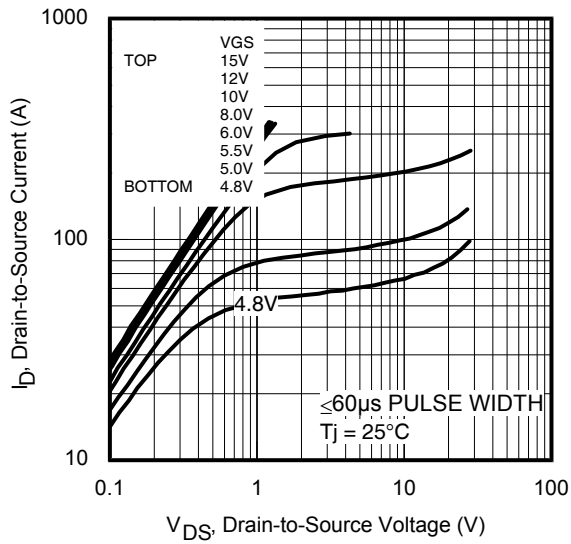
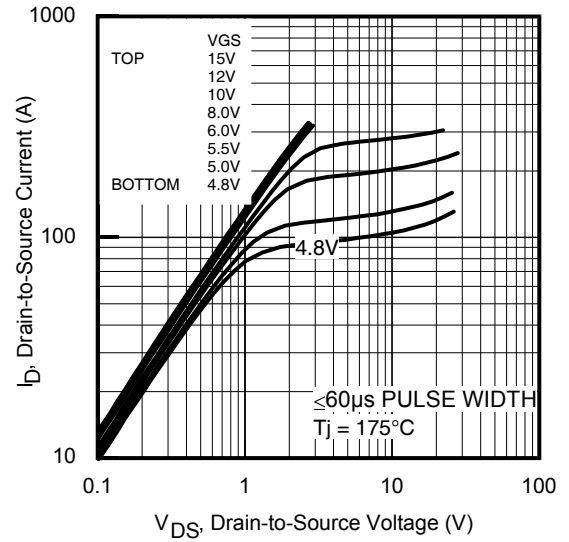
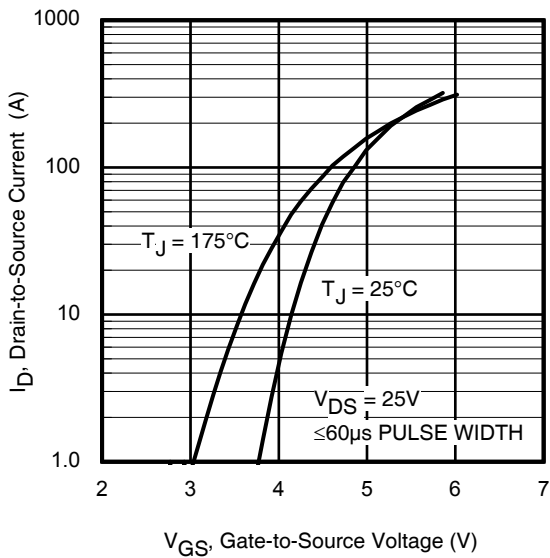
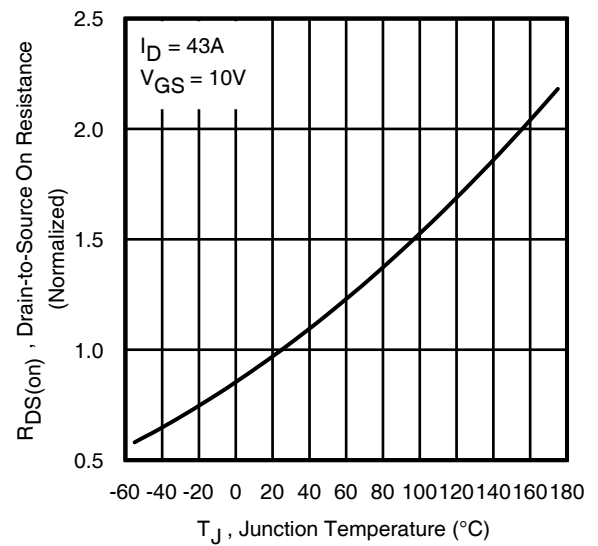
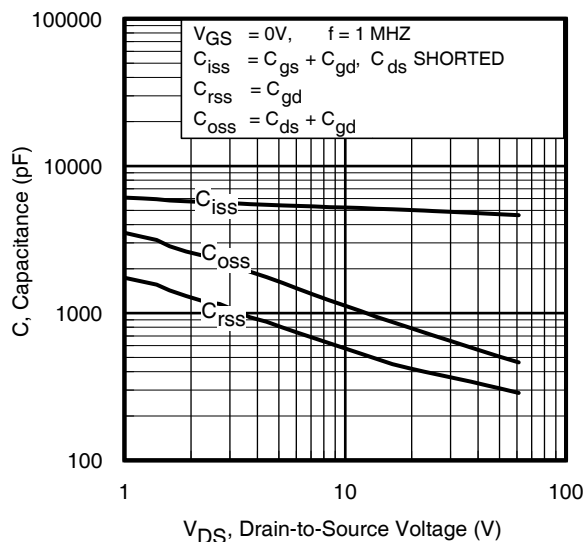
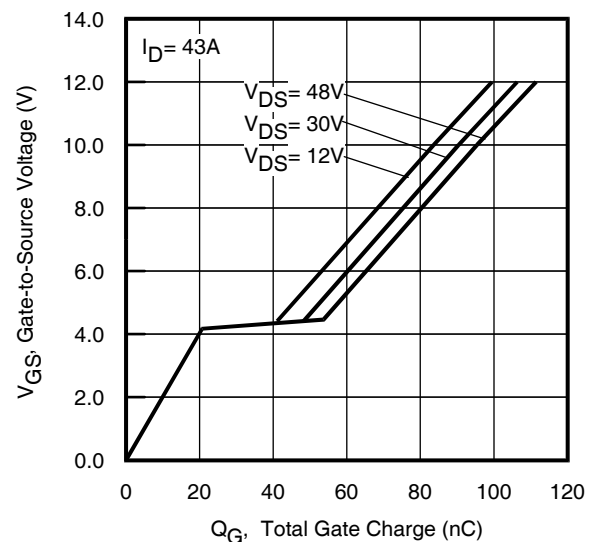
**Diode Characteristics**

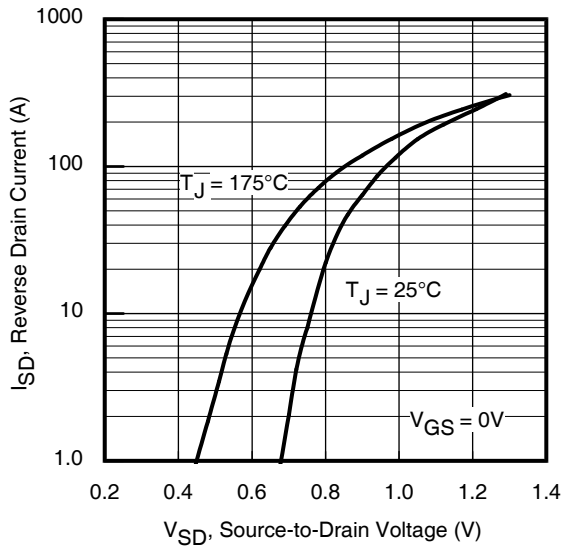
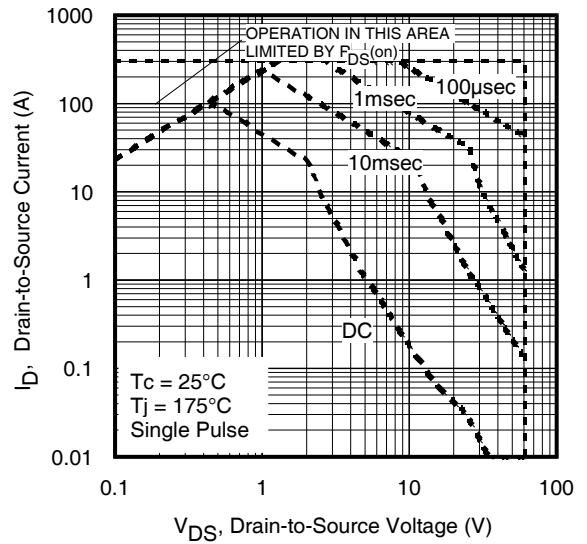
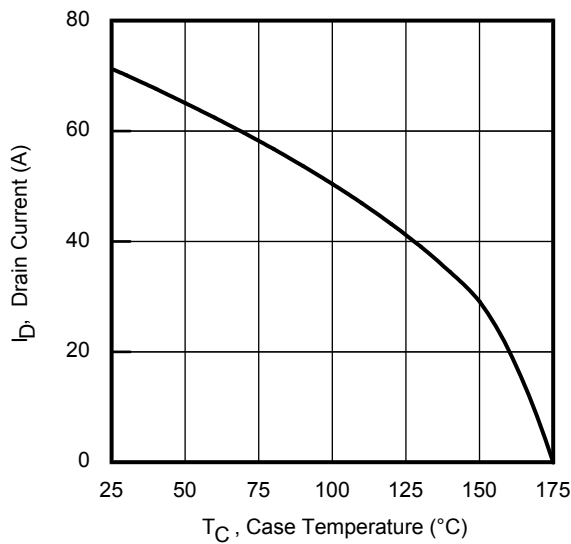
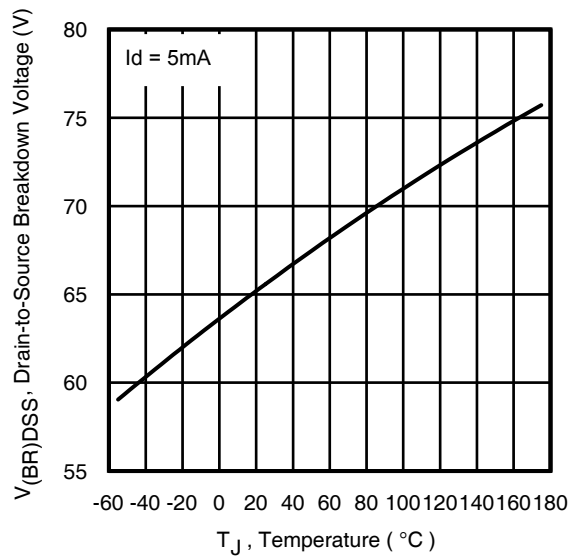
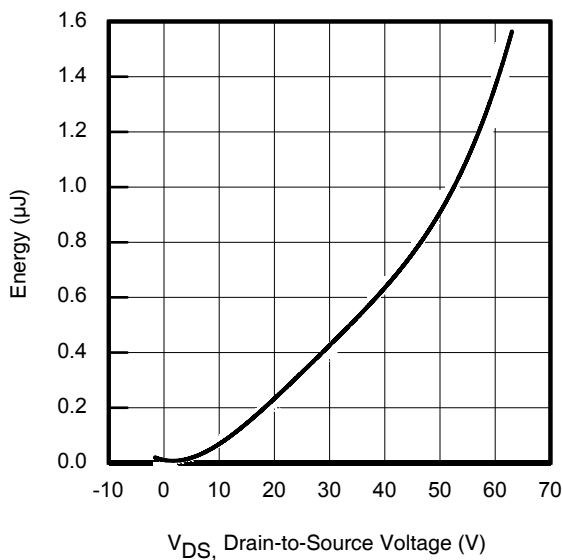
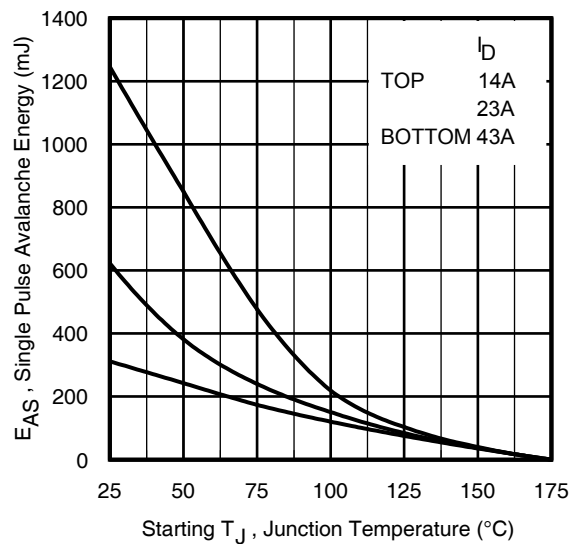
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	71	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	300	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 43A, V <sub>GS</sub> = 0V <sup>③</sup>
dv/dt	Peak Diode Recovery <sup>④</sup>	—	2.3	—	V/ns	
t <sub>rr</sub>	Reverse Recovery Time	—	43	—	ns	T <sub>J</sub> = 25°C — V <sub>R</sub> = 51V
		—	47	—		T <sub>J</sub> = 125°C — I <sub>F</sub> = 43A
Q <sub>rr</sub>	Reverse Recovery Charge	—	63	—	nC	T <sub>J</sub> = 25°C — di/dt = 100A/μs <sup>③</sup>
		—	78	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	2.5	—	A	T <sub>J</sub> = 25°C

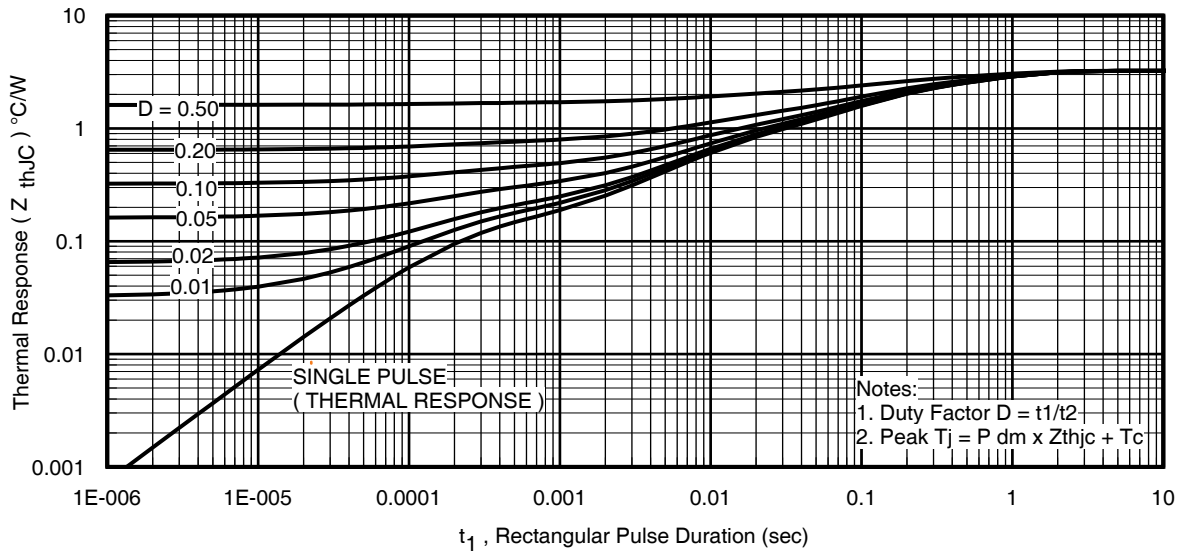
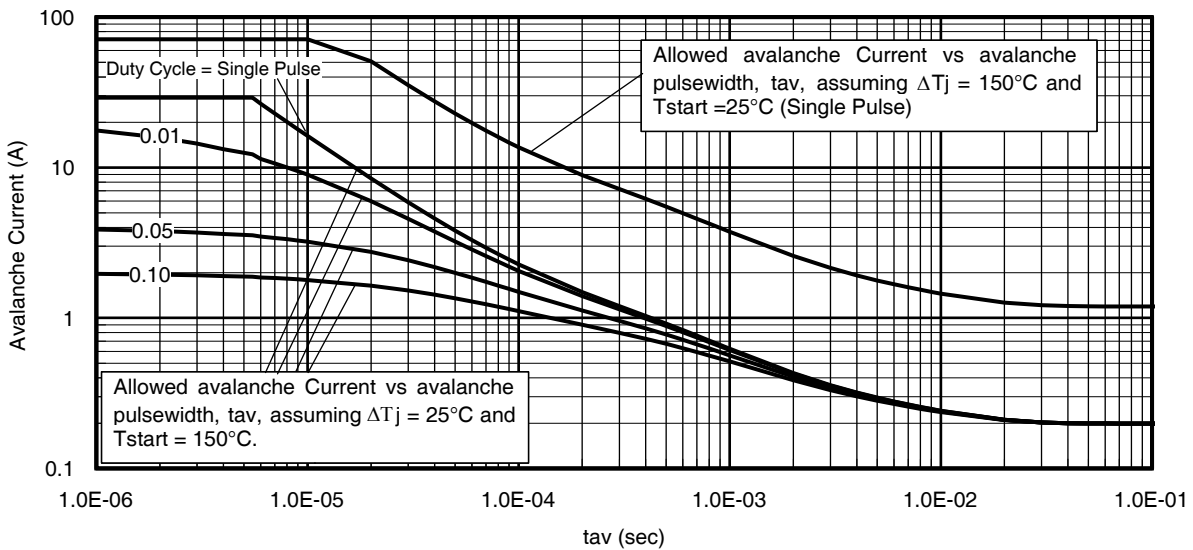
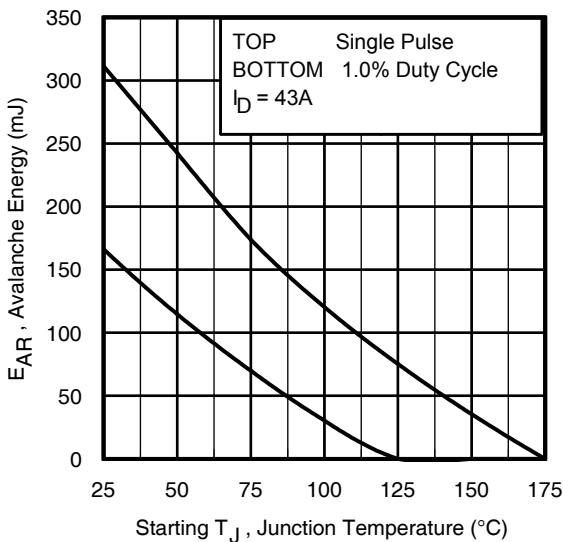
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.34mH  
R<sub>G</sub> = 50Ω, I<sub>AS</sub> = 43A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ④ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C.

- ⑤ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.


**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature

**Fig. 5.** Typical Capacitance vs. Drain-to-Source Voltage

**Fig. 6.** Typical Gate Charge vs. Gate-to-Source Voltage


**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

**Fig. 8.** Maximum Safe Operating Area

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10.** Drain-to-Source Breakdown Voltage

**Fig 11.** Typical  $C_{oss}$  Stored Energy

**Fig 12.** Maximum Avalanche Energy vs. Drain Current


**Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 14. Typical Avalanche Current vs. Pulsewidth**

**Fig 15. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves, Figures 13, 14:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

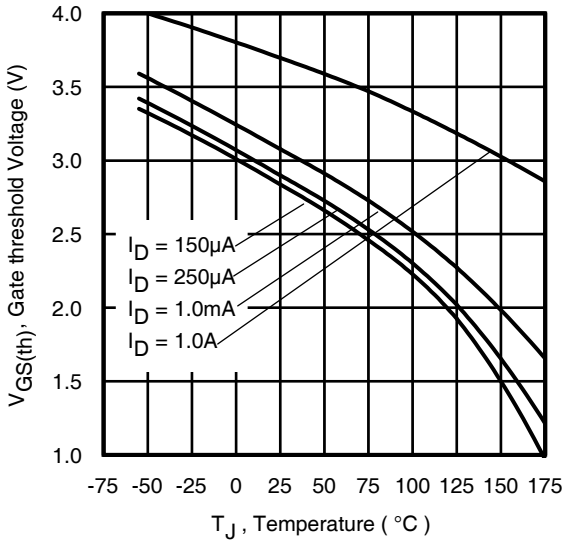


Fig 16. Threshold Voltage vs. Temperature

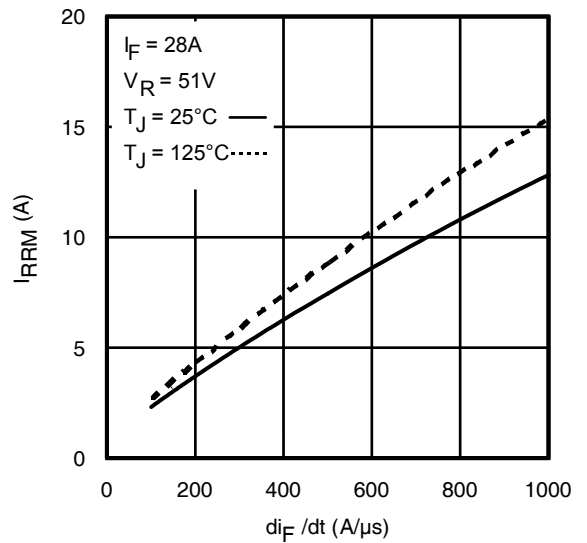


Fig 17. Typical Recovery Current vs. dif/dt

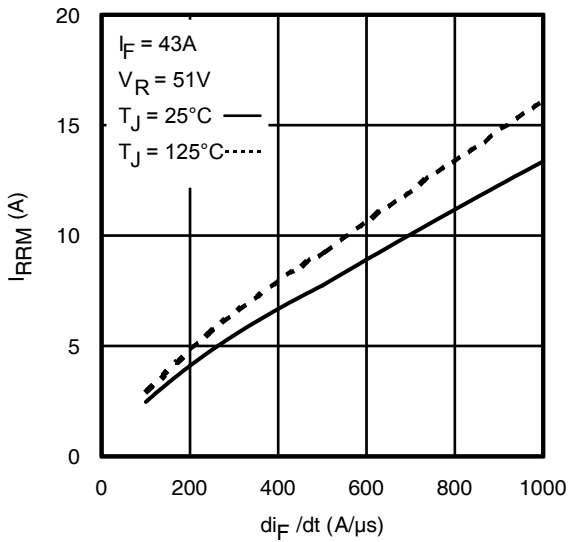


Fig. 18 - Typical Recovery Current vs. dif/dt

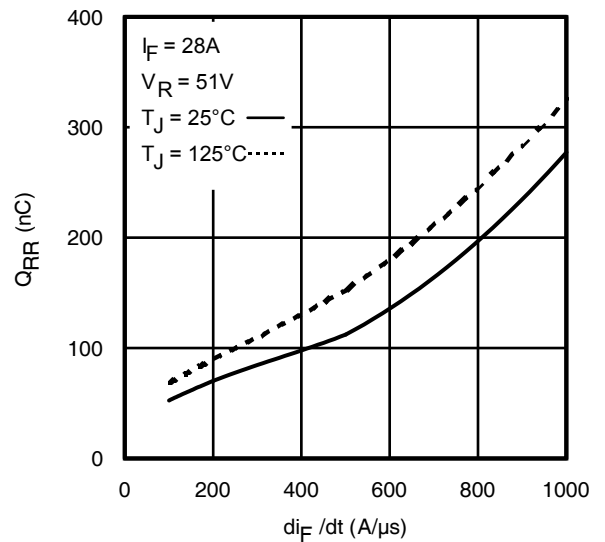


Fig. 19 - Typical Stored Charge vs. dif/dt

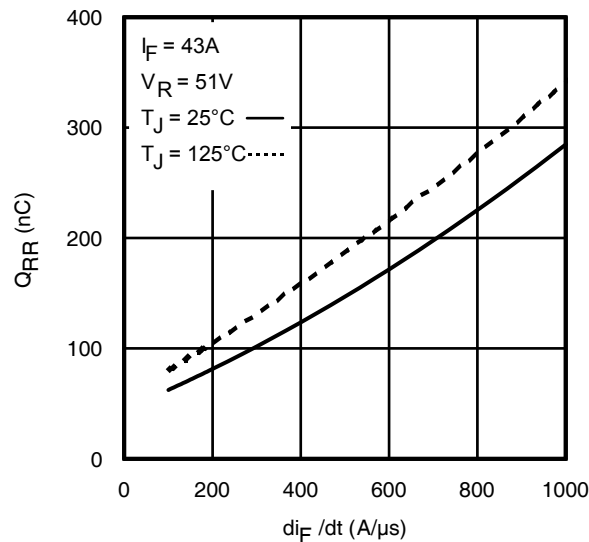
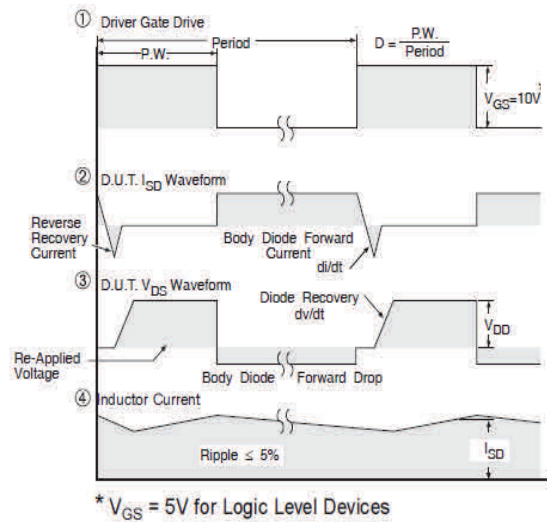
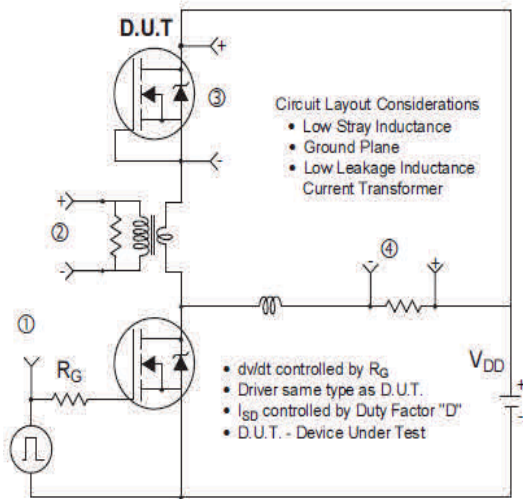
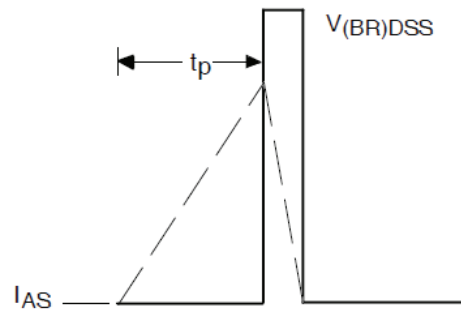
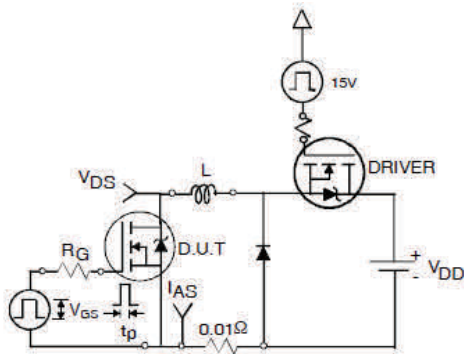
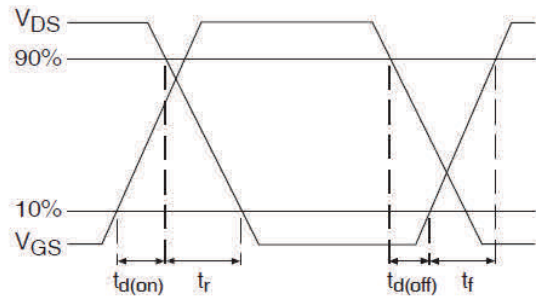
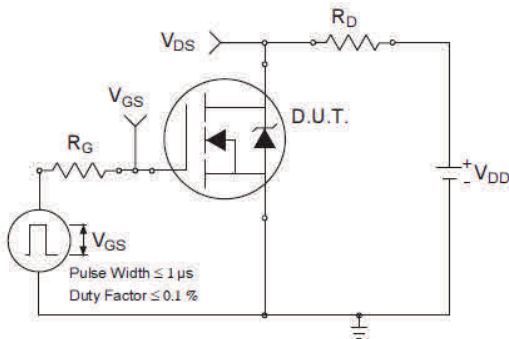
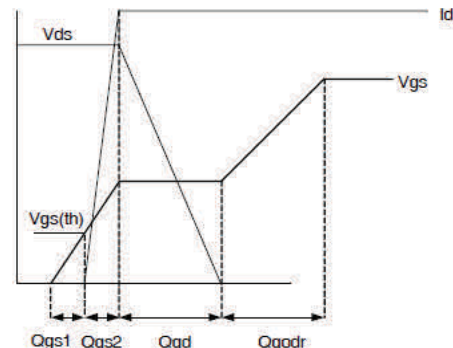
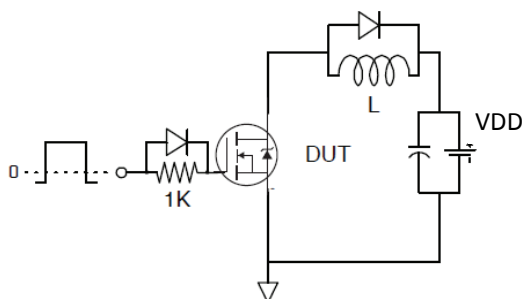
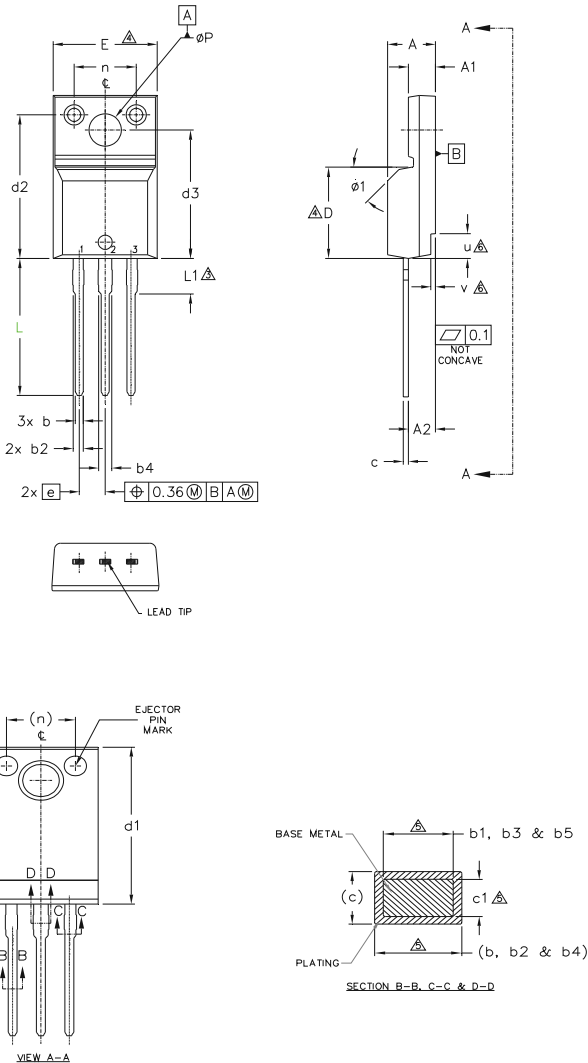


Fig. 20 - Typical Stored Charge vs. dif/dt


**Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 22a. Unclamped Inductive Test Circuit**
**Fig 22b. Unclamped Inductive Waveforms**

**Fig 23a. Switching Time Test Circuit**
**Fig 23b. Switching Time Waveforms**

**Fig 24a. Gate Charge Test Circuit**
**Fig 24b. Gate Charge Waveform**

**TO-220 Full-Pak Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.0 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3.0 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTER MOST EXTREMES OF THE PLASTIC BODY.
- 5.0 DIMENSION b1, b3, b5 & c1 APPLY TO BASE METAL ONLY.
- 6.0 STEP OPTIONAL ON PLASTIC BODY DEFINED BY DIMENSIONS u & v.
- 7.0 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.57	4.83	.180	.190	5
A1	2.57	2.82	.101	.111	
A2	2.51	2.92	.099	.115	
b	0.61	0.94	.024	.037	
b1	0.61	0.89	.024	.035	
b2	0.76	1.27	.030	.050	
b3	0.76	1.22	.030	.048	
b4	1.02	1.52	.040	.060	
b5	1.02	1.47	.040	.058	
c	0.33	0.63	.013	.025	
c1	0.33	0.58	.013	.023	5
D	8.66	9.80	.341	.386	4
d1	15.80	16.13	.622	.635	4
d2	13.97	14.22	.550	.560	
d3	12.29	12.93	.484	.509	
E	9.63	10.74	.379	.423	
e	2.54 BSC		.100 BSC		
L	13.21	13.72	.520	.540	3
L1	3.10	3.68	.122	.145	
n	6.05	6.60	.238	.260	
$\phi P$	3.05	3.45	.120	.136	6
u	2.39	2.49	.094	.098	
v	0.41	0.51	.016	.020	
$\phi 1$	—	45*	—	45*	6

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

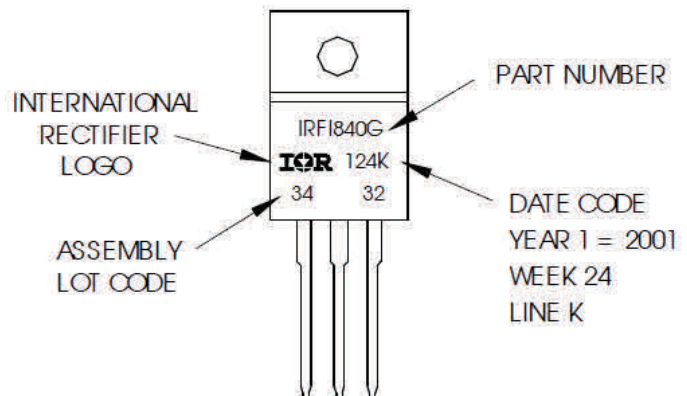
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

**TO-220 Full-Pak Part Marking Information**

EXAMPLE: THIS IS AN IRFI840G  
WITH ASSEMBLY  
LOT CODE 3432  
ASSEMBLED ON WW 24, 2001  
IN THE ASSEMBLY LINE "K"

Note: "P" in assembly line position  
indicates "Lead-Free"



TO-220AB Full-Pak packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification information**

Qualification level	Industrial	
	(per JEDEC JESD47F † guidelines )	
Moisture Sensitivity Level	TO-220 Full-Pak	N/A
		(per JEDEC J-STD-020D†)
RoHS compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
10/07/2013	<ul style="list-style-type: none"> <li>Removed the “Silicon Limited” from the ID rating, on page 1.</li> </ul>
04/27/2017	<ul style="list-style-type: none"> <li>Changed datasheet with Infineon logo - all pages.</li> <li>Corrected Package Outline on page 8.</li> <li>Added disclaimer on last page.</li> </ul>

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