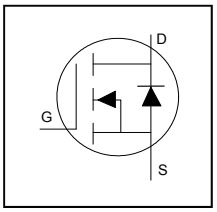
International
IOR Rectifier

IRFP4127PbF

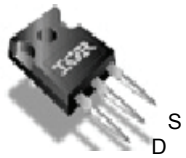
HEXFET® Power MOSFET

Application
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



V_{DSS}	200V
$R_{DS(on)}$ typ.	17mΩ
max	21mΩ
I_D	75A

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



TO-247AC

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFP4127PbF	TO-247AC	Tube	25	IRFP4127PbF

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	75	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	53	
I_{DM}	Pulsed Drain Current ①	300	
P_D @T_C = 25°C	Maximum Power Dissipation	341	W
	Linear Derating Factor	2.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt③	57	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf·in (1.1 N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	244	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	–––	0.4	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.24	–––	
$R_{\theta JA}$	Junction-to-Ambient ⑦⑧	–––	40	

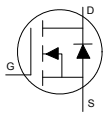
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.23	—	V/°C	Reference to 25°C, I_D = 5mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	17	21	mΩ	V_{GS} = 10V, I_D = 44A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 200 V, V_{GS} = 0V
		—	—	250		V_{DS} =200V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
R_G	Gate Resistance	—	3.0	—	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

gfs	Forward Transconductance	45	—	—	S	V_{DS} = 50V, I_D =44A
Q_g	Total Gate Charge	—	100	150	nC	I_D = 44A
Q_{gs}	Gate-to-Source Charge	—	30	—		V_{DS} = 100V
Q_{gd}	Gate-to-Drain Charge	—	31	—		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	—	69	—		I_D = 44A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	V_{DD} = 100V
t_r	Rise Time	—	18	—		I_D = 44A
$t_{d(off)}$	Turn-Off Delay Time	—	56	—		R_G= 2.7Ω
t_f	Fall Time	—	22	—		V_{GS} = 10V
C_{iss}	Input Capacitance	—	5380	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	410	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	86	—		f = 1.0MHz
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	—	360	—		V_{GS} = 0V, VDS = 0V to 160V⑥ See Fig.11
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	—	590	—		V_{GS} = 0V, VDS = 0V to 160V⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode) ①	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	300		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 44A,V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	136	—	ns	T_J = 25°C V_{DD} = 100V
		—	139	—		T_J = 125°C I_F = 44A,
Q_{rr}	Reverse Recovery Charge	—	458	—	nC	T_J = 25°C di/dt = 100A/µs ④
		—	688	—		T_J = 125°C
I_{RRM}	Reverse Recovery Current	—	8.3	—	A	T_J = 25°C

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Recommended max EAS limit, starting T_J = 25°C, L = 0.25mH, R_G = 25Ω, I_{AS} = 44A, V_{GS} =10V.

③ $I_{SD} \le 44A$, di/dt ≤ 760A/µs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 175°C$.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

⑧ Rθ is measured at T_J approximately 90°C

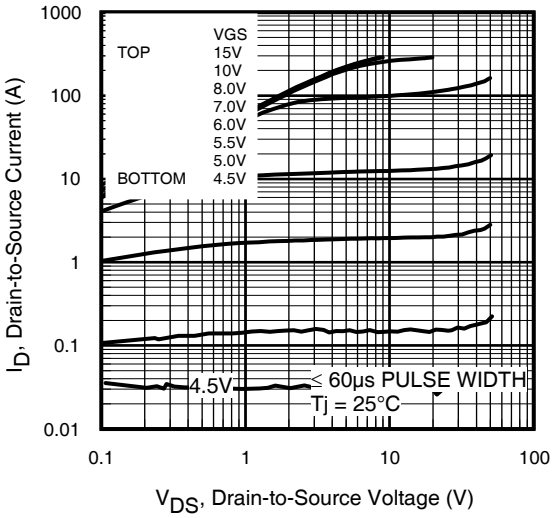


Fig 1. Typical Output Characteristics

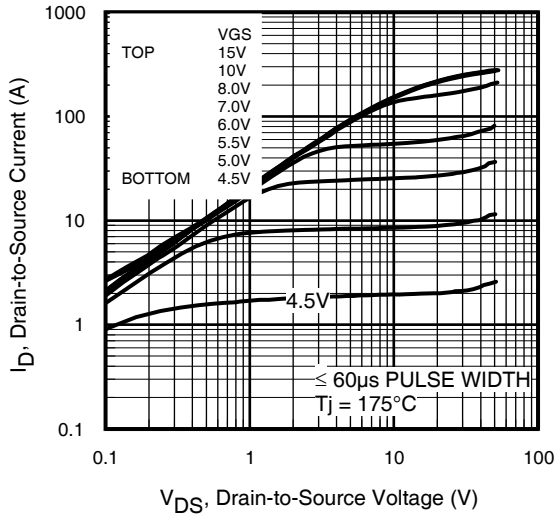


Fig 2. Typical Output Characteristics

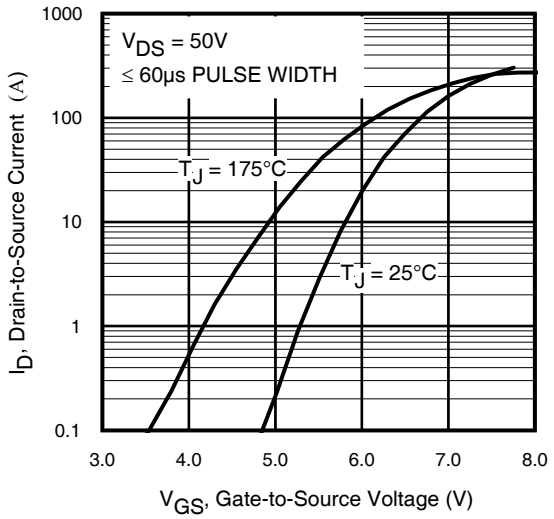


Fig 3. Typical Transfer Characteristics

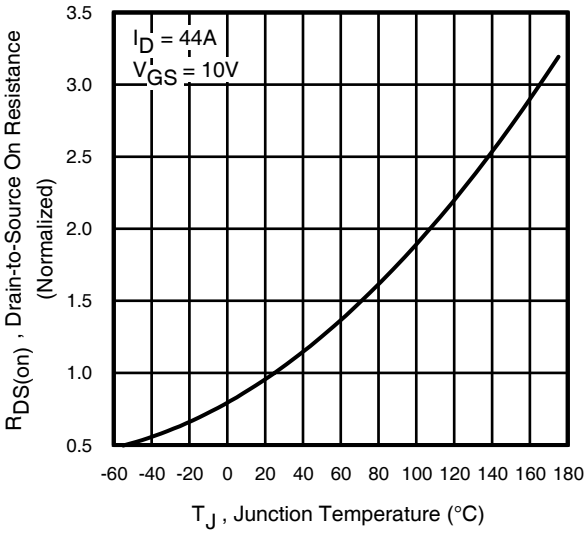


Fig 4. Normalized On-Resistance vs. Temperature

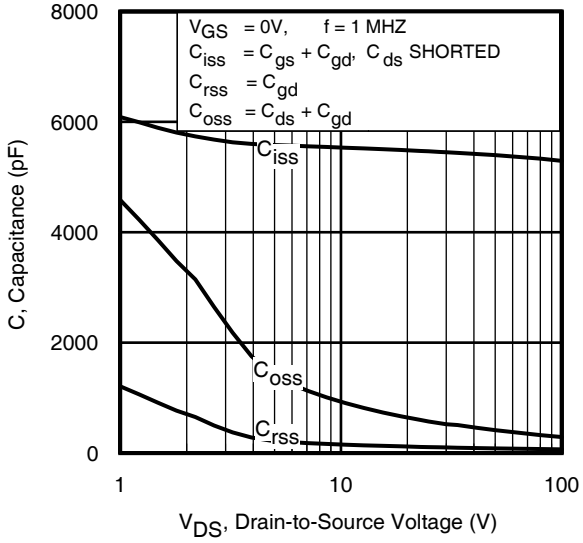


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

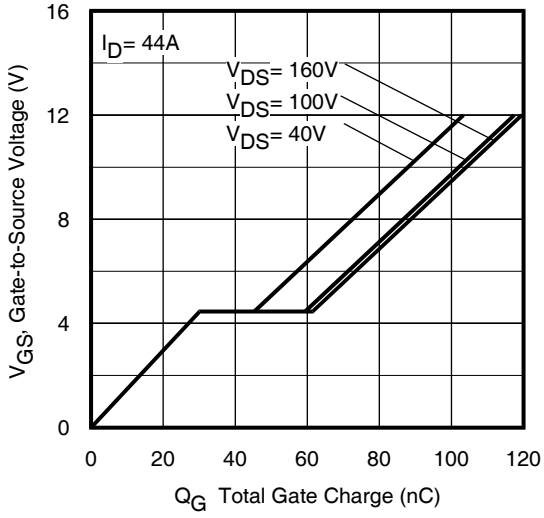


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

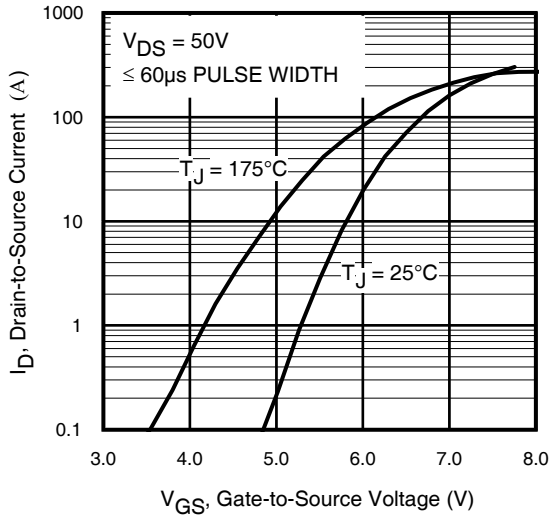


Fig 7. Typical Source-Drain Diode Forward Voltage

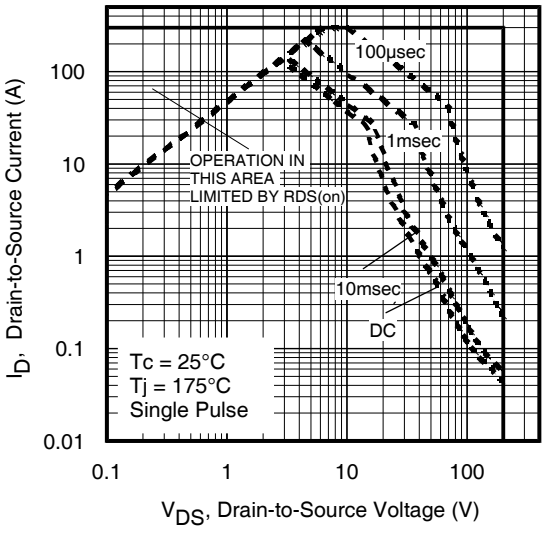


Fig 8. Maximum Safe Operating Area

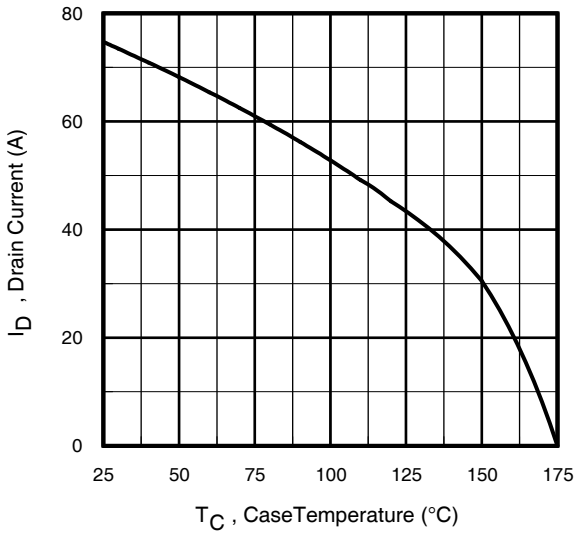


Fig 9. Maximum Drain Current vs. Case Temperature

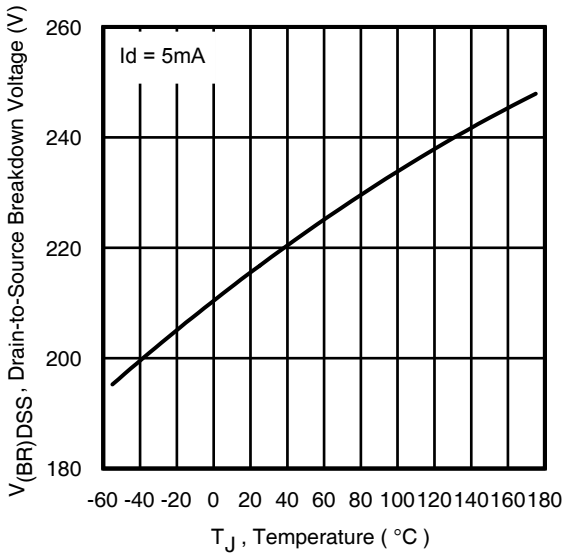


Fig 10. Drain-to–Source Breakdown Voltage

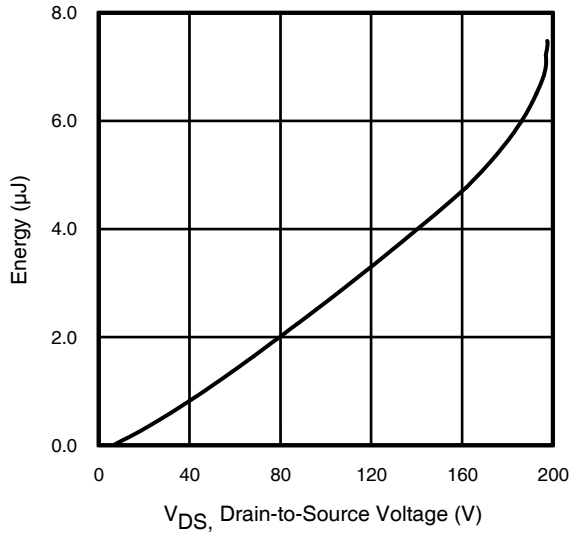


Fig 11. Typical C_{oss} Stored Energy

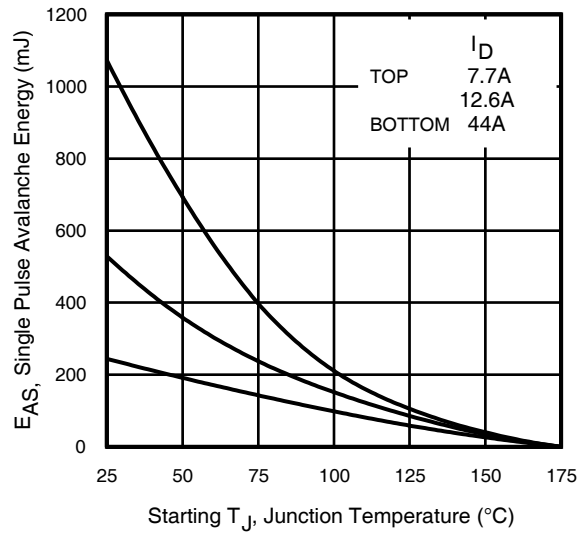


Fig 12. Maximum Avalanche Energy vs. Drain Current

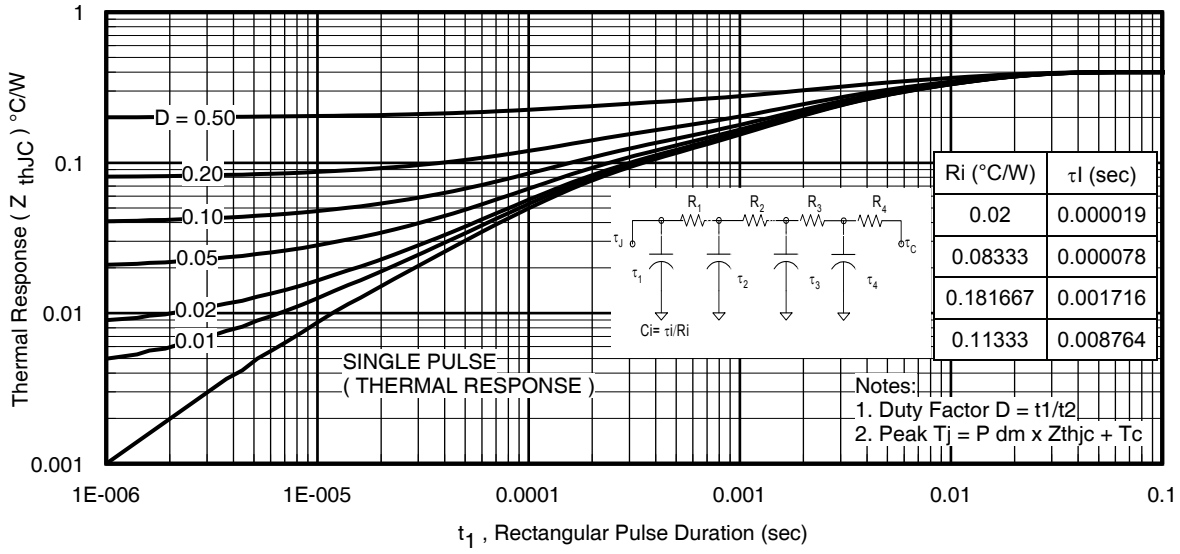


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

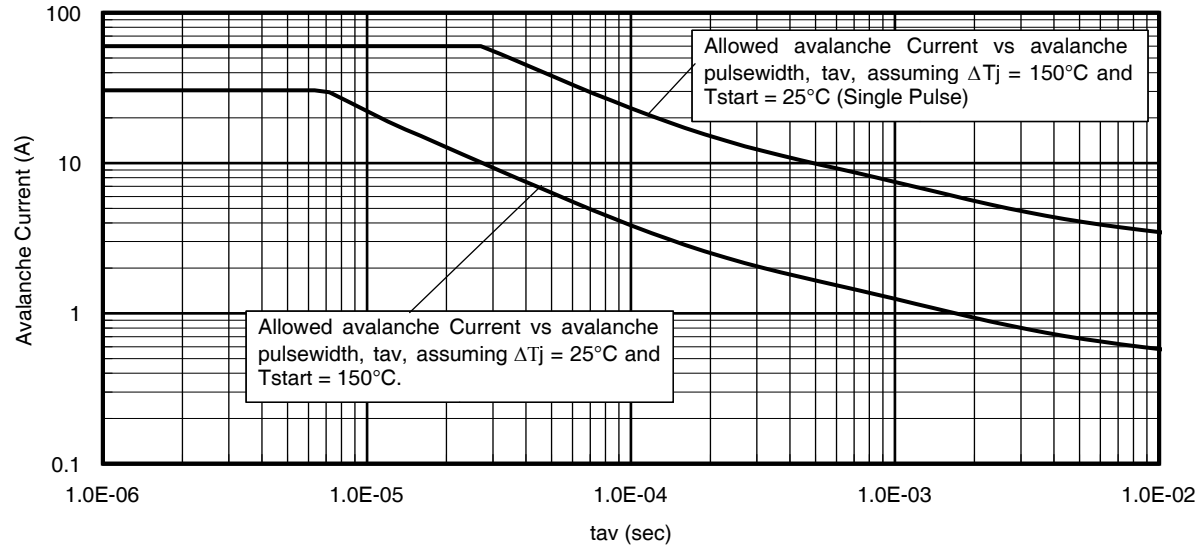
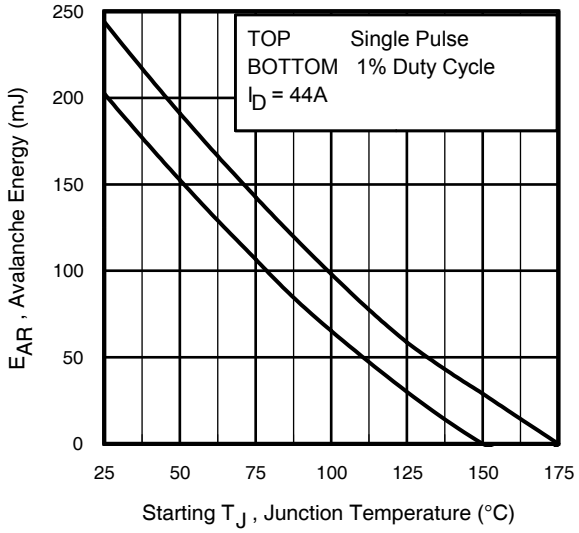


Fig 14. Typical Avalanche Current vs. Pulse Width



Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Fig 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Fig 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Fig 13.

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

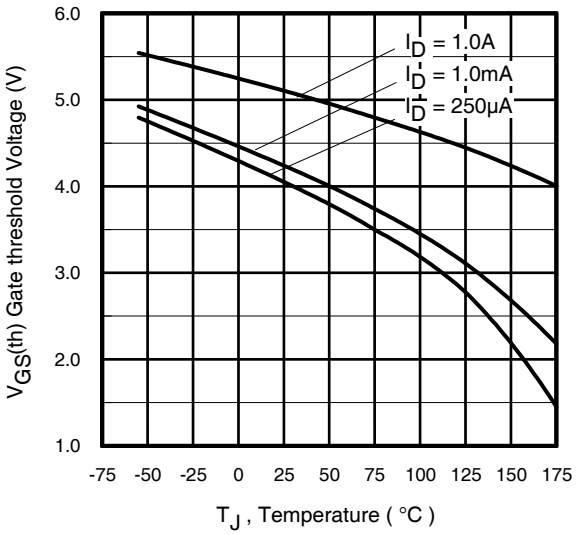


Fig 16. Threshold Voltage vs. Temperature

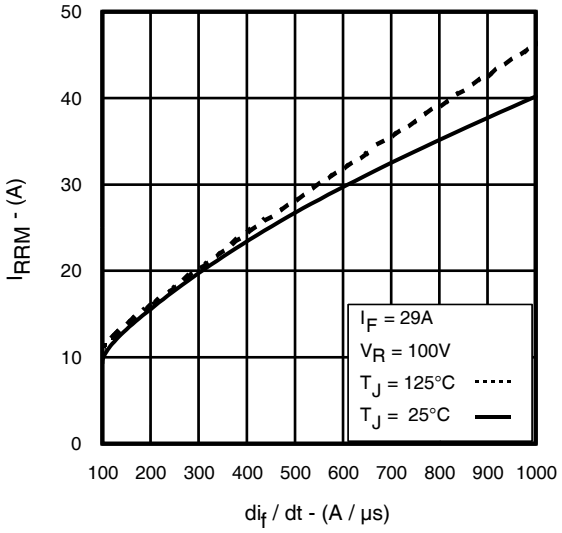


Fig 17. Typical Recovery Current vs. dif/dt

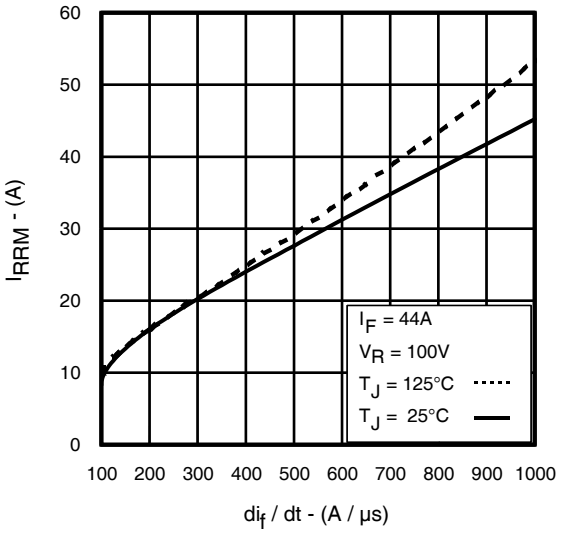


Fig 18. Typical Recovery Current vs. dif/dt

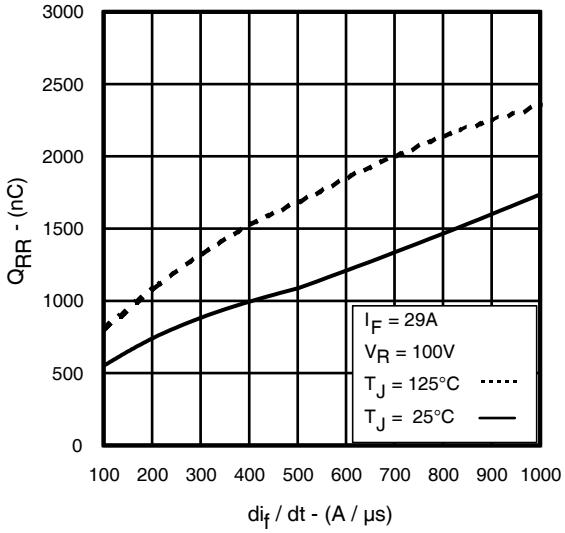


Fig 19. Typical Stored Charge vs. dif/dt

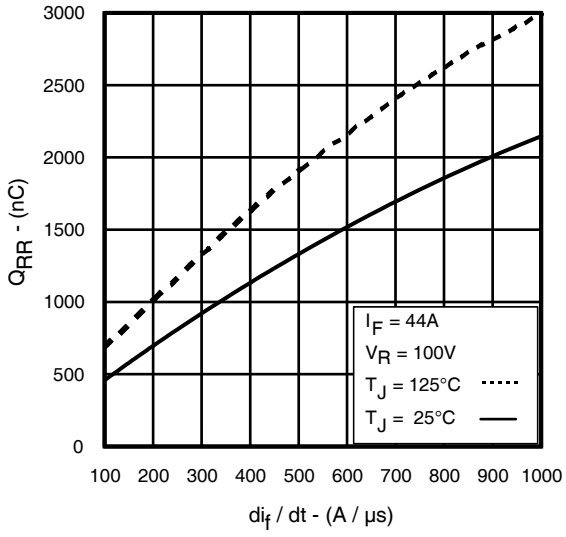


Fig 20. Typical Stored Charge vs. dif/dt

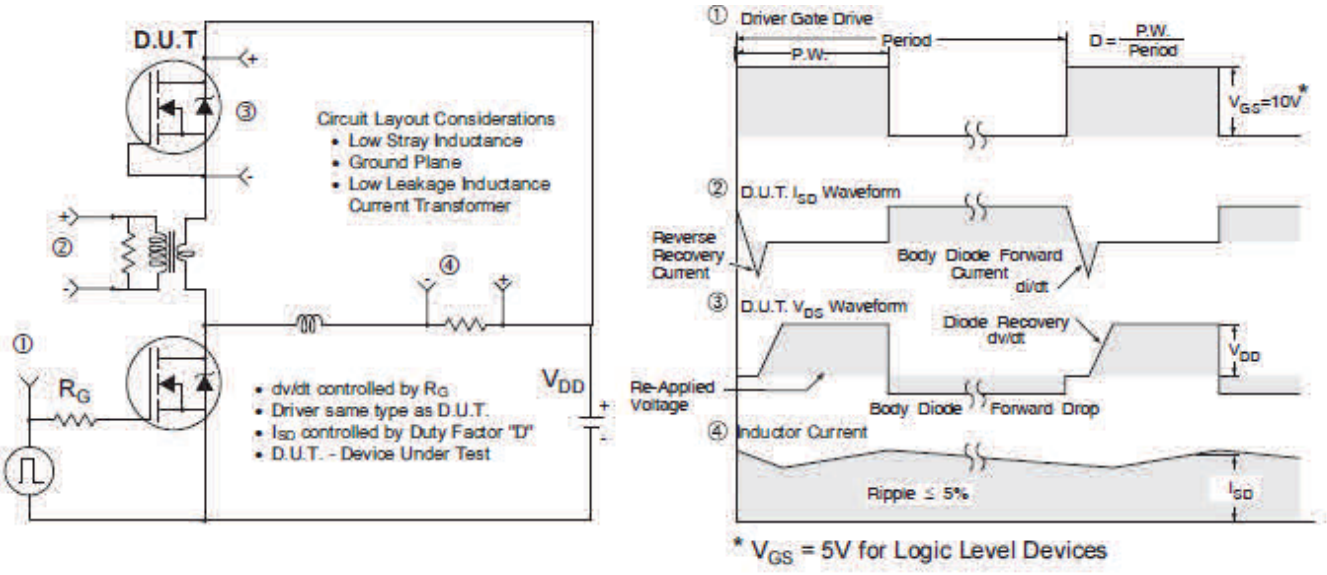


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

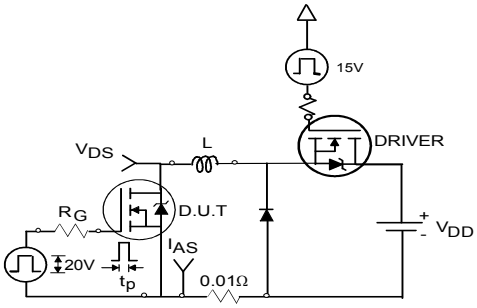


Fig 22a. Unclamped Inductive Test Circuit

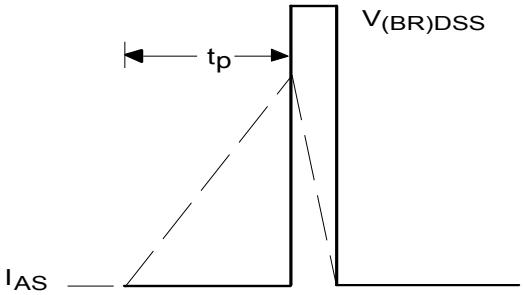


Fig 22b. Unclamped Inductive Waveforms

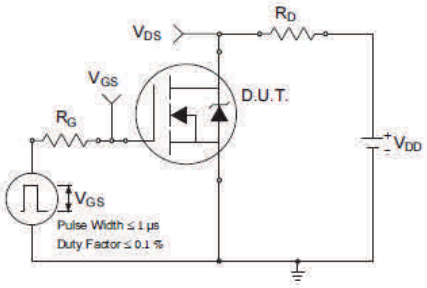


Fig 23a. Switching Time Test Circuit

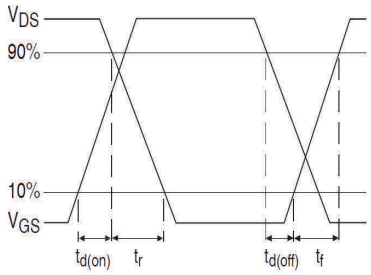


Fig 23b. Switching Time Waveforms

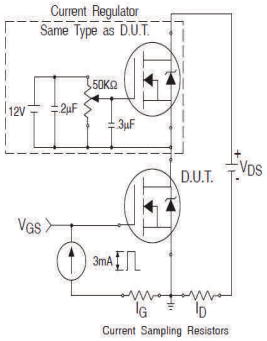


Fig 24a. Gate Charge Test Circuit

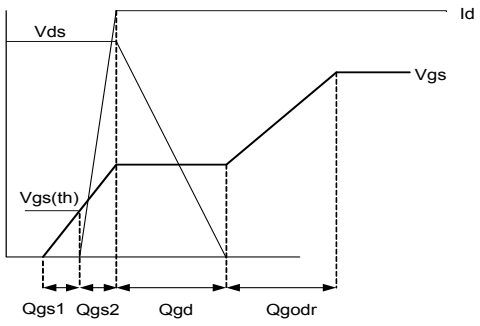
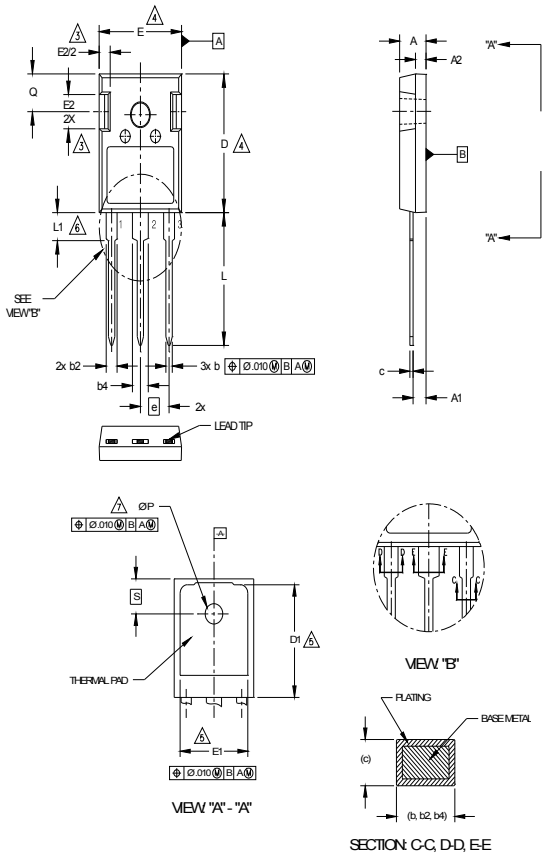


Fig 24b. Gate Charge Waveform

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.190	.204	4.83	5.20	
A1	.090	.100	2.29	2.54	
A2	.075	.085	1.91	2.16	
b	.042	.052	1.07	1.33	
b2	.075	.094	1.91	2.41	
b4	.113	.133	2.87	3.38	
c	.022	.026	0.55	0.68	
D	.819	.830	20.80	21.10	4
D1	.640	694	16.25	17.65	5
E	.620	.635	15.75	16.13	4
E1	.512	.570	13.00	14.50	
E2	.145	.196	3.68	5.00	
e	.215 Typical		5.45 Typical		
L	.780	.800	19.80	20.32	
L1	.161	.173	4.10	4.40	
ø P	.138	.143	3.51	3.65	
Q	.216	.236	5.49	6.00	
S	.238	.248	6.04	6.30	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

NOTES:

1 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.

2 DIMENSIONS ARE SHOWN IN INCHES AND MILLIMETERS.

3 CONTOUR OF SLOT OPTIONAL.

4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

5 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.

6 LEAD FINISH UNCONTROLLED IN L1.

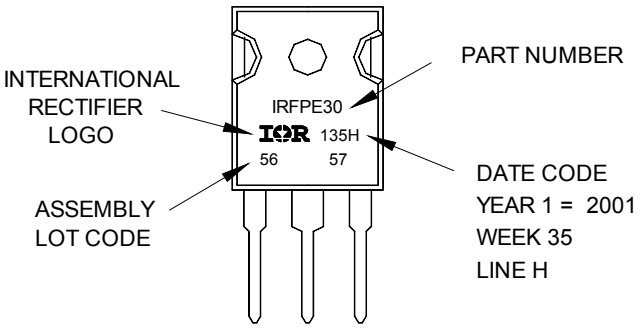
7 ø P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.

TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AC package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	TO-247AC	N/A
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International
IOR Rectifier

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