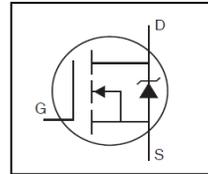


- Surface Mount
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

HEXFET® Power MOSFET



<b>V<sub>DSS</sub></b>	<b>55V</b>
<b>R<sub>DS(on)</sub></b>	<b>0.065Ω</b>
<b>I<sub>D</sub></b>	<b>3.1A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

**Description**

Fifth Generation HEXFETs utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The SOT-223 package is designed for surface-mount using vapor phase, infra red, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heat sinking. Power dissipation of 1.0W is possible in a typical surface mount application.

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRLL024NTRPbF	SOT-223	Tape and Reel	2500	IRLL024NTRPbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V **	4.4	A
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V *	3.1	
I <sub>D</sub> @ T <sub>A</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V *	2.5	
I <sub>DM</sub>	Pulsed Drain Current ①	12	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation (PCB Mount) **	2.1	W
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation (PCB Mount) *	1.0	
	Linear Derating Factor (PCB Mount) *	8.3	mW/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 16	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	120	mJ
I <sub>AR</sub>	Avalanche Current ①	3.1	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①*	0.1	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount, steady state) *	90	120	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount, steady state) **	50	60	

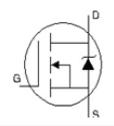
\* When mounted on FR-4 board using minimum recommended footprint.

\*\* When mounted on 1 inch square copper board, for comparison with other SMD devices.

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

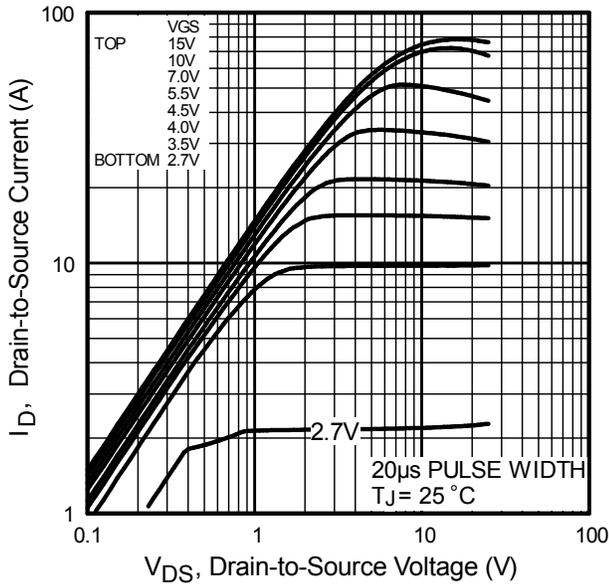
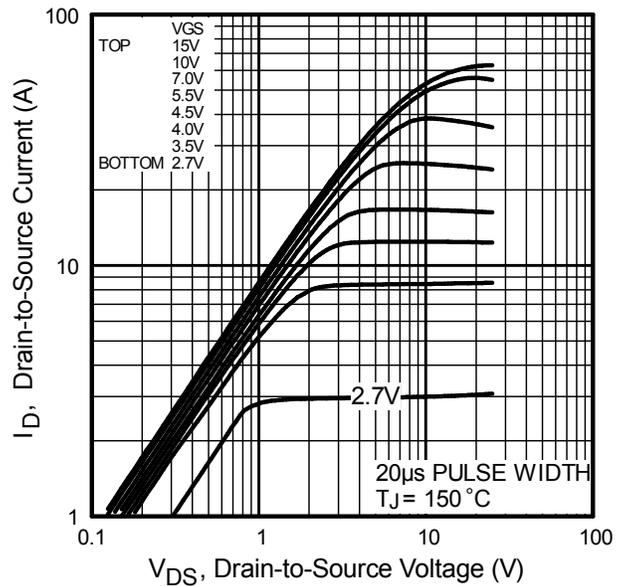
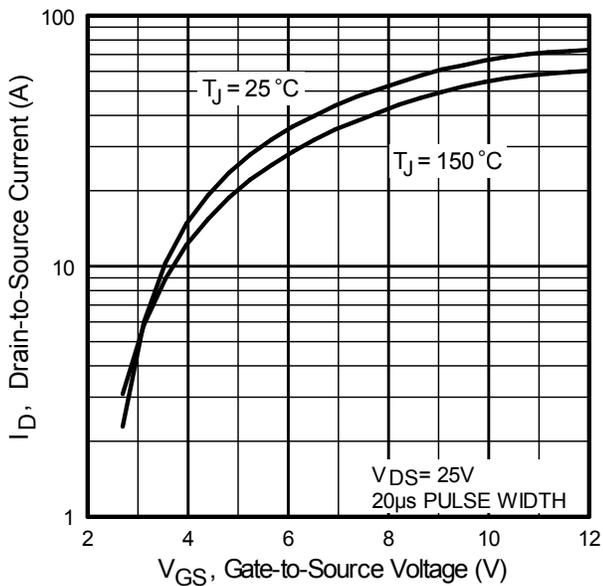
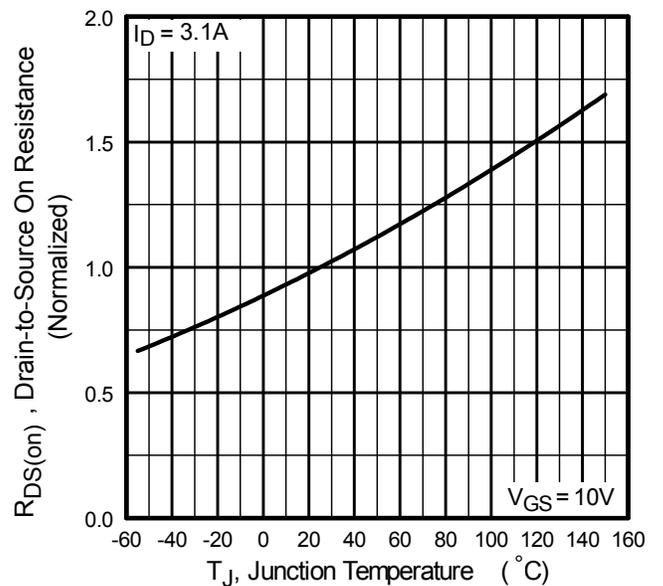
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.048	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.065	$\Omega$	$V_{GS} = 10V, I_D = 3.1A$ ④
		—	—	0.080		$V_{GS} = 5.0V, I_D = 2.5A$ ④
		—	—	0.100		$V_{GS} = 4.0V, I_D = 1.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Trans conductance	3.3	—	—	S	$V_{DS} = 25V, I_D = 1.9A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
$Q_g$	Total Gate Charge	—	10.4	15.6	nC	$I_D = 1.9A$
$Q_{gs}$	Gate-to-Source Charge	—	1.5	2.3		$V_{DS} = 44V$
$Q_{gd}$	Gate-to-Drain Charge	—	5.5	8.3		$V_{GS} = 5.0V$ , See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.4	—		ns
$t_r$	Rise Time	—	21	—	$I_D = 1.9A$	
$t_{d(off)}$	Turn-Off Delay Time	—	18	—	$R_G = 24\Omega$	
$t_f$	Fall Time	—	25	—	$R_D = 15\Omega$ , See Fig. 10 ④	
$C_{iss}$	Input Capacitance	—	510	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	140	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	58	—		$f = 1.0\text{MHz}$ , See Fig. 5

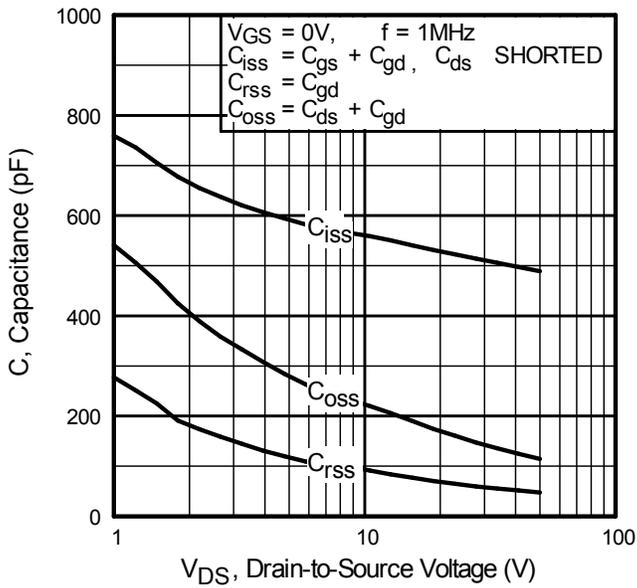
**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	12		
$V_{SD}$	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 1.9A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	39	58	ns	$T_J = 25^\circ\text{C}, I_F = 1.9A$
$Q_{rr}$	Reverse Recovery Charge	—	63	94	nC	$di/dt = 100A/\mu s$ ④

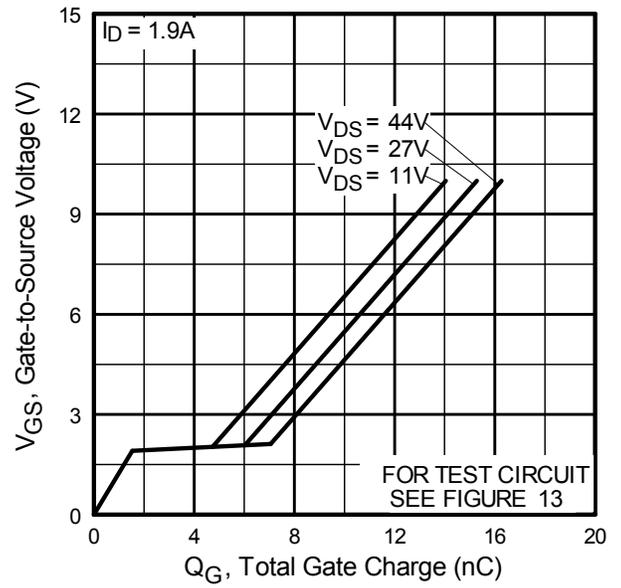
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② starting  $T_J = 25^\circ\text{C}$ ,  $L = 25\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 3.1A$  (See fig. 12)
- ③  $I_{SD} \leq 1.9A$ ,  $di/dt \leq 270A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

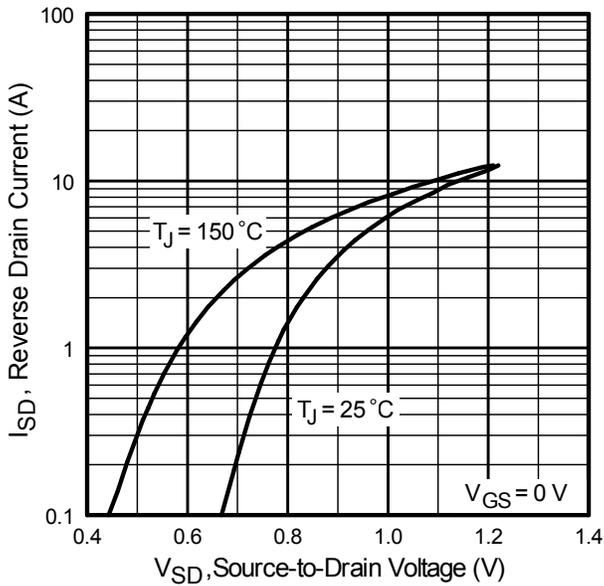

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature



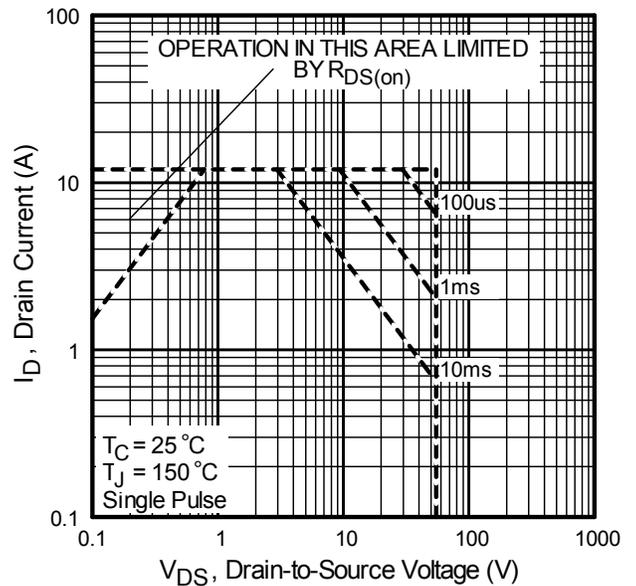
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



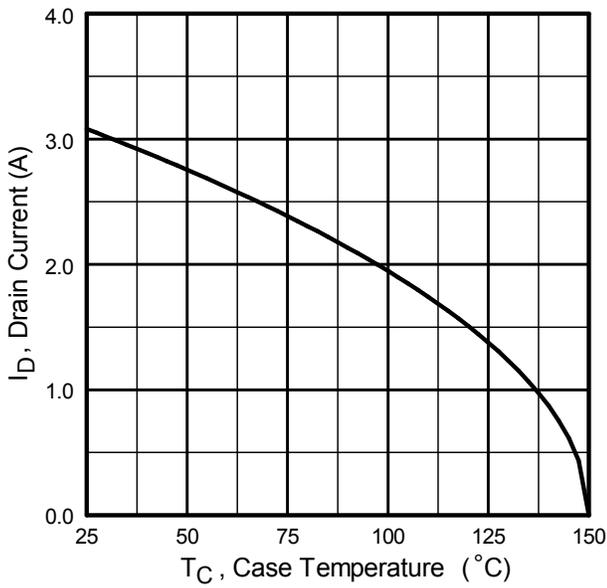
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



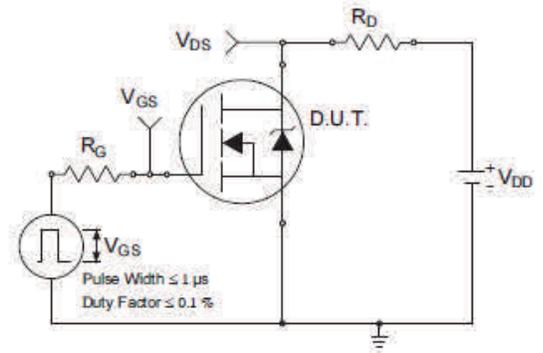
**Fig 7** Typical Source-to-Drain Diode Forward Voltage



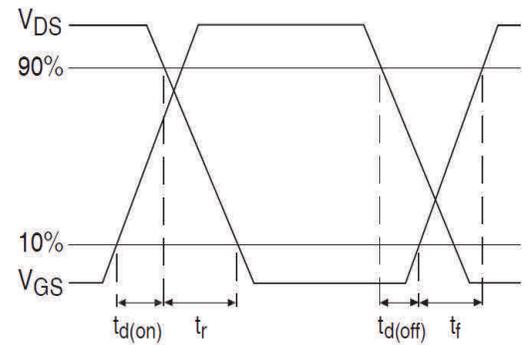
**Fig 8.** Maximum Safe Operating Area



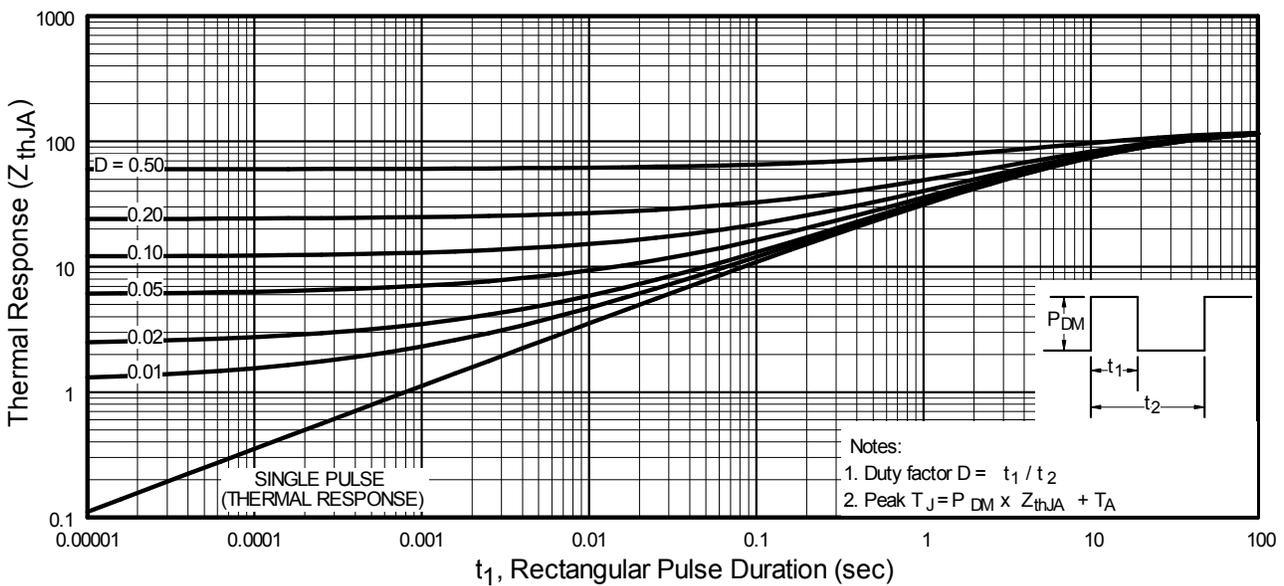
**Fig 9.** Maximum Drain Current Vs. Case Temperature



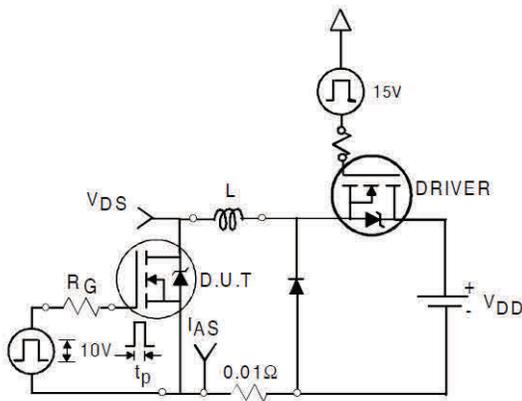
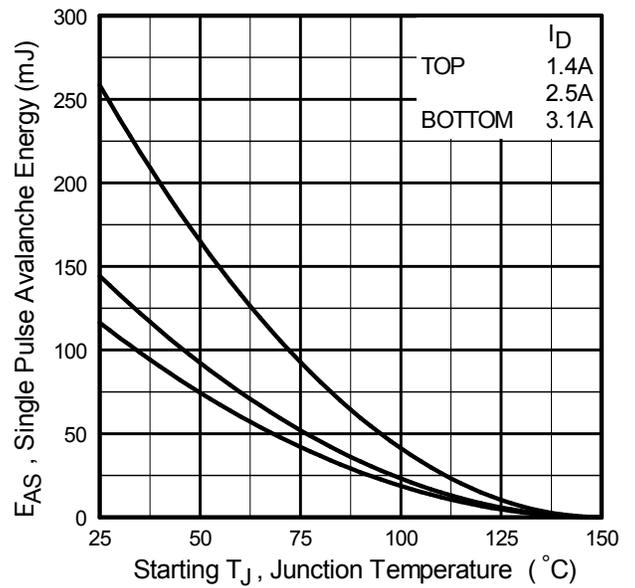
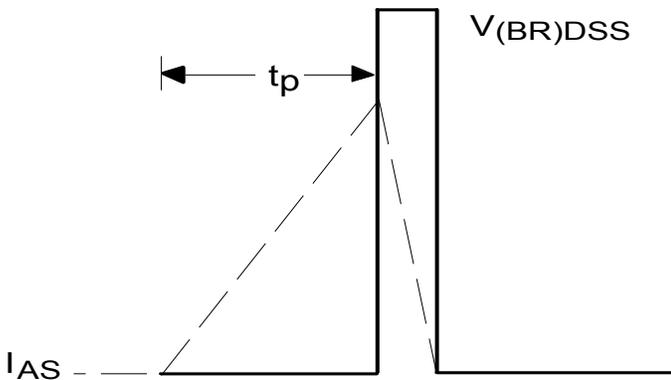
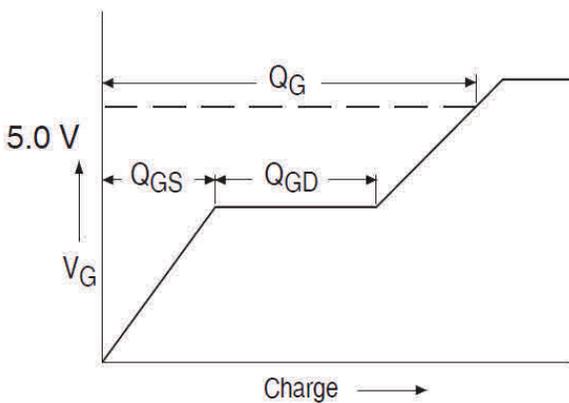
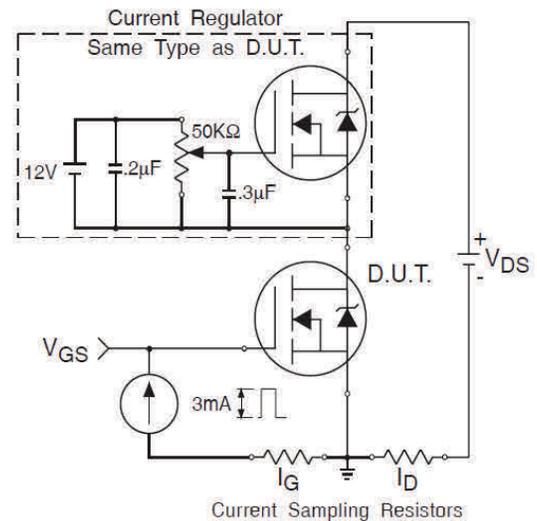
**Fig 10a.** Switching Time Test Circuit

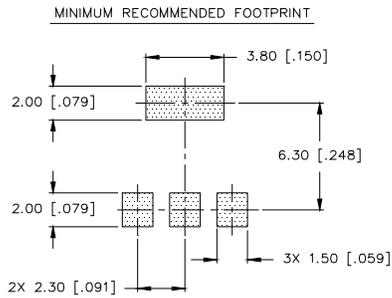
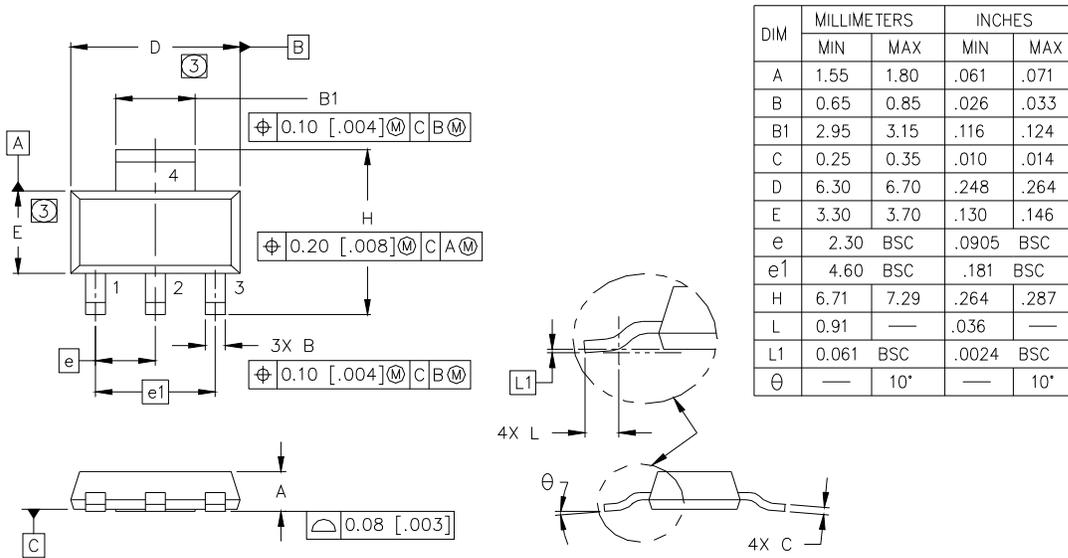


**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

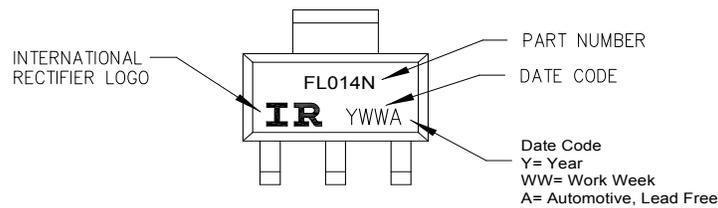
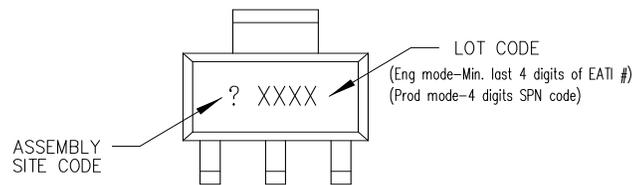

**Fig 12a. Unclamped Inductive Test Circuit**

**Fig 12c. Maximum Avalanche Energy vs. Drain Current**

**Fig 12b. Unclamped Inductive Waveforms**

**Fig 13a. Basic Gate Charge Waveform**

**Fig 13b. Gate Charge Test Circuit**

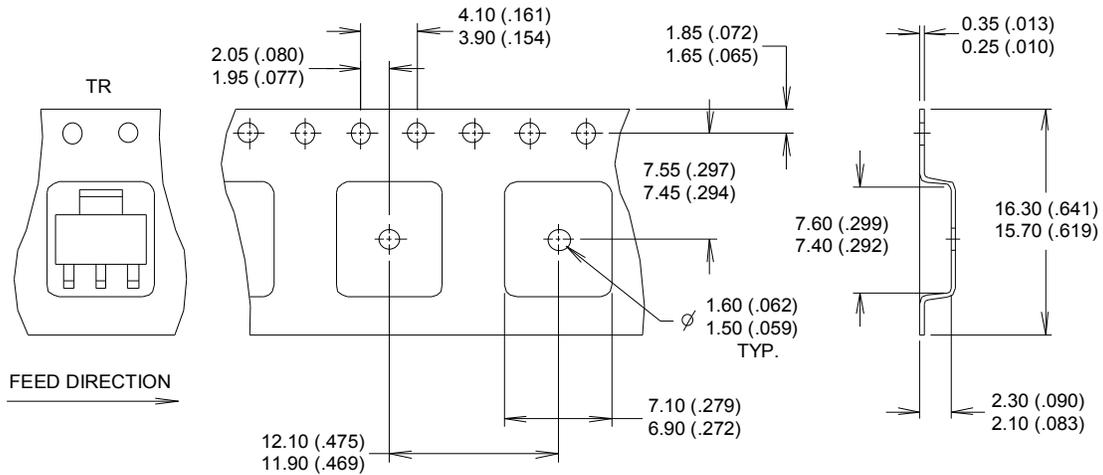
**SOT-223 (TO-261AA) Package Outline** (Dimensions are shown in millimeters (inches))

**LEAD ASSIGNMENTS**

- 1 = GATE
- 2 = DRAIN
- 3 = SOURCE
- 4 = DRAIN

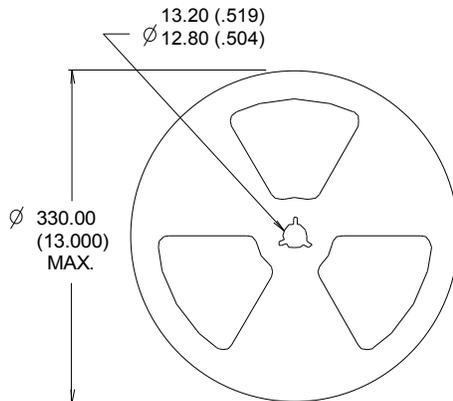
**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
- ③ DIMENSIONS DO NOT INCLUDE MOLD FLASH.
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-261AA.
5. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

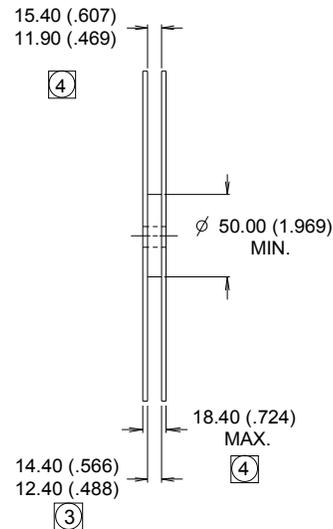
**SOT-223(TO-261AA) Part Marking Information**

**TOP MARKING**

**BOTTOM MARKING**

**SOT-223(TO-261AA) Tape and Reel** (Dimensions are shown in millimeters (inches))

**NOTES :**

1. CONTROLLING DIMENSION: MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.
3. EACH  $\varnothing 330.00$  (13.00) REEL CONTAINS 2,500 DEVICES.


**NOTES :**

1. OUTLINE COMFORMS TO EIA-418-1.
2. CONTROLLING DIMENSION: MILLIMETER..
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.



Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

**Qualification Information**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) †	
<b>Moisture Sensitivity Level</b>	SOT-223	MSL1 (per JEDEC J-STD-020D) †
<b>RoHS Compliant</b>	Yes	

† Applicable version of JEDEC standard at the time of product release (04/27/2004).

**Revision History**

Date	Comments
01/28/2019	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template.</li> <li>Added disclaimer on last page.</li> <li>Corrected part number from "IRLL024NPbF" to "IRLL024NTRPbF"-all pages</li> </ul>

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**Edition 2016-04-19**

**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

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