ISL28130, ISL28230, ISL28430

Single, Dual, and Quad Micropower, Low Drift, RRIO Operational Amplifiers

The ISL28130, ISL28230, and ISL28430 are single, dual and quad micropower, low offset drift operational amplifiers that are optimized for single and dual supply operation from 1.8V to 5.5V and ±0.9V to ±2.75V. Their low supply current of 20µA and rail-to-rail input/output enable the ISL28130, ISL28230, and ISL28430 to be an excellent general-purpose op amp for a range of applications. The ISL28130, ISL28230, and ISL28430 are ideal for handheld devices that operate off 2AA or single Li-ion batteries.

The ISL28130 is available in industry standard pinouts for 5 Ld SOT-23, 5 Ld SC70, and 8 Ld SOIC packages. The ISL28230 is available in industry standard pinouts for 8 Ld MSOP, 8 Ld SOIC, and 8 Ld DFN packages. The ISL28430 is available in 14 Ld TSSOP and 14 Ld SOIC packages. Commercial devices operate across the temperature range of 0°C to 70°C. Full temperature range devices operate across the temperature range of -40°C to 125°C.

Features

- Low input offset voltage: 40µV, Max.
- Low offset drift: 150nV/°C, Max.
- Input bias current: 250pA, Max.
- Quiescent current (per amplifier): 20µA, typical
- Single supply range: +1.8V to +5.5V
- Dual supply range: ±0.9V to ±2.75V
- Low noise (0.01Hz to 10Hz): 1.1µV_{P-P}, typical
- Rail-to-rail inputs and output

Applications

- Bi-directional current sense
- Temperature measurement
- Medical equipment
- Electronic weigh scales
- Precision/strain gauge sensor
- Precision regulation
- Low Ohmic current sense
- High gain analog front ends

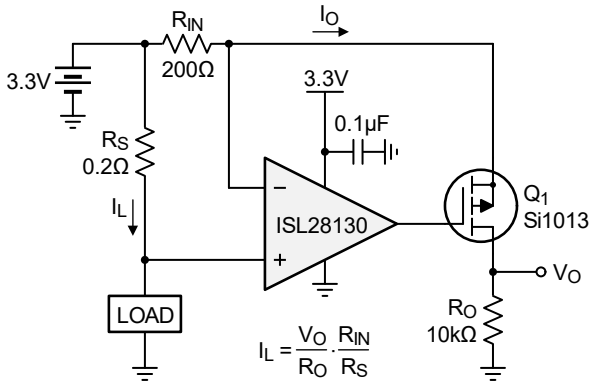


Figure 1. Typical Application Diagram: High-Side CurrentSensing

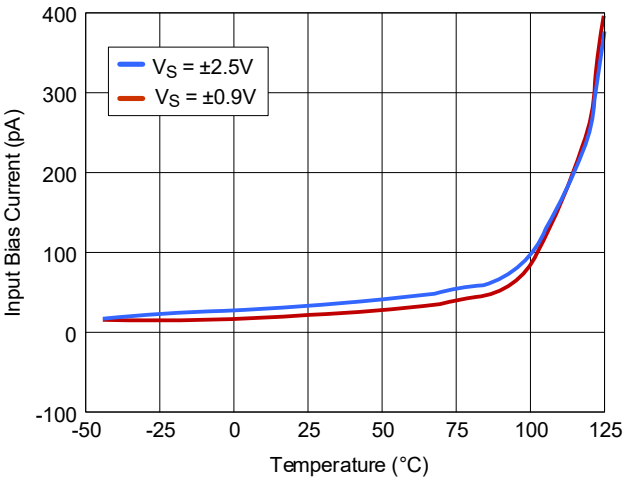


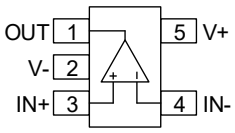
Figure 2. I_B vs Temperature

Contents

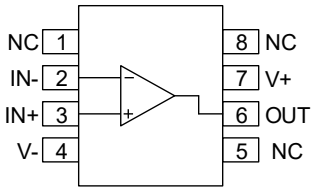
1. Pin Information

1.1 Pin Assignments

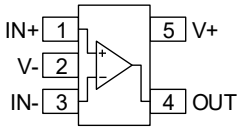
ISL28130



5 Ld SOT-23
Top View

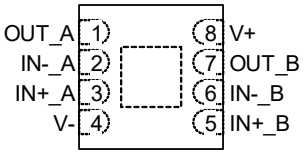


8 Ld SOIC
Top View

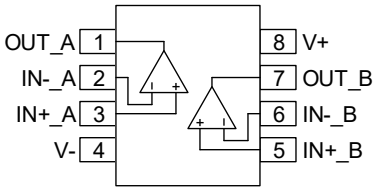


5 ld SC-70
Top View

ISL28230

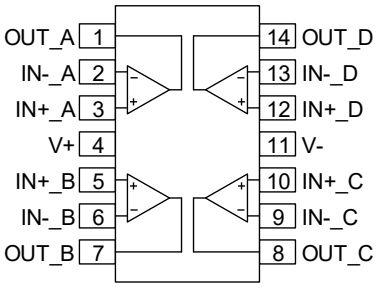


8 ld DFN
Top View



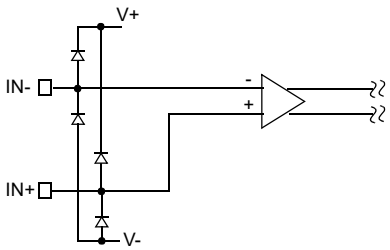
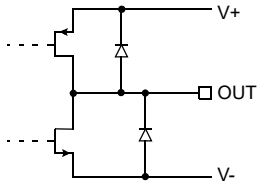
8 Ld MSOP, SOIC
Top View

ISL28430



14 Ld TSSOP, SOIC
Top View

1.2 Pin Descriptions

ISL28130			ISL28230 (8 Ld MSOP, SOIC, DFN)	ISL28430 (14 Ld TSSOP, SOIC)	Pin Name	Function	Equivalent Circuit
5 Ld SOT-23	8 Ld SOIC	5 LD SC-70					
3	3	1	-	-	IN+	Non-inverting input	 Circuit 1
-	-	-	3	3	IN+_A		
-	-	-	5	5	IN+_B		
-	-	-	-	10	IN+_C		
-	-	-	-	12	IN+_D		
2	4	2	4	11	V-	Negative supply	
4	2	3	-	-	IN-	Inverting input	(See Circuit 1)
-	-	-	2	2	IN-_A		
-	-	-	6	6	IN-_B		
-	-	-	-	9	IN-_C		
-	-	-	-	13	IN-_D		
1	6	4	-	-	OUT	Output	 Circuit 2
-	-	-	1	1	OUT_A		
-	-	-	7	7	OUT_B		
-	-	-	-	8	OUT_C		
-	-	-	-	14	OUT_D		
5	7	5	8	4	V+	Positive supply	
-	1, 5, 8	-	-	-	NC	Not Connected – This pin is not electrically connected internally.	
-	-	-	PAD	-	Paddle	Thermal Pad. Connect to most negative supply. DFN packages only.	

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Max Supply Voltage V+ to V-		6.5	V
Max Voltage VIN to GND	V- - 0.3	V+ + 0.3	V
Max Input Differential Voltage		6.5	V
Max Input Current		20	mA
Max Voltage VOUT to GND (10s)	V- - 0.5	V+ + 0.5	V

2.2 ESD Ratings

ESD Model/Test	Rating	Unit
ISL28130		
Human Body Model (Tested per JESD22-A114F)	3	kV
Machine Model (Tested at JESD22-A115B)	200	V
Charged Device Model (Tested per JESD22-C110D)	1.5	kV
ISL28230, ISL28430		
Human Body Model (Tested per JESD22-A114F)	4	kV
Machine Model (Tested at JESD22-A115B)	400	V
Charged Device Model (Tested per JESD22-C110D)	2	kV
Latch-Up (Tested per JESD78B), T_A = 125°C	100	mA

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature Ranges			
Full Grade Devices	-40	+125	°C
Commercial Grade Devices	0	70	°C

2.4 Thermal Specifications

Package Description	Thermal Resistance (Typical)	
	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23[1][2]	225	110
5 Ld SC70[1][2]	206	146
8 Ld SOIC (ISL28130)[1][2]	135	95
8 Ld MSOP [1][2]	180	65

Package Description	Thermal Resistance (Typical)	
	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC (ISL28230)[1][2]	125	90
8 Ld DFN[3][4]	53	12
14 Ld TSSOP[1][2]	110	40
14 Ld SOIC[1][2]	75	47

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.
3. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
4. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.5 Electrical Specifications

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C, R_L = 10kΩ, unless otherwise specified. **Boldface limits apply over the entire operating temperature range.**

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
DC Specifications						
Input Offset Voltage	V_{OS}	Vs = 1.8V to 5.5V	-40	±5	40	µV
		Vs = 1.8 to 5.5V; T = 0°C to +70°C	**-46.8**		**46.8**	µV
		Vs = 1.8V to 5.5V; T = -40°C to +125°C	**-55**		**55**	µV
Input Offset Voltage Temperature Coefficient	TCV_{OS}		**-150**	20	**150**	nV/°C
Input Offset Current	I_{OS}			-60		pA
Input Offset Current Temperature Coefficient	TCI_{OS}			0.11		pA/°C
Input Bias Current	I_B	T = 0°C to +70°C	**-250**		**250**	pA
		T = -40°C to +125°C	**-700**		**700**	pA
Common Mode Input Voltage Range		Assured by CMRR	**-0.1**		**5.1**	V
Common Mode Rejection Ratio	CMRR	V_{CM} = -0.1V to 5.1V	110	125		dB
			105			dB
Power Supply Rejection Ratio	PSRR	Vs = 2.0V to 5.5V	105	138		dB
			105			dB
Output Voltage Swing, High	V_{OH}		**4.950**	4.981		V
Output Voltage Swing, Low	V_{OL}			18	**50**	mV
Open-Loop Gain	A_{OL}	R_L = 1MΩ		150		dB

V_+ = 5V, V_- = 0V, V_{CM} = 2.5V, T_A = +25°C, R_L = 10kΩ, unless otherwise specified. **Boldface limits apply over the entire operating temperature range. (Cont.)**

Parameter	Symbol	Conditions	Min[1]	Typ	Max[1]	Unit
Supply Voltage	V_+	Guaranteed by V_{OS}	**1.8**		**5.5**	V
Supply Current, Per Amplifier	I_S	R_L = OPEN		20	25	µA
					35	µA
Output Source Short-Circuit Current	I_{SC+}	R_L = Short V-		15		mA
Output Sink Short-Circuit Current	I_{SC-}	R_L = Short V+		-15		mA
AC Specifications						
Gain Bandwidth Product	GBWP	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}		400		kHz
Peak-to-Peak Input Noise Voltage	$e_N V_{P-P}$	f = 0.01Hz to 10Hz		1.1		μV_{P-P}
Input Noise Voltage Density	e_N	f = 1kHz		65		nV/√(Hz)
Input Noise Current Density	i_N	f = 1kHz		72		fA/√(Hz)
		f = 10Hz		80		fA/√(Hz)
Differential Input Capacitance	C_{in}	f = 1MHz		1.6		pF
Common Mode Input Capacitance				1.12		pF
Transient Response						
Positive Slew Rate	SR	V_{OUT} = 1V to 4V, R_L = 10kΩ		0.2		V/µs
Negative Slew Rate				0.1		V/µs
Rise Time, t_r 10% to 90%	t_r, t_f, Small Signal	A_V = +1, V_{OUT} = 0.1V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		1.1		µs
Fall Time, t_f 10% to 90%				1.1		µs
Rise Time, t_r 10% to 90%	t_r, t_f Large Signal	A_V = +1, V_{OUT} = 2V_{P-P}, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		20		µs
Fall Time, t_f 10% to 90%				30		µs
Settling Time to 0.1%, 2V_{P-P} Step	t_s	A_V = +1, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF		35		µs
Output Overload Recovery Time, Recovery to 90% of Output Saturation	$t_{recover}$	A_V = +2, R_F = 10kΩ, R_L = Open, C_L = 3.7pF		10.5		µs

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

3. Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified.

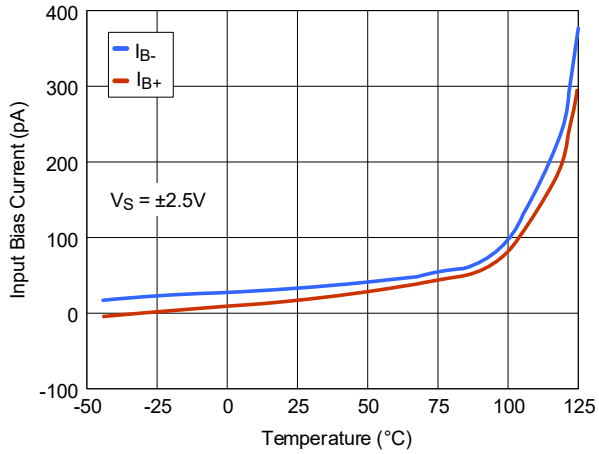


Figure 3. I_{B+}, I_{B-} vs Temperature: V_S = ±2.5V

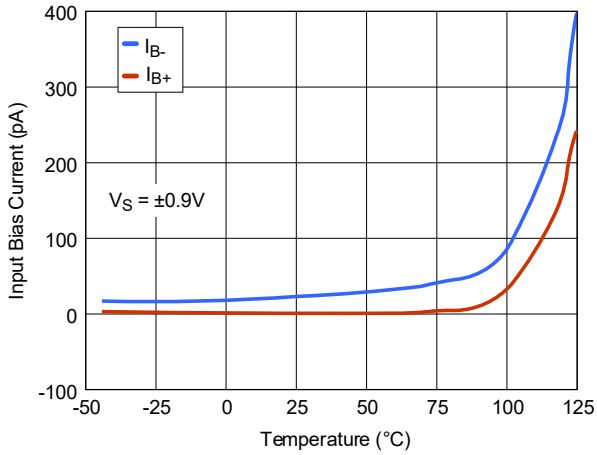


Figure 4. I_{B+}, I_{B-} vs Temperature: V_S = ±0.9V

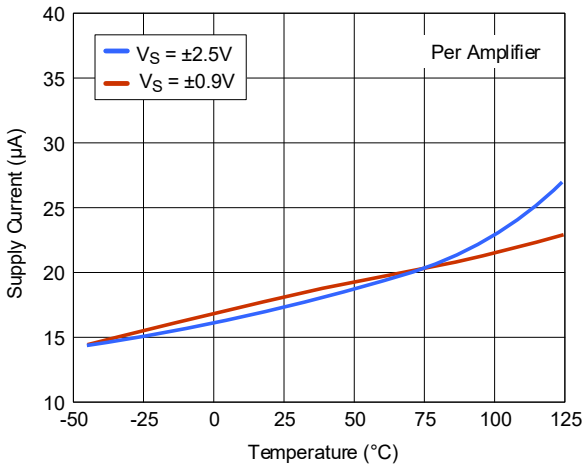


Figure 5. Supply Current vs Temperature

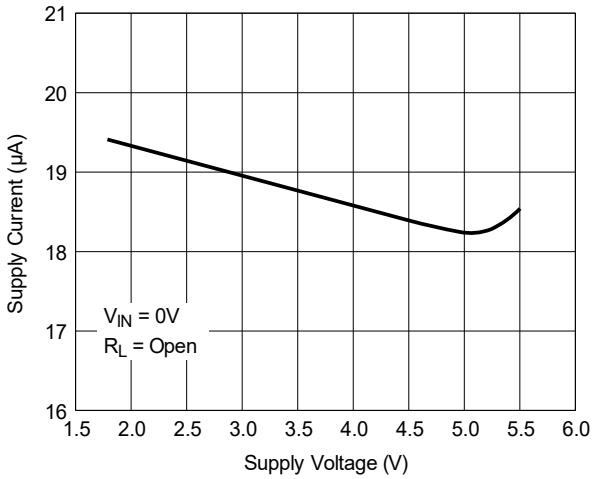


Figure 6. Supply Current vs Supply Voltage

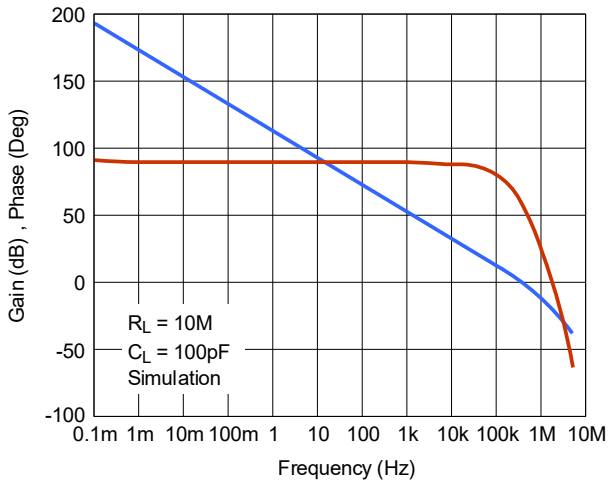


Figure 7. Open-Loop Gain and Phase Response

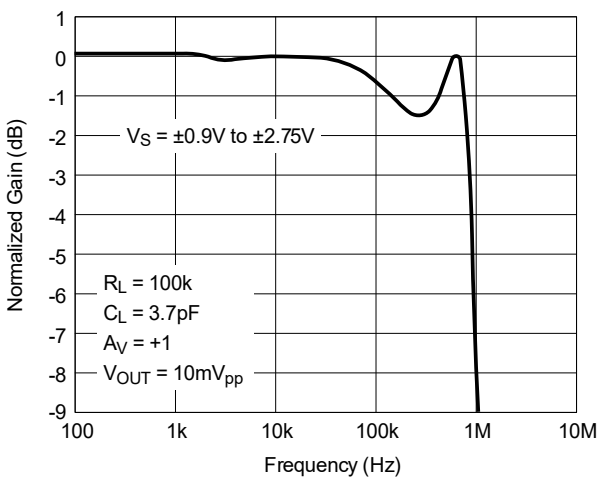


Figure 8. Gain Response vs Supply Voltage

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Cont.)

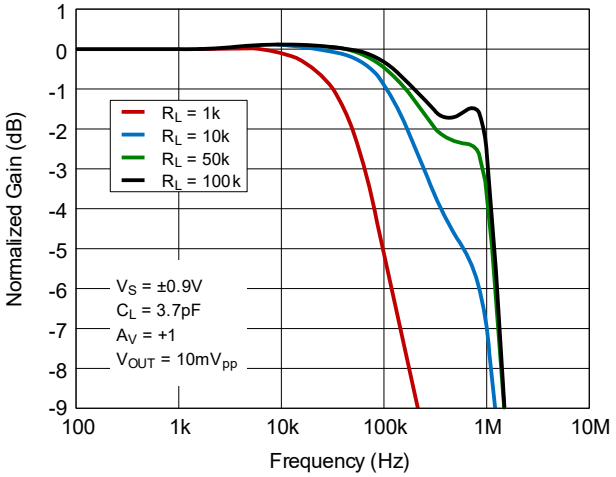


Figure 9. Gain Response vs Load Resistance, V_S = ±0.9V

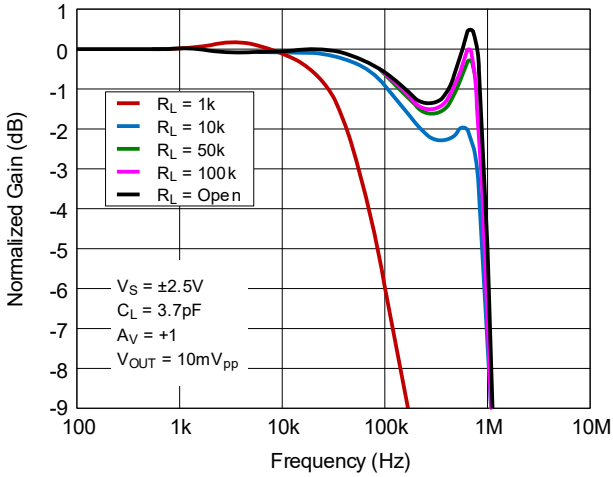


Figure 10. Gain Response vs Load Resistance, V_S = ±2.5V

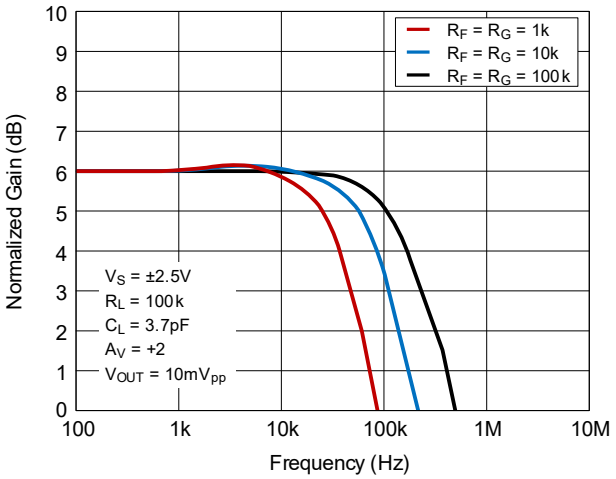


Figure 11. Gain Response vs Feedback Resistor Values

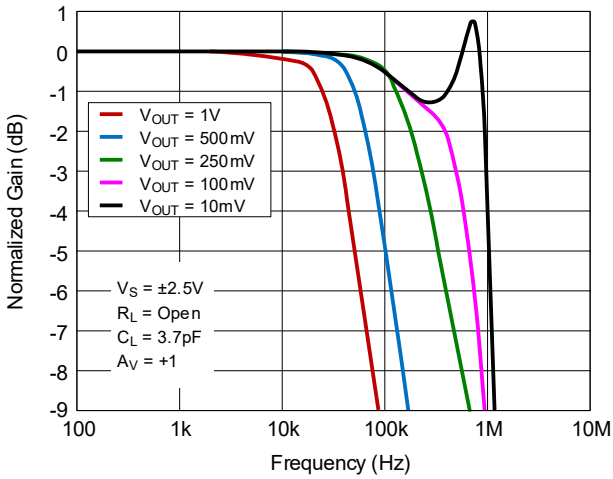


Figure 12. Gain Response vs Output Voltage

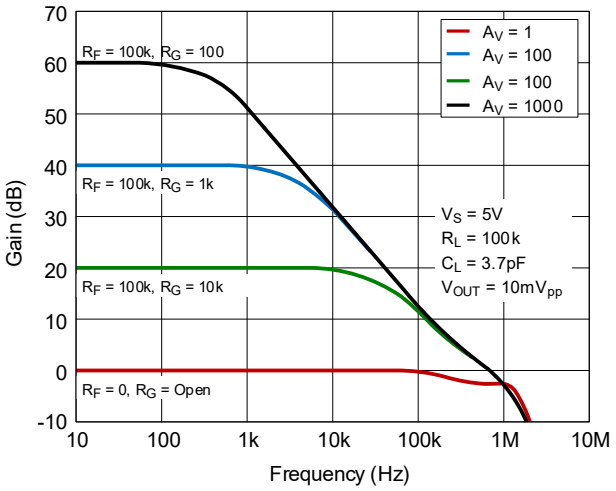


Figure 13. Closed Loop Gains vs Frequency

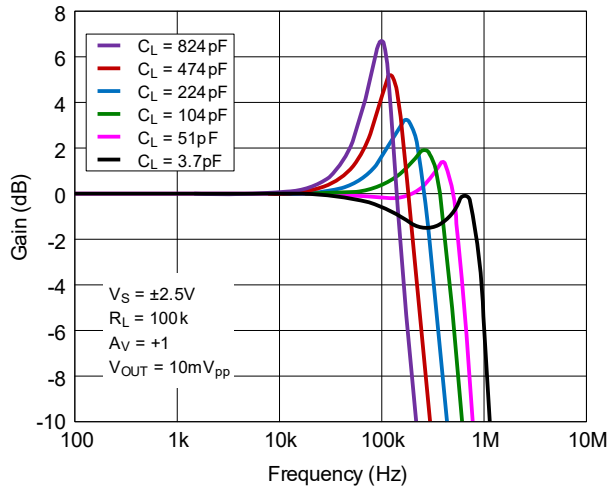


Figure 14. Gain Response vs Load Capacitance

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Cont.)

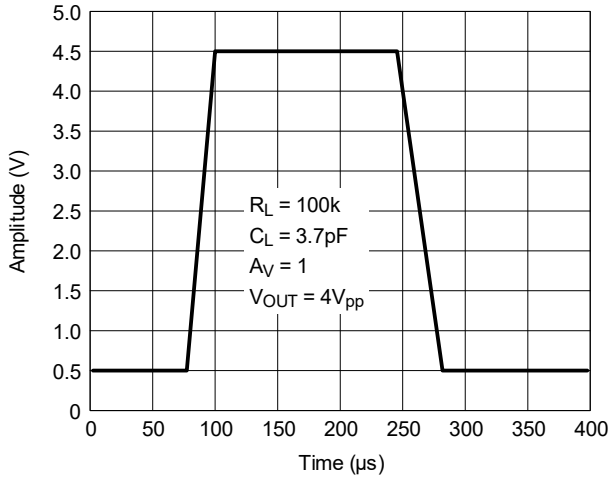


Figure 15. Large Signal Step Response (4V)

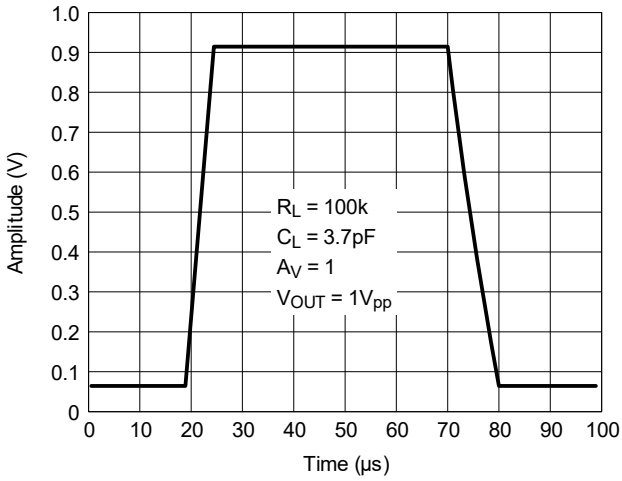


Figure 16. Large Signal Step Response (1V)

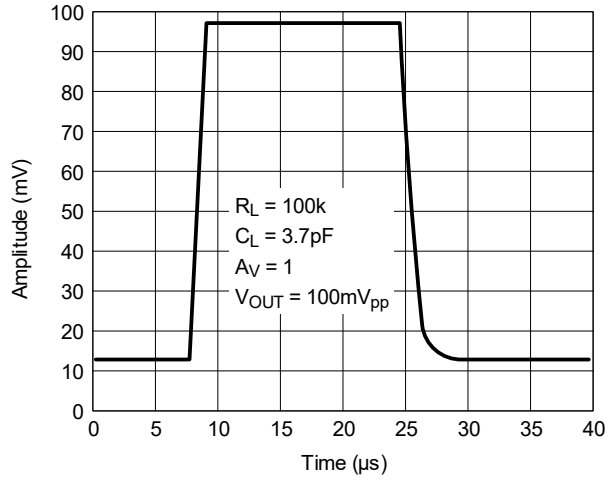


Figure 17. Small Signal Step Response (100mV)

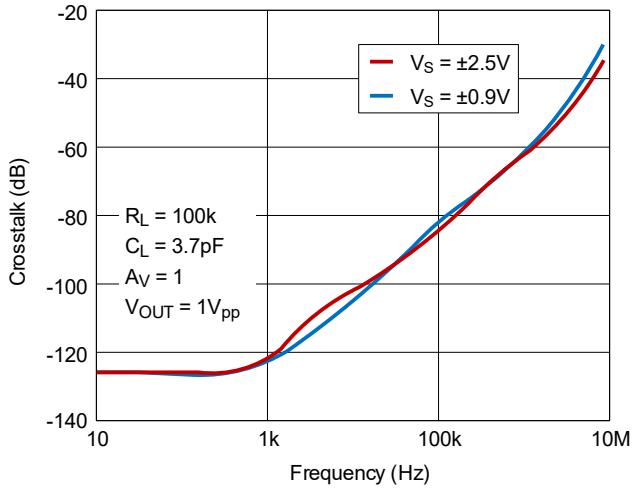


Figure 18. Crosstalk vs Frequency

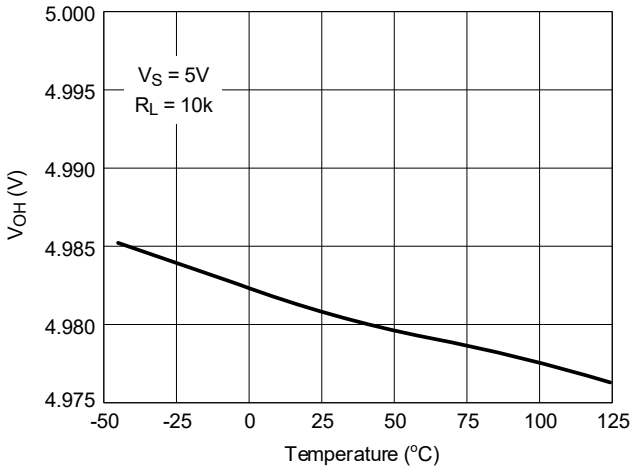


Figure 19. V_{OH} vs Temperature

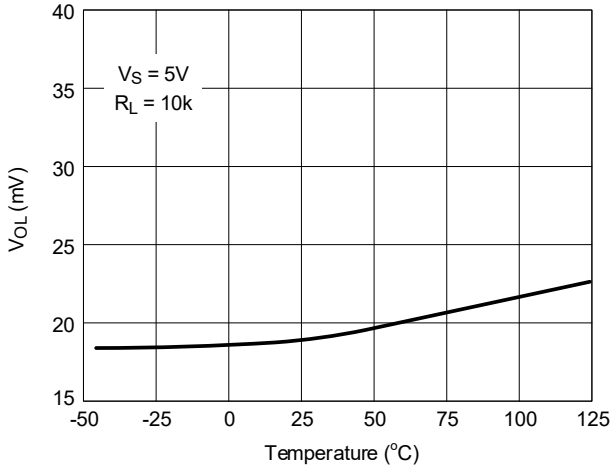


Figure 20. V_{OL} vs Temperature

4. Applications Information

4.1 Functional Description

The ISL28130, ISL28230, and ISL28430 are low offset and low drift operational amplifiers with a very high open-loop gain (150dB) and rail-to-rail input/output. They are designed to operate on a single supply range of 1.8V to 5.5V or a dual supply range of ±0.9V to ±2.75V while consuming only 20µA of supply current per channel. The ISL28130, ISL28230, and ISL28430 have a 400kHz gain-bandwidth.

The high open-loop gain, low offset voltage, high bandwidth, and low 1/f noise make the ISL28130, ISL28230, and ISL28430 ideal for precision applications.

4.2 Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 15mA current limit and the capability to swing to within 50mV of either rail while driving a 10kΩ load.

4.3 IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications in which either input is expected to exceed the rails by 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 21).

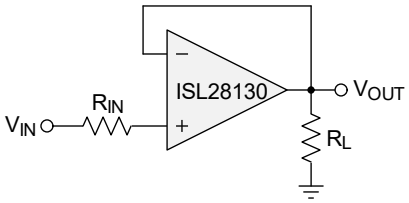


Figure 21. Input Current Limiting

4.4 Layout Guidelines for High Impedance Inputs

To achieve maximum performance from the high input impedance and low offset voltage of the ISL28130, ISL28230, and ISL28430 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board.

4.5 High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 22 implements a single-stage DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low VOS amplifier with high open loop gain. High gain DC amplifiers operating from low voltage supplies are not practical using typical low offset precision op amps. For example, consider a typical precision amplifier in a gain of 10kV/V. A low offset op amp with ±100µV V_{OS} and 0.5µV/°C offset drift yields a DC error of >1V, with an additional 5mV/°C of temperature-dependent error. This amount of error makes it difficult to resolve DC input voltage changes in the mV range.

The ±40µV max V_{OS} and 150nV/°C temperature drift of the ISL28130, ISL28230, and ISL28430 produce a temperature-stable maximum DC output error of only ±400mV, with a maximum output temperature drift of

1.5mV/°C. The additional benefit of a very low 1/f noise corner frequency and some feedback filtering allows DC voltages and voltage fluctuations well below 10µV to be easily detected with a simple, single-stage amplifier.

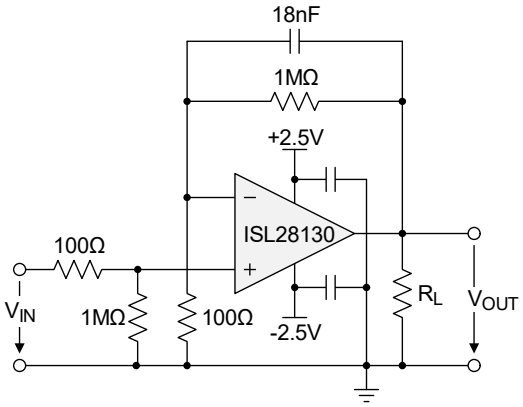
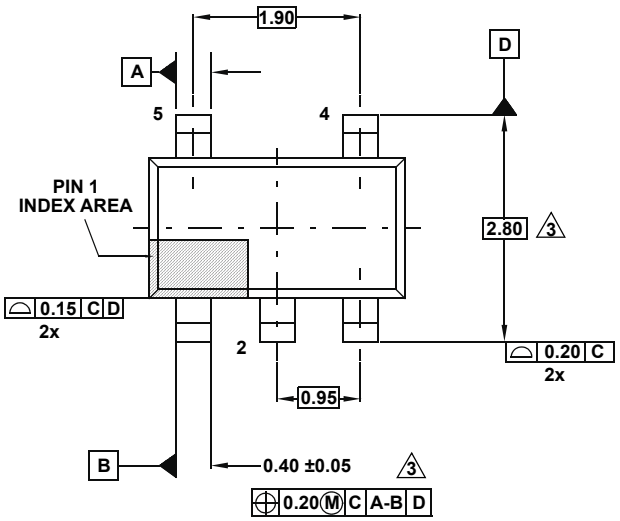


Figure 22. High Gain, Precision DC-Coupled Amplifier

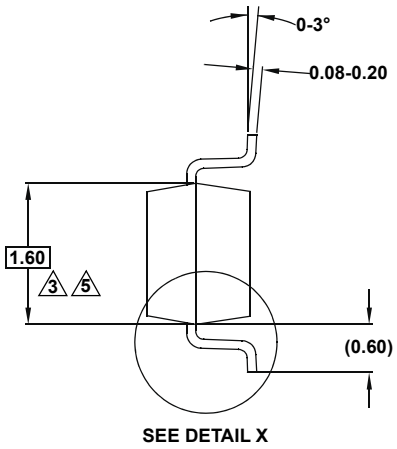
5. Package Outline Drawings

For the most recent package outline drawing, see P5.064A.

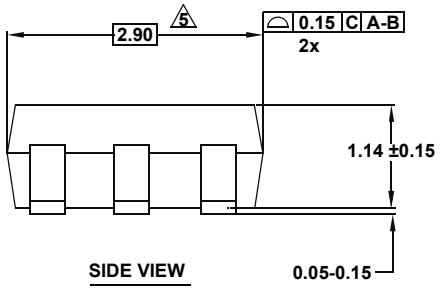
P5.064A
5 Lead Small Outline Transistor Plastic Package
Rev 0, 2/10



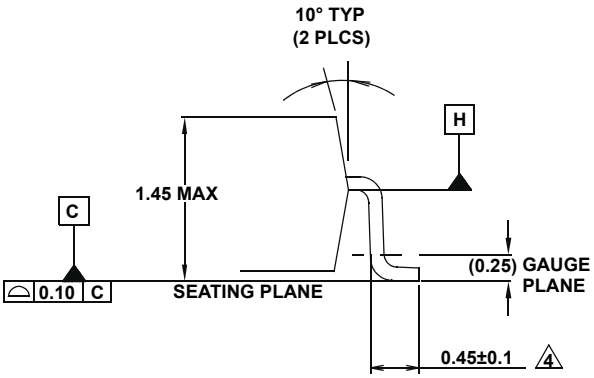
TOP VIEW



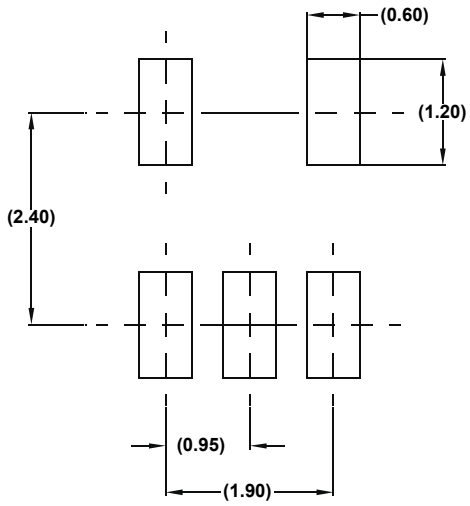
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

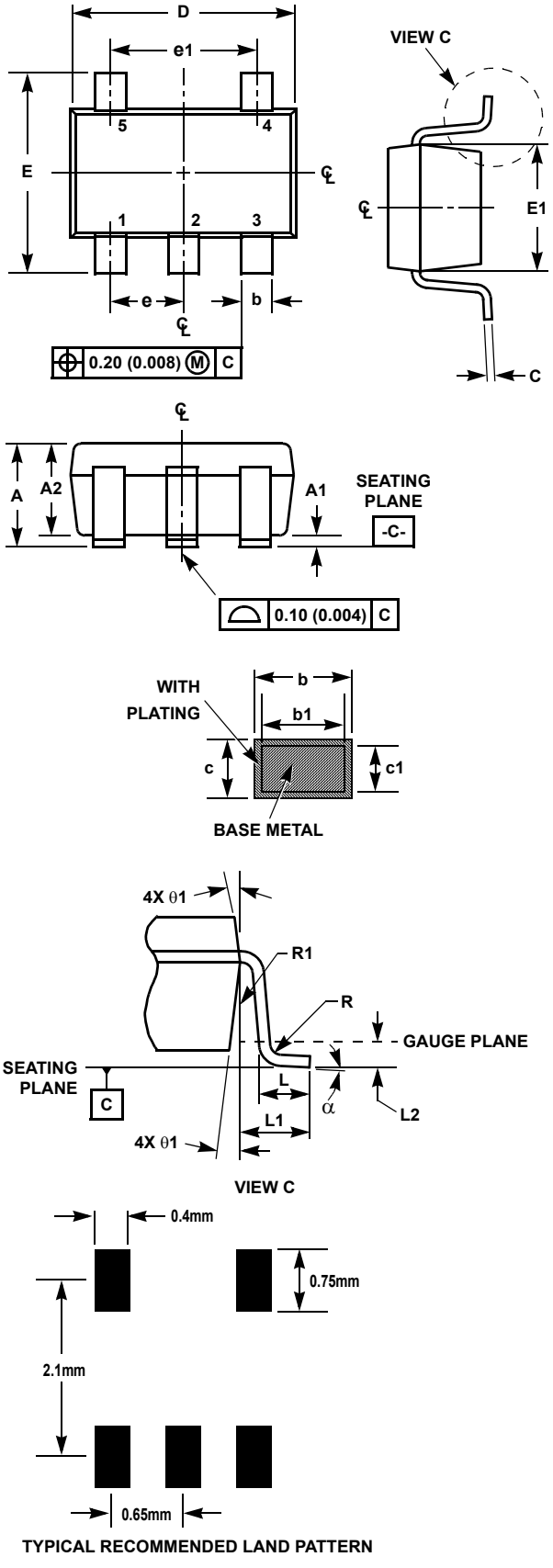
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

For the most recent package outline drawing, see P5.049.

P5.049

5 Lead Small Outline Transistor Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0°	8°	0°	8°	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

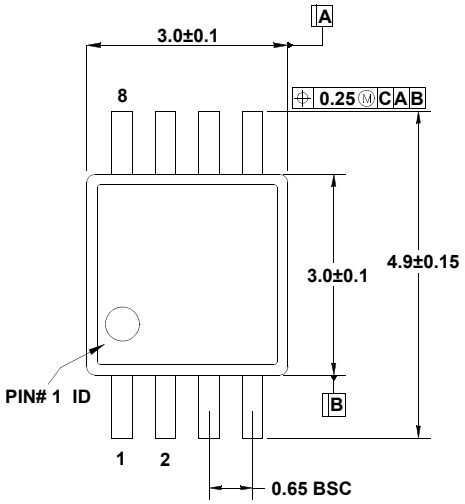
Rev. 3 7/07

NOTES:

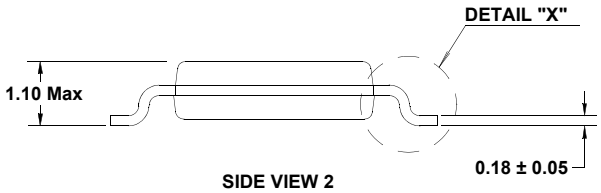
1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

For the most recent package outline drawing, see M8.118A.

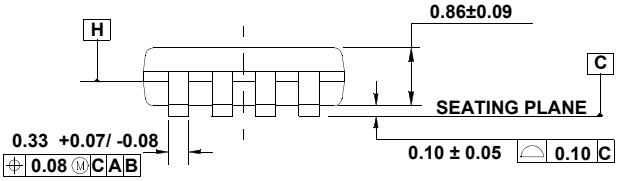
M8.118A
8 Lead Mini Small Outline Plastic Package (MSOP)
Rev 0, 9/09



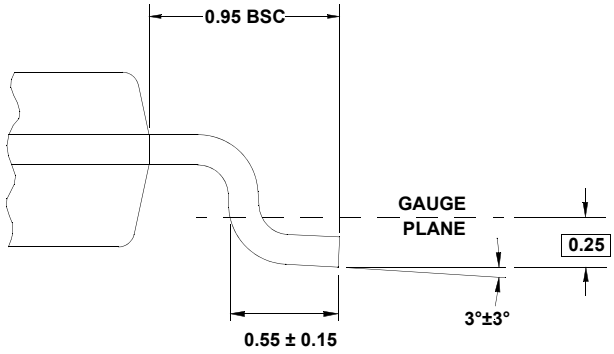
TOP VIEW



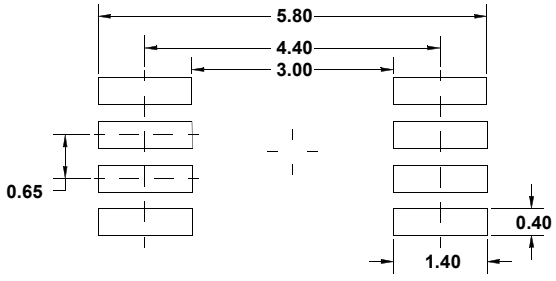
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



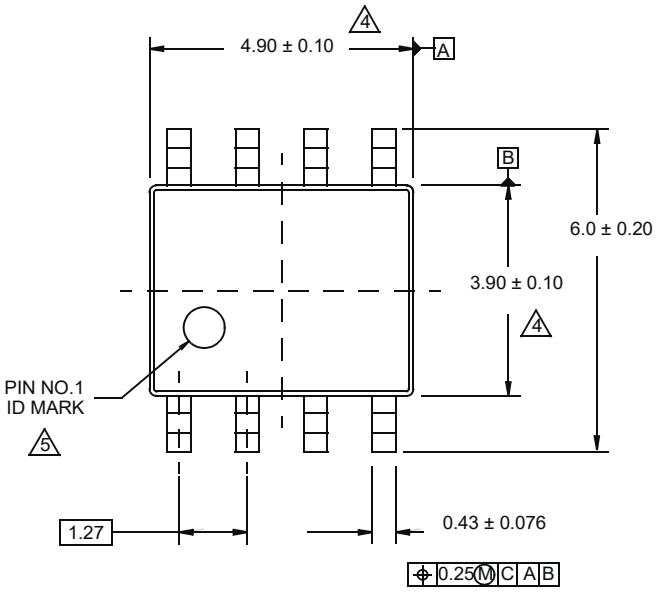
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

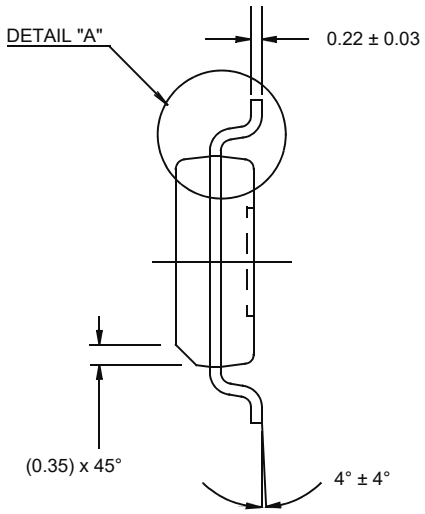
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

For the most recent package outline drawing, see M8.15E.

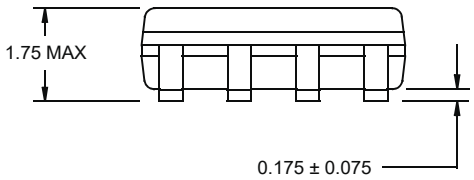
M8.15E
8 Lead Narrow Body Small Outline Plastic Package
Rev 0, 08/09



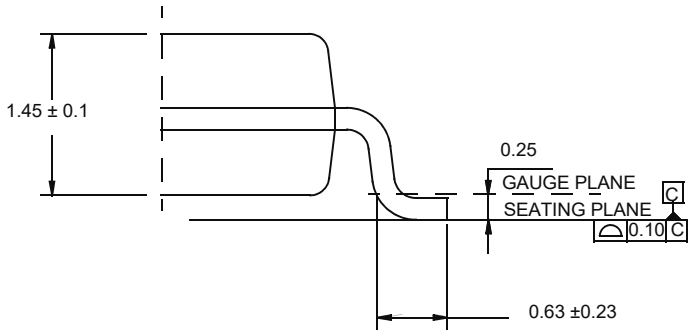
TOP VIEW



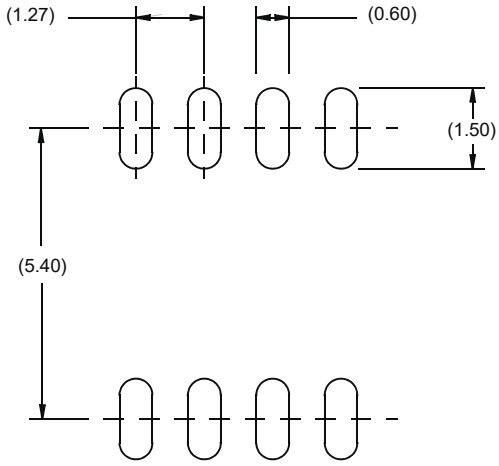
SIDE VIEW "B"



SIDE VIEW "A



DETAIL "A"



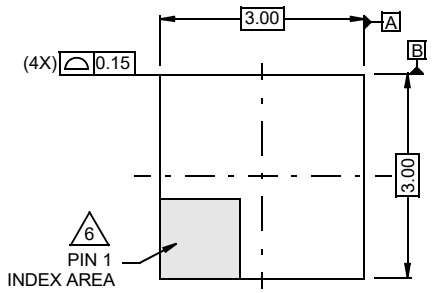
TYPICAL RECOMMENDED LAND PATTERN

NOTES:

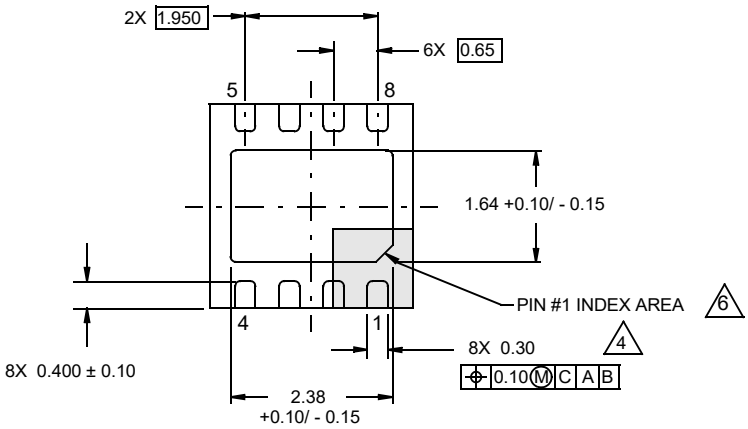
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

For the most recent package outline drawing, see L8.3x3J.

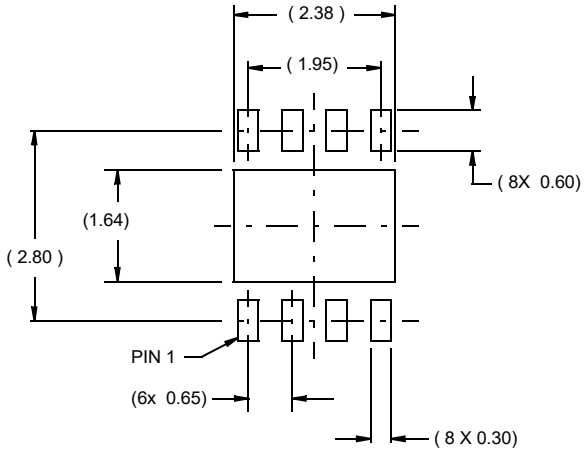
L8.3x3J
8 Lead Dual Flat No-Lead Plastic Package
Rev 1 3/15



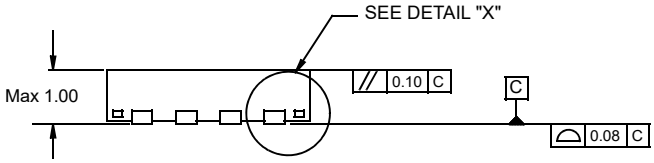
TOP VIEW



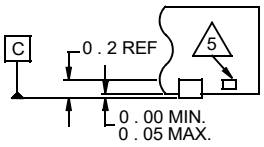
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



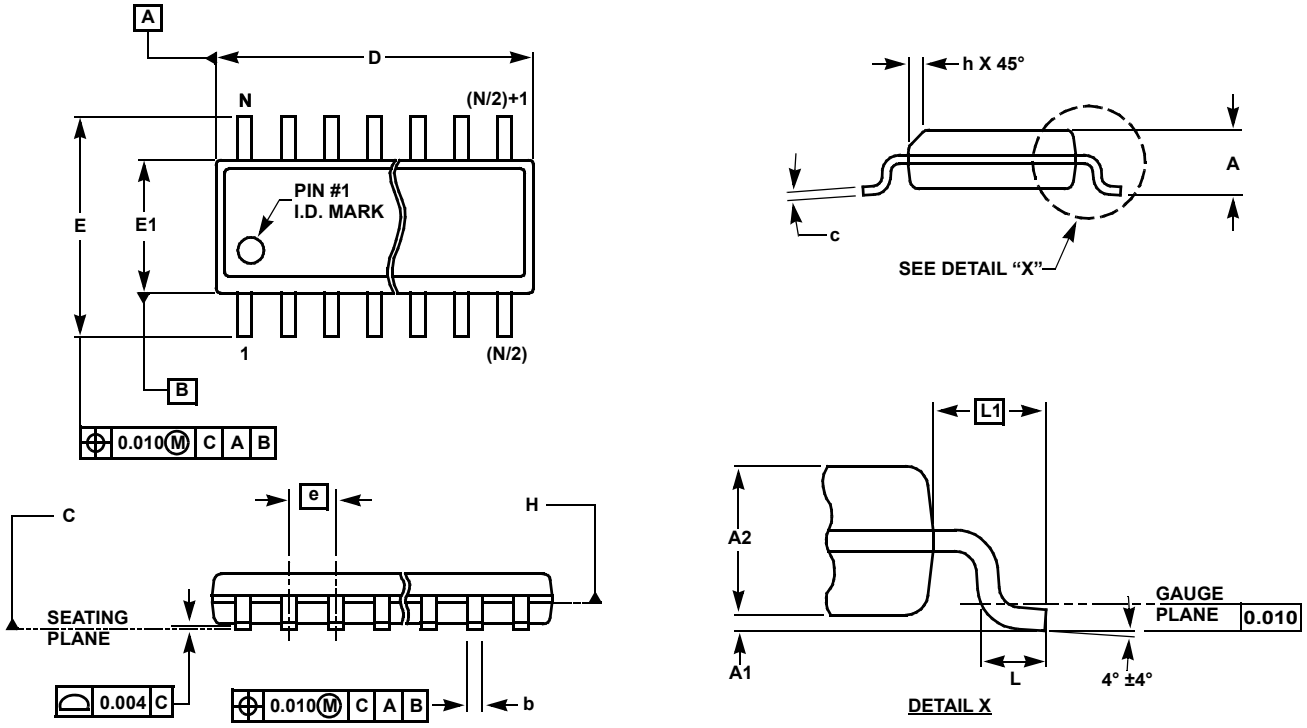
DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

For the most recent package outline drawing, see MDP0027.

MDP0027
Small Outline Package Family (SO)
Rev. M 2/07



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

Symbol	Inches							Tolerance	Notes
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

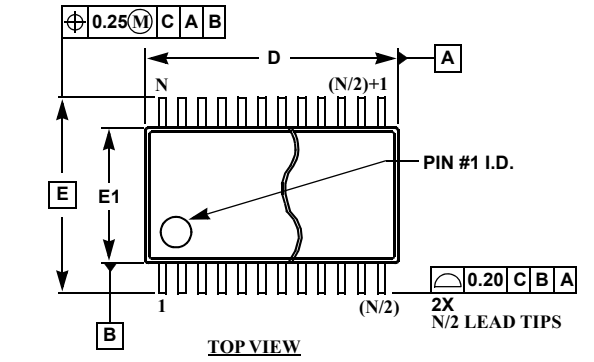
Rev. M 2/07

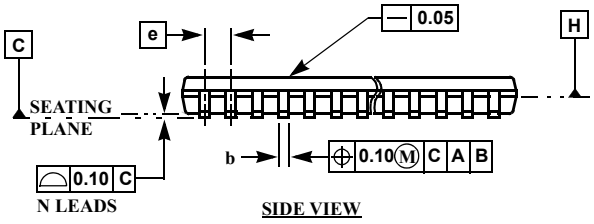
NOTES:

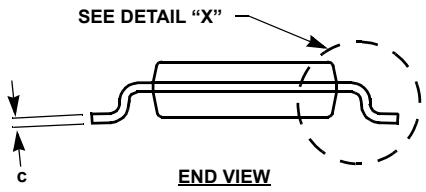
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

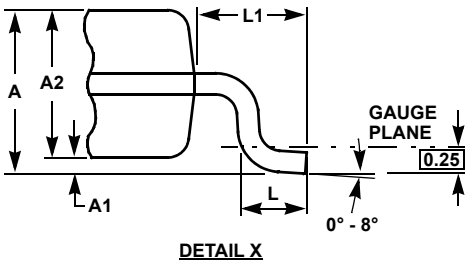
For the most recent package outline drawing, see MDP0044.

MDP0044
Thin Shrink Small Outline Package Family









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

5. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
6. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
7. Dimensions "D" and "E1" are measured at dAtum Plane H.
8. Dimensioning and tolerancing per ASME Y14.5M-1994.

6. Ordering Information

Part Number[1][2]	Part Marking	Temp. Grade	Package Description (RoHS Compliant)	PKG. DWG. #	Carrier Type[3]	Temp. Range
ISL28130CEZ-T7	BLA[4]	Commercial	5 Ld SC-70	P5.049	Reel, 3k	0 to +70°C
ISL28130CEZ-T7A					Reel, 250	
ISL28130CHZ-T7	BDPA[4]		5 Ld SOT-23	P5.064A	Reel, 3k	
ISL28130CHZ-T7A					Reel, 250	
ISL28130FEZ-T7	BNA [4]	Full	5 Ld SC-70	P5.049	Reel, 3k	-40 to +125°C
ISL28130FEZ-T7A					Reel, 250	
ISL28130FHZ-T7	BEFA[4]		5 Ld SOT-23	P5.064A	Reel, 3k	
ISL28130FHZ-T7A					Reel, 250	
ISL28230CBZ	28230 CBZ	Commercial	8 Ld SOIC	M8.15E	Tube	0 to +70°C
ISL28230CBZ-T7					Reel, 2k	
ISL28230CBZ-T7A					Reel, 250	
ISL28230CUZ	8230Z		8 Ld MSOP	M8.118A	Tube	
ISL28230CUZ-T7					Reel, 3k	
ISL28230CUZ-T7A					Reel, 250	
ISL28230CRZ	230Z		8 Ld 3mmx3mm DFN	L8.3x3J	Tube	
ISL28230CRZ-T7					Reel, 2k	
ISL28230CRZ-T13					Reel, 2.5k	
ISL28230CRZ-T7A					Reel, 250	
ISL28230FBZ	28230 FBZ	Full	8 Ld SOIC	M8.15E	Tube	-40 to +125°C
ISL28230FBZ-T13					Reel, 2.5k	
ISL28230FBZ-T7					Reel, 2k	
ISL28230FBZ-T7A					Reel, 250	
ISL28230FRZ	230F		8 Ld 3mmx3mm DFN	L8.3x3J	Tube	
ISL28230FRZ-T13					Reel, 6k	
ISL28230FRZ-T7					Reel, 2k	
ISL28230FRZ-T7A					Reel, 250	
ISL28230FUZ	8230F		8 Ld MSOP	M8.118A	Tube	
ISL28230FUZ-T7					Reel, 2k	
ISL28230FUZ-T7A					Reel, 250	
ISL28430CBZ	28430 CBZ	Commercial	14 Ld SOIC	MDP0027	Tube	0 to +70°C
ISL28430CBZ-T7					Reel, 2k	
ISL28430CBZ-T7A					Reel, 250	
ISL28430CVZ	28430 CVZ		14 Ld TSSOP	MDP0044	Tube	
ISL28430CVZ-T13					Reel, 2.5k	
ISL28430CVZ-T7A					Reel, 250	

Part Number[1][2]	Part Marking	Temp. Grade	Package Description (RoHS Compliant)	PKG. DWG. #	Carrier Type[3]	Temp. Range
ISL28430FBZ	28430 FBZ	Full	14 Ld SOIC	MDP0027	Tube	-40 to +125°C
ISL28430FBZ-T13					Reel, 2.5k	
ISL28430FBZ-T7					Reel, 2k	
ISL28430FVZ	28430 FVZ		14 Ld TSSOP	MDP0044	Tube	
ISL28430FVZ-T13					Reel, 2.5k	
ISL28430FVZ-T7					Reel, 2k	
ISL28430FVZ-T7A					Reel, 250	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL28130, ISL28230, ISL28430 device information. For more information about MSL, see TB363.
3. See **TB347** for details about reel specifications.
4. The part marking is located on the bottom of the part.

7. Revision History

Revision	Date	Description
8.00	Oct 24, 2022	Applied New Template and flow. Updated Ordering information table. Removed About Intersil section. Updated all Figures. Updated POD L8.3x3J to the latest revision, changes are as follows: -Updated Tiebar Note.
7.00	Feb 13, 2014	Ordering information table: Added part number ISL28230FRZ - Absolute Maximum Ratings section: changed Max Voltage VOUT to GND (10s): from ±3.0V to: (V- - 0.5V) to (V+ + 0.5V)V..
6.00	Nov 22, 2013	Removed “Coming Soon” from ISL28430FBZ in “Ordering Information” table.
5.00	Nov 8, 2012	Removed “Coming Soon” from ISL28130FHZ-T7, ISL28130FEZ-T7, ISL28130CBZ, ISL28130FBZ, ISL28230FUZ, ISL28230FRZ, ISL28430FVZ, ISL28230FRZ, ISL28130CBZ and ISL28130FBZ in “Ordering Information” table.
4.00	Feb 10, 2012	Removed “Coming Soon” from ISL28230FBZ in “Ordering Information” table.
3.00	Jun 13, 2011	Changed minimum operating supply voltage from +1.65V to +1.8V throughout datasheet. Modified Electrical Specifications table for all specs related at +1.65V to +1.8V, and all other text references accordingly. On page 1, paragraph 2, last sentence: changed from “All devices operate over the temperature range of -40°C to +125°C.” to “Commercial temp range devices operate over the temperature range of 0°C to 70°C. Full temp range devices operate over the temperature range of -40°C to 125°C.” Updated Ordering Information table: added “Coming Soon” to all devices with -40°C to 125°C temp range and to ISL28130CBZ at 0°C to +70°C temp range.

Revision	Date	Description
2.00	Mar 1, 2011	-Ordering Information Table: Removed all 'Coming Soon' under part numbers (except for ISL28130FBZ and ISL28230FRZ), added part markings for all 125°C grade parts. Added new data column called 'TEMPERATURE GRADE' to distinguish between 'Commercial' and 'Full' temp grades. - Electrical Specifications Table: added new text to common conditions: “Boldface limits apply over the entire operating temperature range”. This note allows bold face limits to apply both to commercial and full grade temp devices. - Added over temperature 0°C to 70°C spec for Vos in addition to -40°C to 125°C Vos spec. Original Vos spec of 46.8µV for -40°C to 125°C is a typo based on a TCVos of 150nV/C. -40°C to 125°C limit corrected as 55µV over temp.
1.00	December 7, 2010	Corrected Thermals for DFN package in “Tja from 125 to 53, “Tjc from 90 to 12” Removed Part Markings from Full temp grade parts and changed to TBD until availability is validated. -Updated front page text to add DFN packaging and extended temp range -40°C to +125°C -Removed previous Ib vs Temp plot and added new -40°C to +125°C Ib vs Temp plot on front page. -Updated ordering information table by adding a full temp range option to all parts and temp range column. Also added in DFN part to ordering table. All full temp parts are stamped Coming Soon. -Added DFN package to Pin Configurations table. -Added -40°C to +125°C temp range under Operating Conditions page 5. -Added the testing standards performance information to the ESD ratings in Abs Max Table -Added new Input Bias Current Ib spec of 700pA MIN/MAX in Electrical Spec table for -40°C to +125°C temp range -Revised Note in Electrical Spec table as: “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.” -Updated all curves in the datasheet with 0°C to +70°C temp range to -40°C to +125°C temp range. -Added DFN package L8.3x3J outline drawing to the end of datasheet. On page 7 changed “Supply Current, Per Amplifier” from a typical of 18µA to 20µA to comply with front page.
0.00	Aug 17, 2010	Initial release.

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