



Features

- 9A Peak Source/Sink Drive Current
- Wide Operating Voltage Range: 4.5V to 35V
- -40°C to +125°C Extended Operating Temperature Range
- Logic Input Withstands Negative Swing of up to 5V
- Matched Rise and Fall Times
- Low Propagation Delay Time
- Low, 10µA Supply Current
- Low Output Impedance

Applications

- Efficient Power MOSFET and IGBT Switching
- Switch Mode Power Supplies
- Motor Controls
- DC to DC Converters
- Class-D Switching Amplifiers
- Pulse Transformer Driver

Description

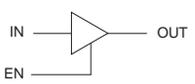
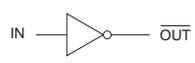
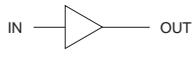
The IXDD609/IXDI609/IXDN609 high-speed gate drivers are especially well suited for driving the latest IXYS MOSFETs and IGBTs. The IXD_609 high-current output can source and sink 9A of peak current while producing voltage rise and fall times of less than 25ns. The input is CMOS compatible, and is virtually immune to latch up. Proprietary circuitry eliminates cross-conduction and current “shoot-through.” Low propagation delay and fast, matched rise and fall times make the IXD_609 family ideal for high-frequency and high-power applications.

The IXDD609 is configured as a non-inverting driver with an enable, the IXDN609 is configured as a non-inverting driver, and the IXDI609 is configured as an inverting driver.

The IXD_609 family is available in a standard 8-pin DIP (PI); an 8-pin SOIC (SIA); an 8-pin Power SOIC with an exposed metal back (SI); an 8-pin DFN (D2); a 5-pin TO-263 (YI); and a 5-pin TO-220 (CI).



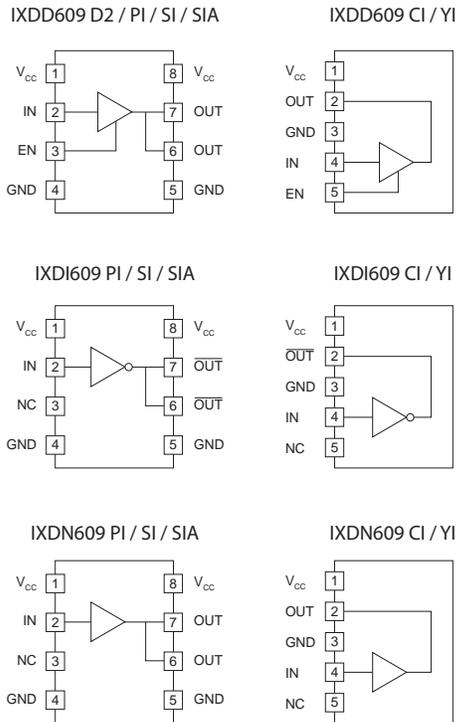
Ordering Information

| Part Number | Logic Configuration | Package Type | Packing Method | Quantity |
|--------------|---|--|----------------|----------|
| IXDD609D2TR |  | 8-Pin DFN | Tape & Reel | 2000 |
| IXDD609SI | | 8-Pin Power SOIC with Exposed Metal Back | Tube | 100 |
| IXDD609SITR | | 8-Pin Power SOIC with Exposed Metal Back | Tape & Reel | 2000 |
| IXDD609SIA | | 8-Pin SOIC | Tube | 100 |
| IXDD609SIATR | | 8-Pin SOIC | Tape & Reel | 2000 |
| IXDD609PI | | 8-Pin DIP | Tube | 50 |
| IXDD609CI | | 5-Pin TO-220 | Tube | 50 |
| IXDD609YI | | 5-Pin TO-263 | Tube | 50 |
| IXDI609SI |  | 8-Pin Power SOIC with Exposed Metal Back | Tube | 100 |
| IXDI609SITR | | 8-Pin Power SOIC with Exposed Metal Back | Tape & Reel | 2000 |
| IXDI609SIA | | 8-Pin SOIC | Tube | 100 |
| IXDI609SIATR | | 8-Pin SOIC | Tape & Reel | 2000 |
| IXDI609PI | | 8-Pin DIP | Tube | 50 |
| IXDI609CI | | 5-Pin TO-220 | Tube | 50 |
| IXDI609YI | 5-Pin TO-263 | Tube | 50 | |
| IXDN609SI |  | 8-Pin Power SOIC with Exposed Metal Back | Tube | 100 |
| IXDN609SITR | | 8-Pin Power SOIC with Exposed Metal Back | Tape & Reel | 2000 |
| IXDN609SIA | | 8-Pin SOIC | Tube | 100 |
| IXDN609SIATR | | 8-Pin SOIC | Tape & Reel | 2000 |
| IXDN609PI | | 8-Pin DIP | Tube | 50 |
| IXDN609CI | | 5-Pin TO-220 | Tube | 50 |
| IXDN609YI | | 5-Pin TO-263 | Tube | 50 |

| | |
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1 Specifications

1.1 Pin Configurations



1.2 Pin Definitions

| Pin Name | Description |
|-------------------------|---|
| IN | Logic Input |
| EN | Output Enable - Drive pin low to disable output, and force output to a high impedance state |
| OUT | Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT |
| $\overline{\text{OUT}}$ | Inverted Output - Sources or sinks current to turn-on or turn-off a discrete MOSFET or IGBT |
| V _{CC} | Supply Voltage - Provides power to the device |
| GND | Ground - Common ground reference for the device |
| NC | Not connected |

1.3 Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Maximum | Units |
|----------------------|-----------------------------------|---------|----------------------|-------|
| Supply Voltage | V _{CC} | -0.3 | 40 | V |
| Input Voltage | V _{IN} , V _{EN} | -5 | V _{CC} +0.3 | V |
| Output Current | I _{OUT} | - | ±9 | A |
| Junction Temperature | T _J | -55 | +150 | °C |
| Storage Temperature | T _{STG} | -65 | +150 | °C |

Unless stated otherwise, absolute maximum electrical ratings are at 25°C

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

| Parameter | Symbol | Range | Units |
|-----------------------------|-----------------|-------------|-------|
| Supply Voltage | V _{CC} | 4.5 to 35 | V |
| Operating Temperature Range | T _A | -40 to +125 | °C |

1.5 Electrical Characteristics: $T_A = 25^\circ\text{C}$

 Test Conditions: $4.5\text{V} \leq V_{CC} \leq 35\text{V}$ (unless otherwise noted).

| Parameter | Conditions | Symbol | Minimum | Typical | Maximum | Units |
|---|---|--------------|----------------|---------|-------------|---------------|
| Input Voltage, High | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IH} | 3.0 | - | - | V |
| Input Voltage, Low | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IL} | - | - | 0.8 | |
| Input Current | $0\text{V} \leq V_{IN} \leq V_{CC}$ | I_{IN} | - | - | ± 10 | μA |
| EN Input Voltage, High | IXDD609 only | V_{ENH} | $2/3V_{CC}$ | - | - | V |
| EN Input Voltage, Low | IXDD609 only | V_{ENL} | - | - | $1/3V_{CC}$ | |
| Output Voltage, High | - | V_{OH} | $V_{CC}-0.025$ | - | - | V |
| Output Voltage, Low | - | V_{OL} | - | - | 0.025 | |
| Output Resistance, High State | $V_{CC}=18\text{V}, I_{OUT}=100\text{mA}$ | R_{OH} | - | 0.6 | 1 | Ω |
| Output Resistance, Low State | $V_{CC}=18\text{V}, I_{OUT}=100\text{mA}$ | R_{OL} | - | 0.4 | 0.8 | |
| Output Current, Continuous | Limited by package power dissipation | I_{DC} | - | - | ± 2 | A |
| Rise Time | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_r | - | 22 | 35 | ns |
| Fall Time | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_f | - | 15 | 25 | |
| On-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_{ondly} | - | 40 | 60 | |
| Off-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_{offdly} | - | 42 | 60 | |
| Enable to Output-High Delay Time (IXDD609 Only) | $V_{CC}=18\text{V}$ | t_{ENOH} | - | 25 | 60 | |
| Disable to High Impedance State Delay Time (IXDD609 Only) | $V_{CC}=18\text{V}$ | t_{DOLD} | - | 35 | 60 | |
| Enable Pull-Up Resistor | - | R_{EN} | - | 200 | - | |
| Power Supply Current | $V_{CC}=18\text{V}, V_{IN}=3.5\text{V}$ | I_{CC} | - | 1 | 2 | mA |
| | $V_{CC}=18\text{V}, V_{IN}=0\text{V}$ | | - | <1 | 10 | |
| | $V_{CC}=18\text{V}, V_{IN}=V_{CC}$ | | - | <1 | 10 | |

1.6 Electrical Characteristics: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$

 Test Conditions: $4.5\text{V} \leq V_{CC} \leq 35\text{V}$ unless otherwise noted.

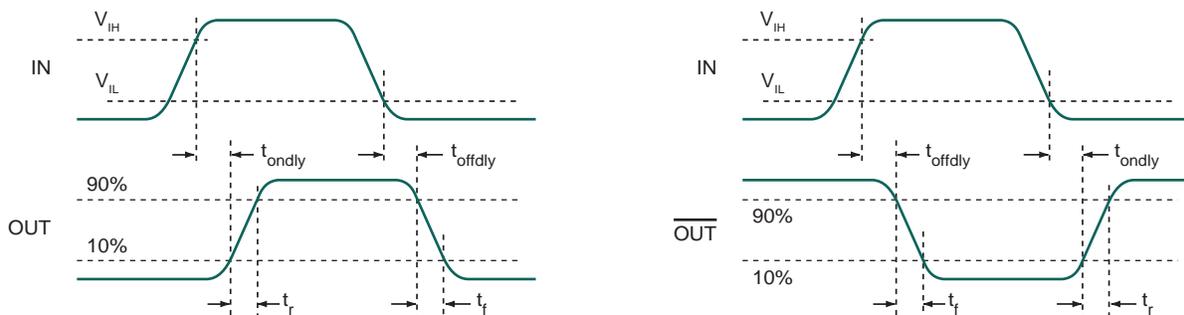
| Parameter | Conditions | Symbol | Minimum | Maximum | Units |
|--|---|--------------|----------------|----------|---------------|
| Input Voltage, High | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IH} | 3.3 | - | V |
| Input Voltage, Low | $4.5\text{V} \leq V_{CC} \leq 18\text{V}$ | V_{IL} | - | 0.65 | |
| Input Current | $0\text{V} \leq V_{IN} \leq V_{CC}$ | I_{IN} | - | ± 10 | μA |
| Output Voltage, High | - | V_{OH} | $V_{CC}-0.025$ | - | V |
| Output Voltage, Low | - | V_{OL} | - | 0.025 | |
| Output Resistance, High State | $V_{CC}=18\text{V}, I_{OUT}=100\text{mA}$ | R_{OH} | - | 2 | Ω |
| Output Resistance, Low State | $V_{CC}=18\text{V}, I_{OUT}=100\text{mA}$ | R_{OL} | - | 1.5 | |
| Output Current, Continuous | Limited by package power dissipation | I_{DC} | - | ± 1 | A |
| Rise Time | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_r | - | 40 | ns |
| Fall Time | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_f | - | 30 | |
| On-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_{ondly} | - | 75 | |
| Off-Time Propagation Delay | $V_{CC}=18\text{V}, C_{LOAD}=10\text{nF}$ | t_{offdly} | - | 75 | |
| Enable to Output-High Delay Time | IXDD609 only, $V_{CC}=18\text{V}$ | t_{ENOH} | - | 75 | |
| Disable to High Impedance State Delay Time | IXDD609 only, $V_{CC}=18\text{V}$ | t_{DOLD} | - | 75 | |
| Power Supply Current | $V_{CC}=18\text{V}, V_{IN}=3.5\text{V}$ | I_{CC} | - | 2.5 | |
| | $V_{CC}=18\text{V}, V_{IN}=0\text{V}$ | | - | 150 | |
| | $V_{CC}=18\text{V}, V_{IN}=V_{CC}$ | | - | 150 | μA |

1.7 Thermal Characteristics

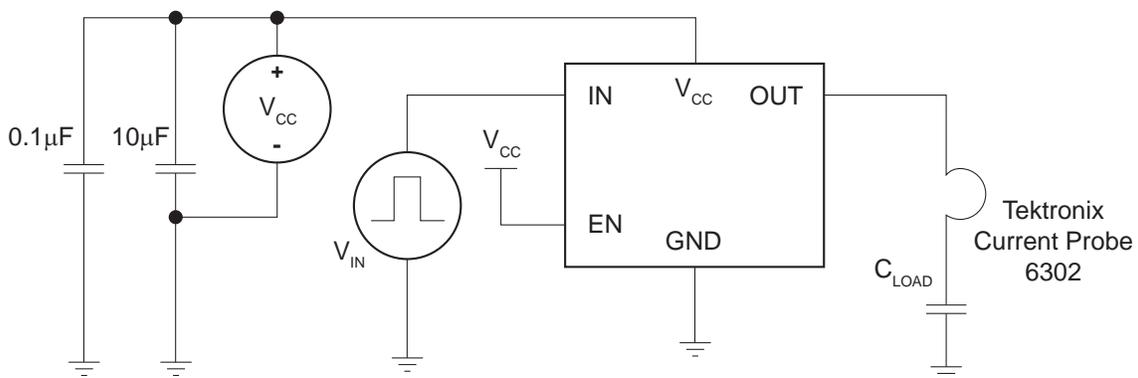
| Package | Parameter | Symbol | Rating | Units |
|-----------------------|--|---------------|--------|----------------------|
| D2 (8-Pin DFN) | Thermal Impedance, Junction-to-Ambient | θ_{JA} | 35 | $^{\circ}\text{C/W}$ |
| CI (5-Pin TO-220) | | | 36 | |
| PI (8-Pin DIP) | | | 125 | |
| SI (8-Pin Power SOIC) | | | 85 | |
| SIA (8-Pin SOIC) | | | 120 | |
| YI (5-Pin TO-263) | | | 46 | |
| CI (5-Pin TO-220) | Thermal Impedance, Junction-to-Case | θ_{JC} | 3 | $^{\circ}\text{C/W}$ |
| SI (8-Pin Power SOIC) | | | 10 | |
| YI (5-Pin TO-263) | | | 2 | |

2 IXD_609 Performance

2.1 Timing Diagrams

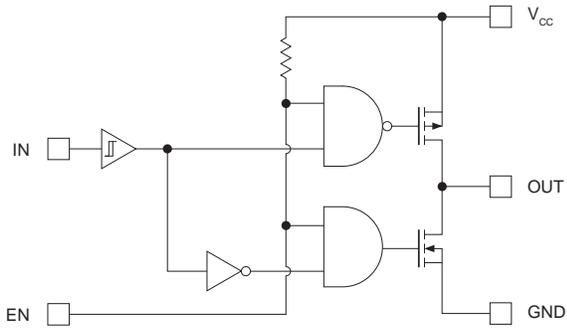


2.2 Characteristics Test Diagram



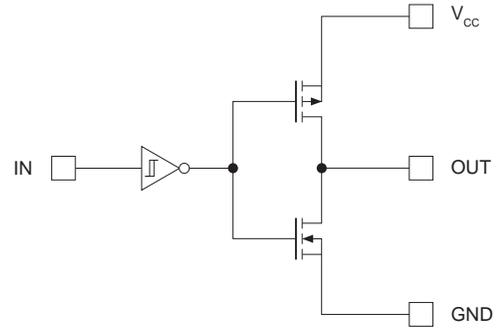
3 Block Diagrams & Truth Tables

3.1 IXDD609



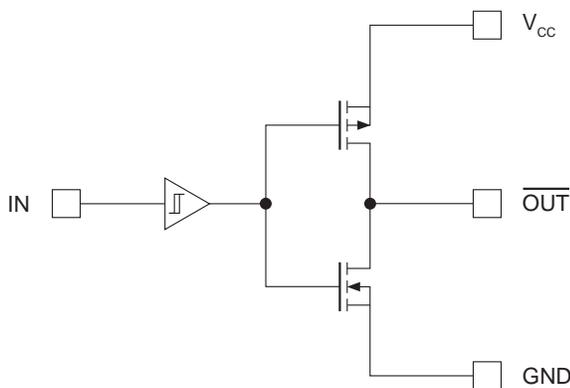
| IN | EN | OUT |
|----|-----------|-----|
| 0 | 1 or open | 0 |
| 1 | 1 or open | 1 |
| x | 0 | Z |

3.3 IXDN609



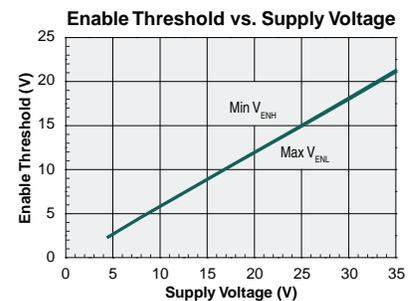
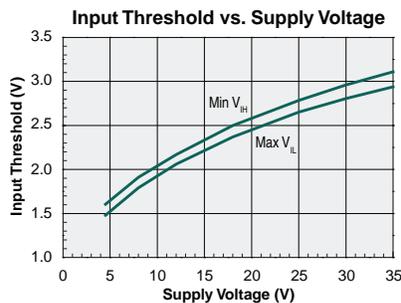
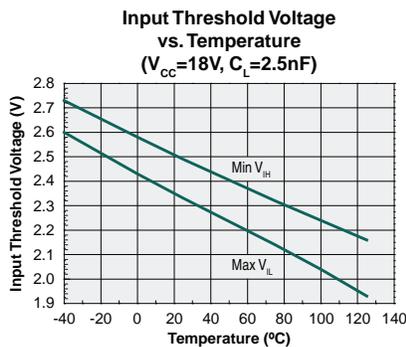
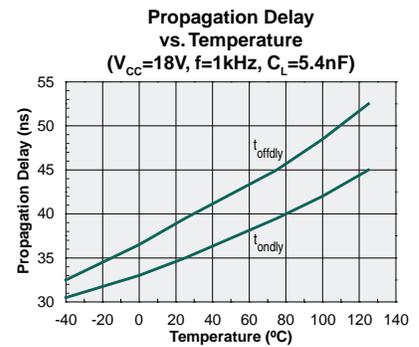
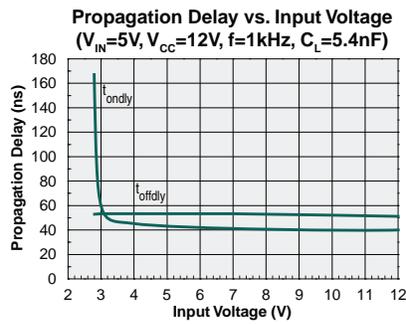
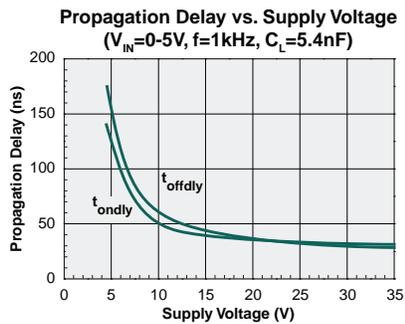
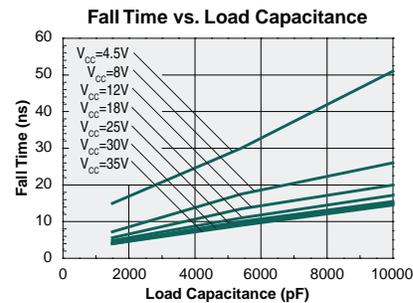
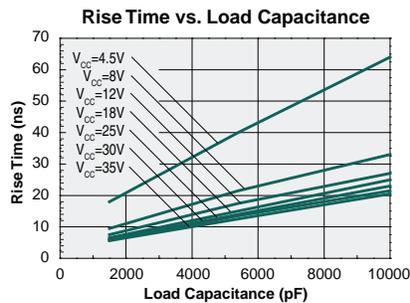
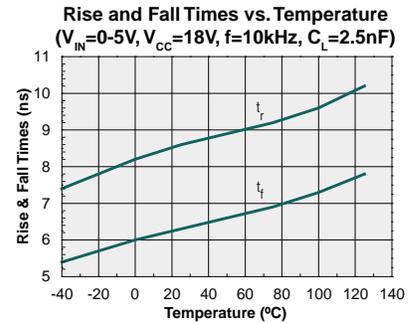
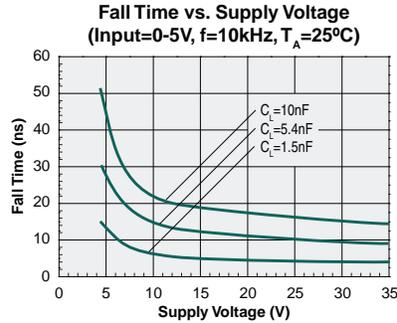
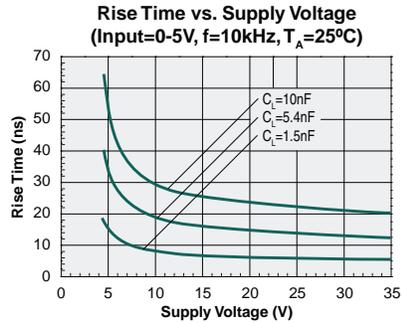
| IN | OUT |
|----|-----|
| 0 | 0 |
| 1 | 1 |

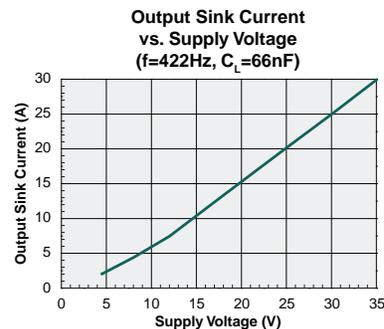
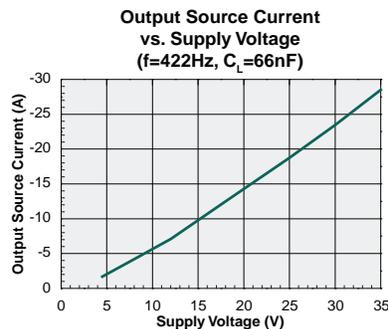
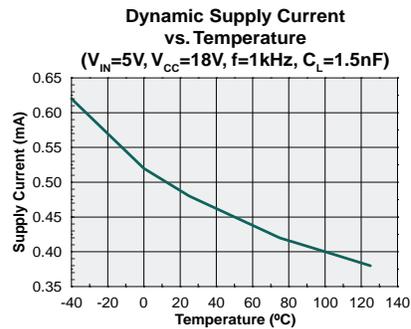
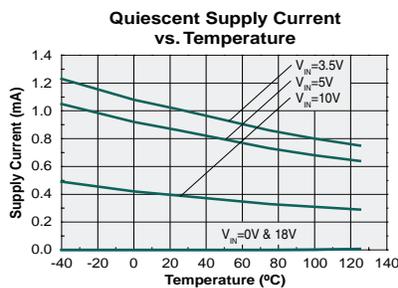
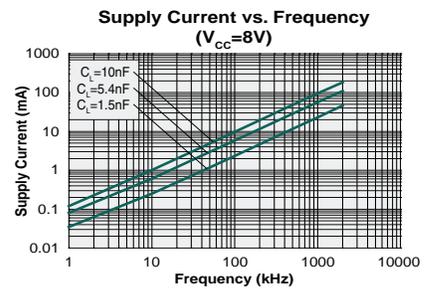
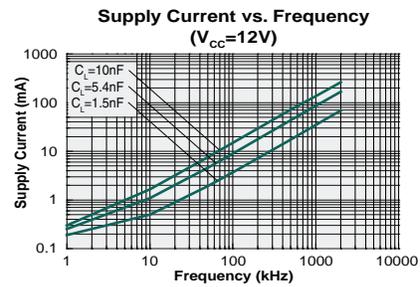
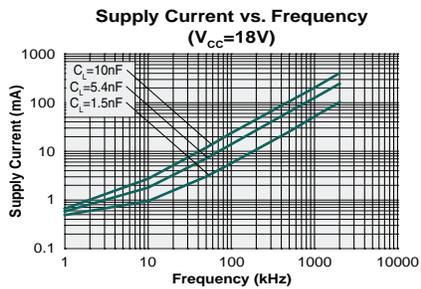
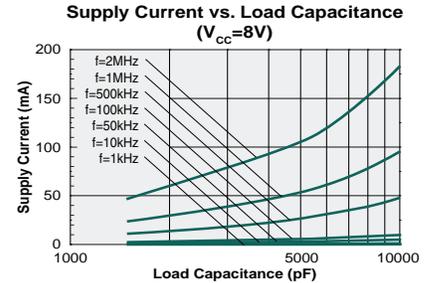
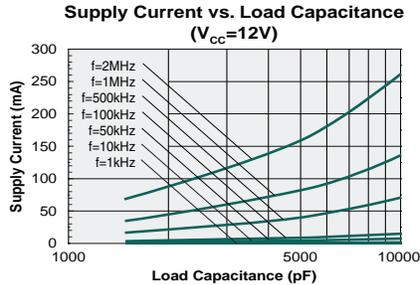
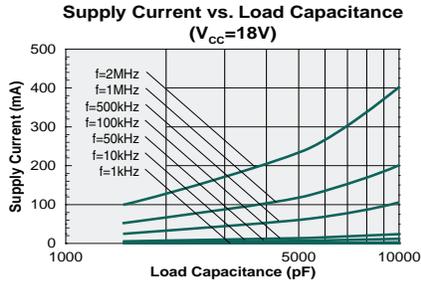
3.2 IXDI609

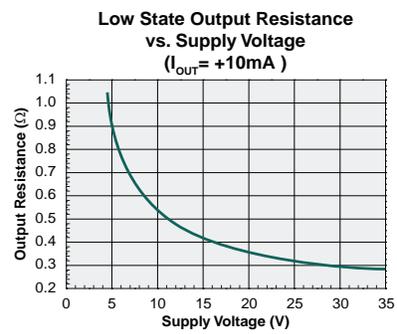
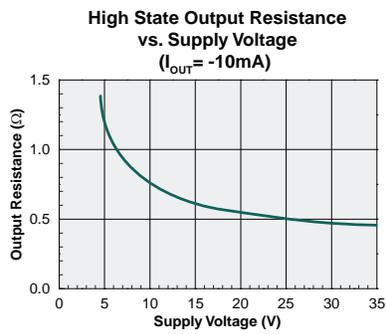
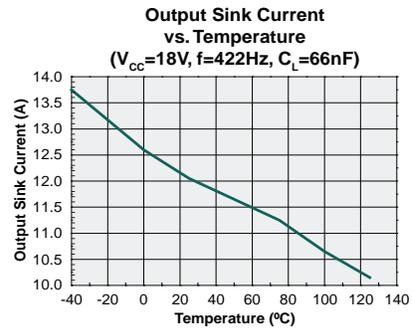
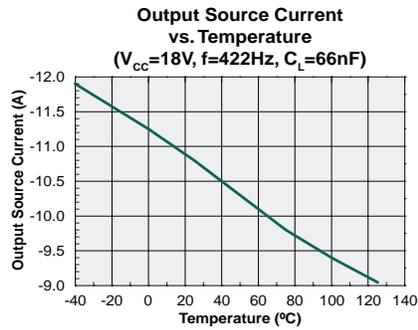


| IN | $\overline{\text{OUT}}$ |
|----|-------------------------|
| 0 | 1 |
| 1 | 0 |

4 Typical Performance Characteristics







5 Manufacturing Information

5.1 Moisture Sensitivity



All plastic encapsulated semiconductor packages are susceptible to moisture ingress. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation.

We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

| Device | Moisture Sensitivity Level (MSL) Classification |
|---------------------------------------|---|
| IXD_609 All Versions except IXD_609Y1 | MSL 1 |
| IXD_609Y1 | MSL 3 |

5.2 ESD Sensitivity



This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be ($T_C - 5$)°C or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

| Device | Classification Temperature (T_C) | Dwell Time (t_p) | Maximum Cycles |
|------------------------------------|--------------------------------------|----------------------|----------------|
| IXD_609CI | 245°C for 30 seconds | 30 seconds | 1 |
| IXD_609Y1 | 245°C for 30 seconds | 30 seconds | 3 |
| IXD_609PI | 250°C for 30 seconds | 30 seconds | 3 |
| IXD_609SI / IXD_609SIA / IXD_609D2 | 260°C for 30 seconds | 30 seconds | 3 |

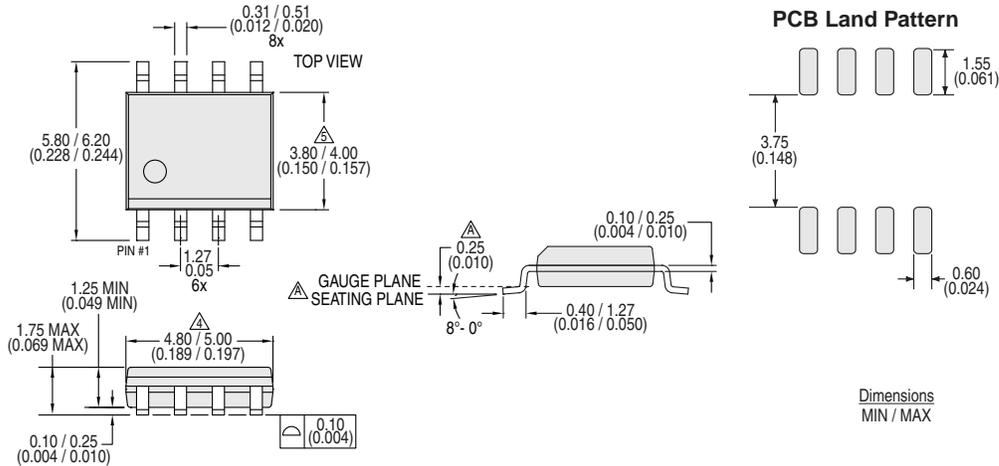
5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.



5.5 Mechanical Dimensions

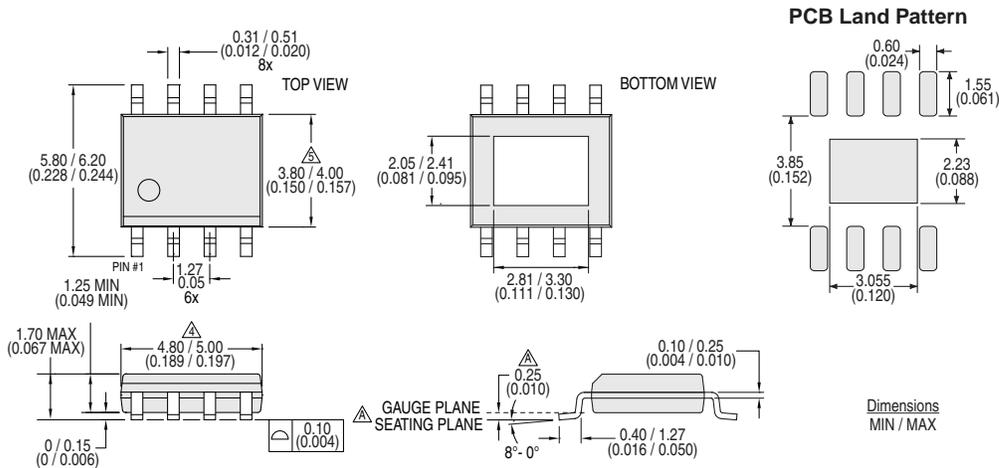
5.5.1 SIA (8-Pin SOIC)



Notes:

1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation AA, Rev. F.
- △ Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
- △ Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. Lead thickness includes plating.

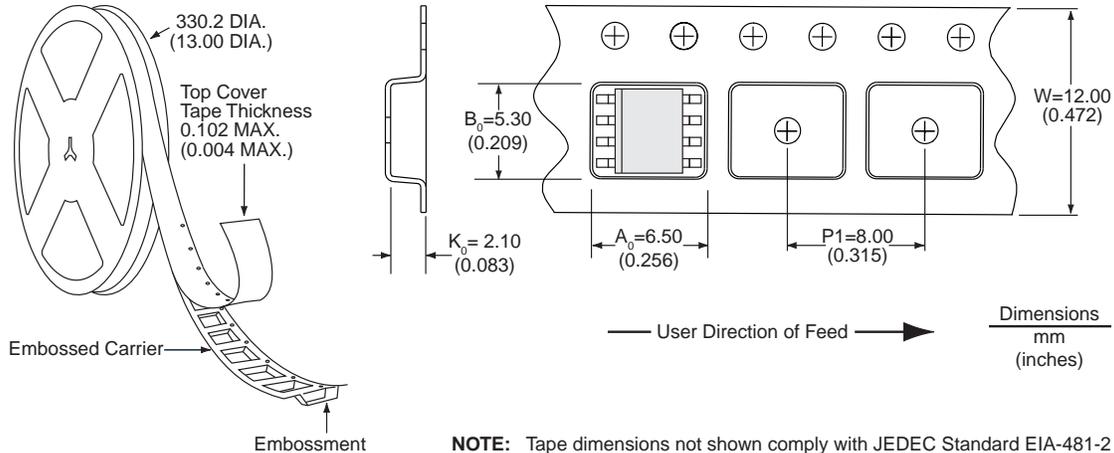
5.5.2 SI (8-Pin Power SOIC with Exposed Metal Back)



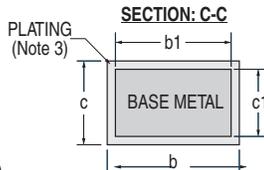
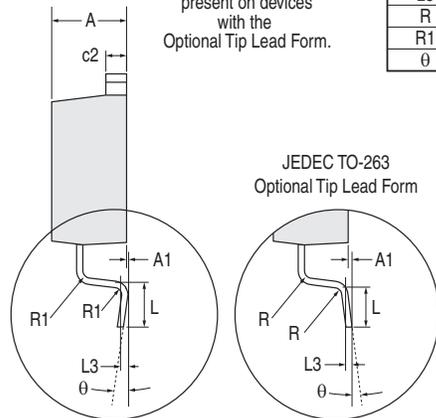
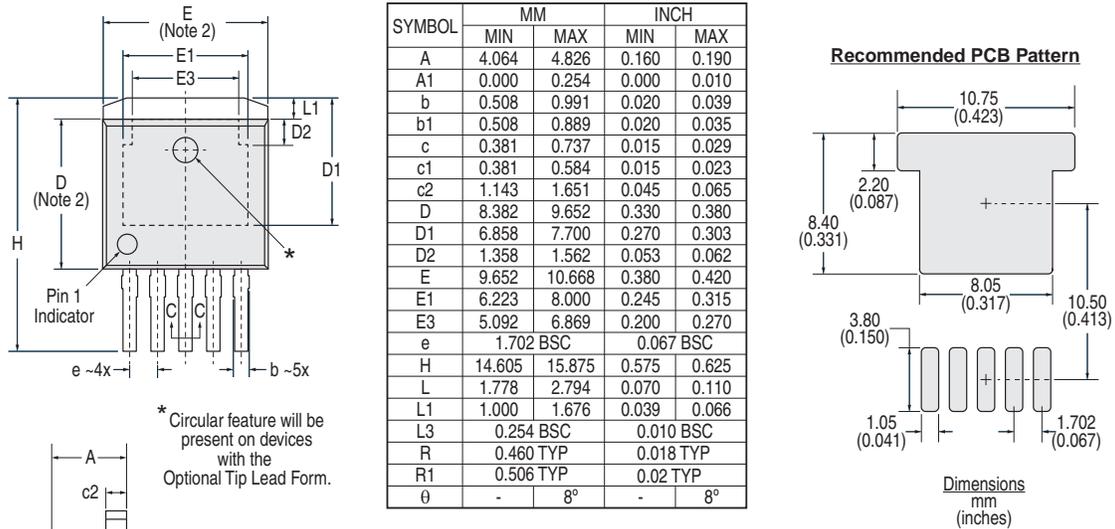
Notes:

1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. This package conforms to JEDEC Standard MS-012, variation BA, Rev. F.
- △ Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15mm per end.
- △ Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
6. The exposed metal pad on the back of the package should be connected to GND. It is not suitable for carrying current.
7. Lead thickness includes plating.

5.5.3 Tape & Reel Information for SI and SIA Packages

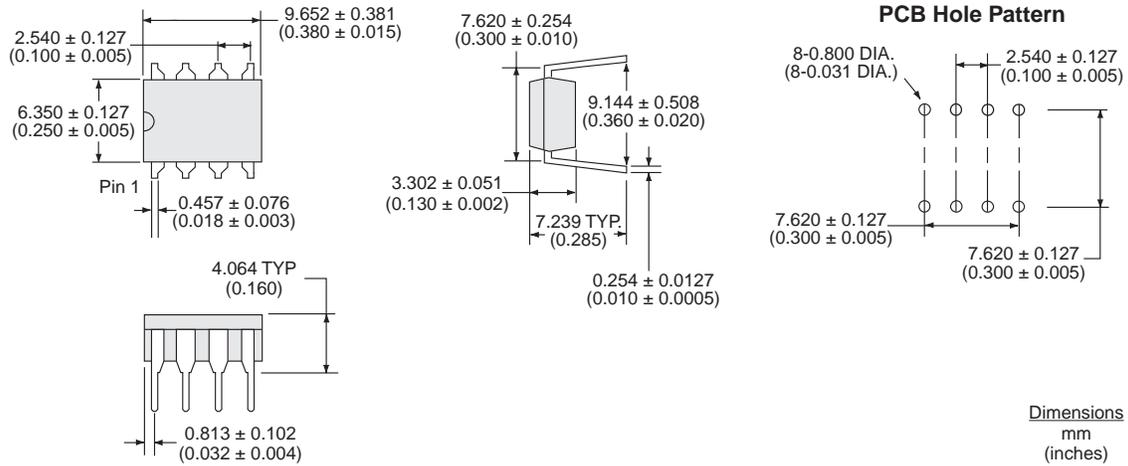


5.5.4 YI (5-Pin TO-263)



- NOTES:
1. Reference JEDEC TO-263 Type "BA".
 2. Dimension does not include mold flash; mold flash shall not exceed 0.127mm (0.005 inch) per side.
 3. Minimum plating: 1000 microinches.
 4. Controlling dimension: millimeters.

5.5.5 PI (8-Pin DIP)



5.5.6 CI (5-Pin TO-220)

