



# PDTD114ET

50 V, 500 mA NPN resistor-equipped transistor;  
R1 = 10 kΩ, R2 = 10 kΩ

13 October 2022

Product data sheet

## 1. General description

NPN Resistor-Equipped Transistor (RET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTB114ET

## 2. Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- $\pm 10\%$  resistor ratio tolerance
- High temperature applications up to 175 °C
- AEC-Q101 qualified

## 3. Applications

- IC inputs control
- Cost-saving alternative to BC807 series transistors in digital applications
- Switching loads

## 4. Quick reference data

Table 1. Quick reference data

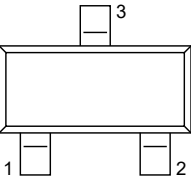
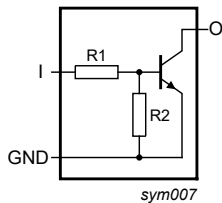
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	50	V
I <sub>O</sub>	output current			-	-	500	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.9	1	1.1	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 500 mA NPN resistor-equipped transistor; R1 = 10 k $\Omega$ , R2 = 10 k $\Omega$ 

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p style="text-align: center;"><b>SOT23</b></p>	 <p style="text-align: center;"><i>sym007</i></p>
2	GND	ground (emitter)		
3	O	output (collector)		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
<a href="#">PDTD114ET</a>	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	<a href="#">SOT23</a>

## 7. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
PDTD114ET	%10

[1] % = placeholder for manufacturing site code

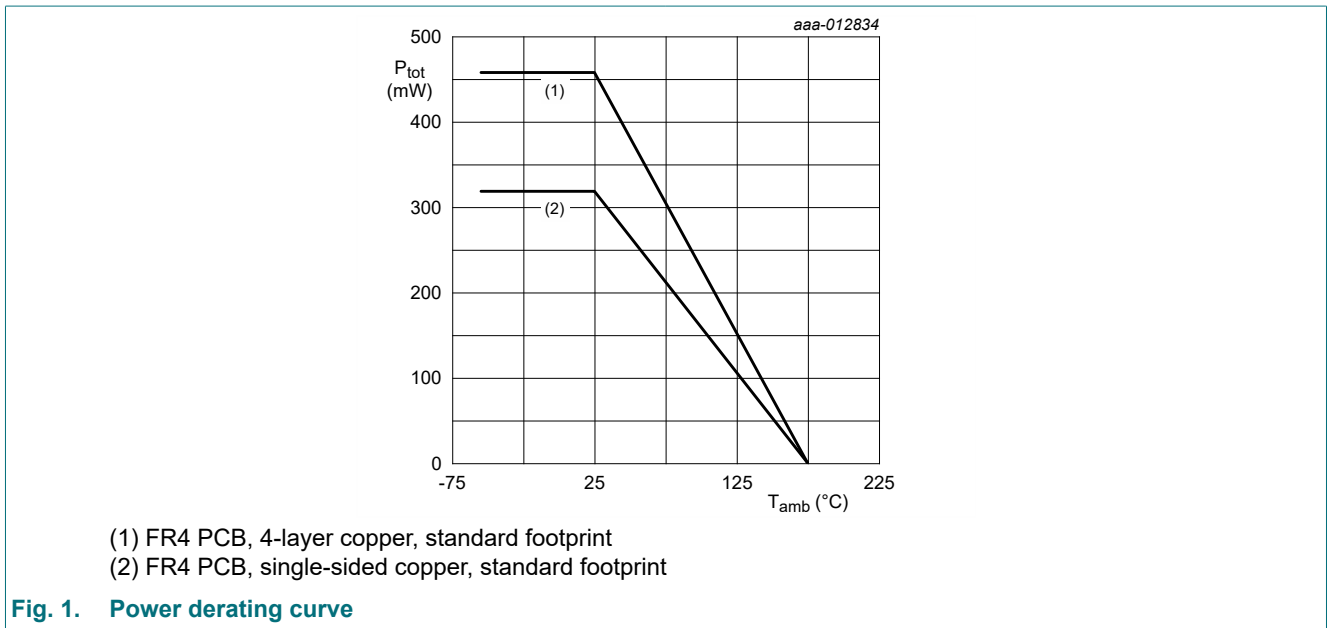
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>CBO</sub>	collector-base voltage	open emitter	-	50	V	
V <sub>CEO</sub>	collector-emitter voltage	open base	-	50	V	
V <sub>EBO</sub>	emitter-base voltage	open collector	-	10	V	
V <sub>I</sub>	input voltage	positive	-10	50	V	
I <sub>O</sub>	output current		-	500	mA	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	320	mW
			[2]	-	460	mW
T <sub>j</sub>	junction temperature		-	175	°C	
T <sub>amb</sub>	ambient temperature		-55	175	°C	
T <sub>stg</sub>	storage temperature		-55	175	°C	

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.



**Fig. 1. Power derating curve**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	470	K/W
			[2]	-	-	327	K/W

- [1] Device mounted on an FR4 PCB, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

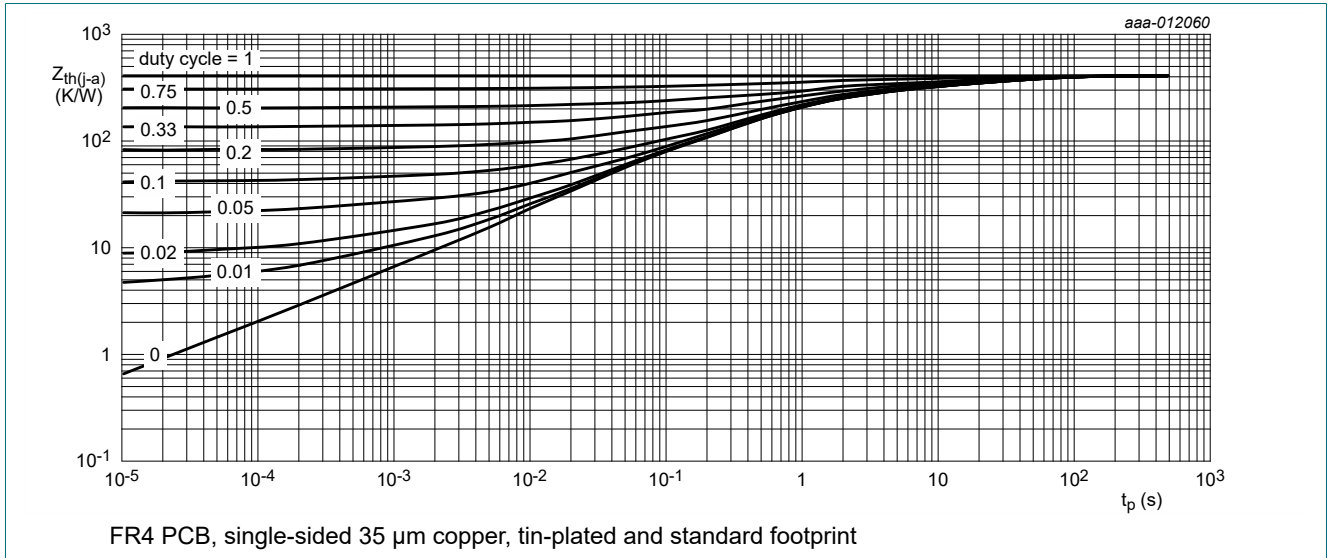


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

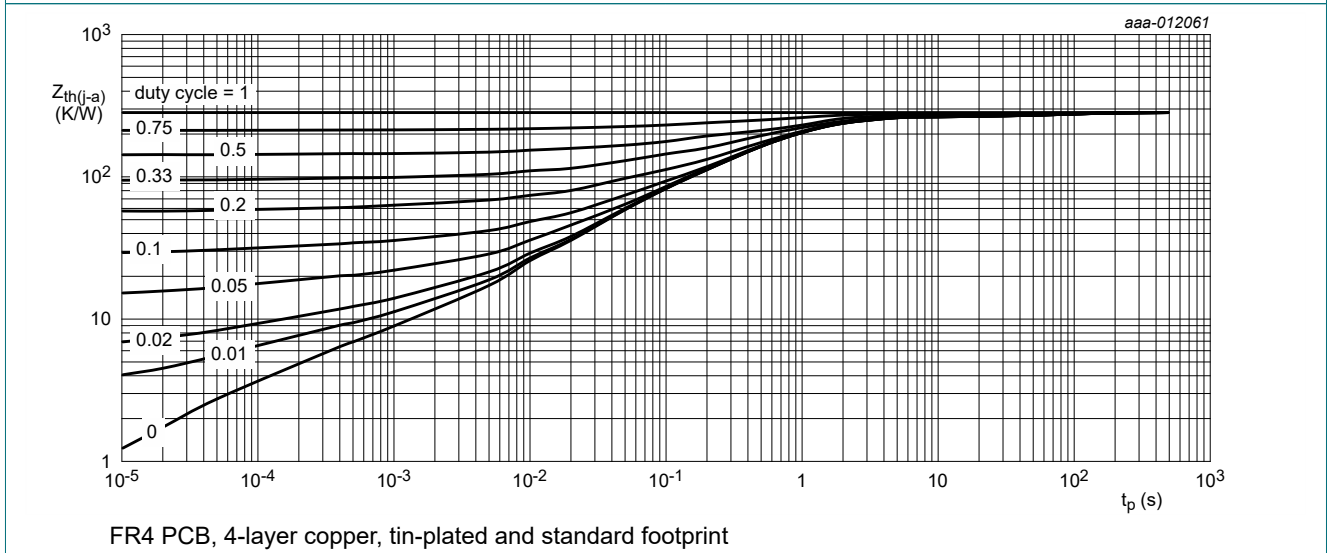


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

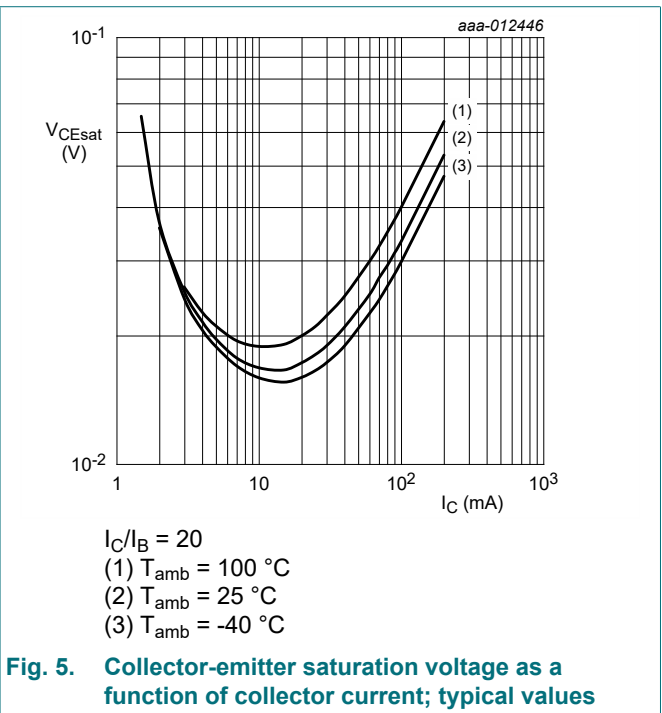
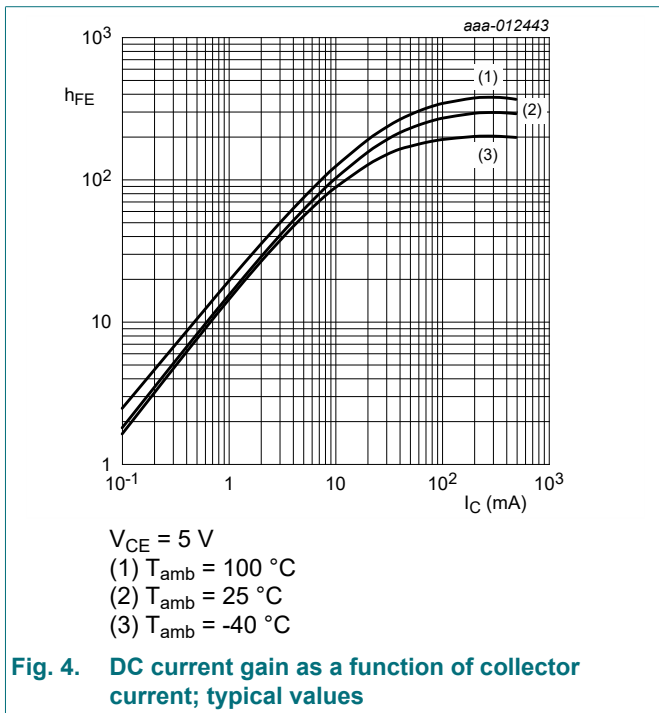
## 10. Characteristics

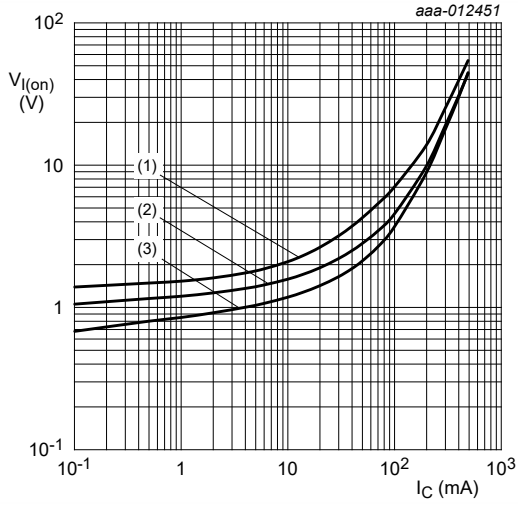
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu A; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 10 \text{ mA}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	50	-	-	V	
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 40 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	100	nA	
		$V_{CB} = 50 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	100	nA	
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 50 \text{ V}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	0.5	$\mu A$	
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	0.4	mA	
$h_{FE}$	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 50 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	70	-	-		
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 50 \text{ mA}; I_B = 2.5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	-	-	100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_C = 100 \mu A; T_{amb} = 25 \text{ }^\circ C$	0.6	1	1.5	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_C = 20 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	1	1.9	3	V	
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.9	1	1.1	
$C_c$	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	-	7	-	pF	
$f_T$	transition frequency	$V_{CE} = 5 \text{ V}; I_C = 50 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	[2]	-	225	-	MHz

[1] See "Section 11: Test information" for resistor calculation and test conditions.

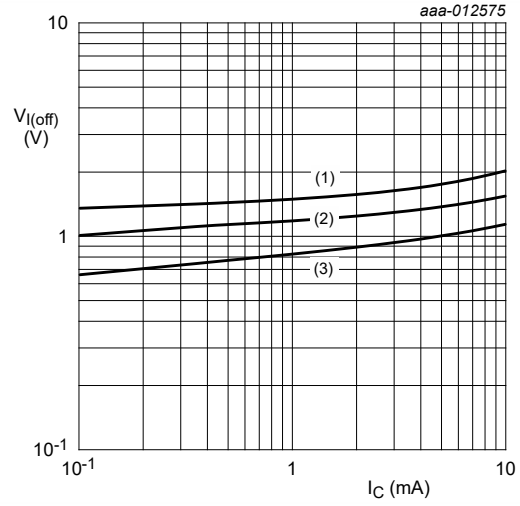
[2] Characteristics of built-in transistor.





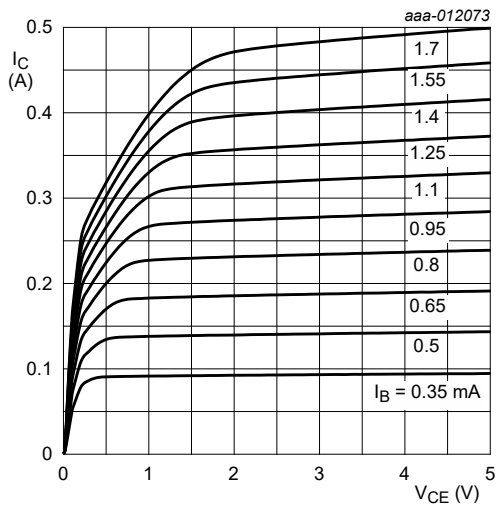
$V_{CE} = 0.3$  V  
 (1)  $T_{amb} = -40$  °C  
 (2)  $T_{amb} = 25$  °C  
 (3)  $T_{amb} = 100$  °C

**Fig. 6. On-state input voltage as a function of collector current; typical values**



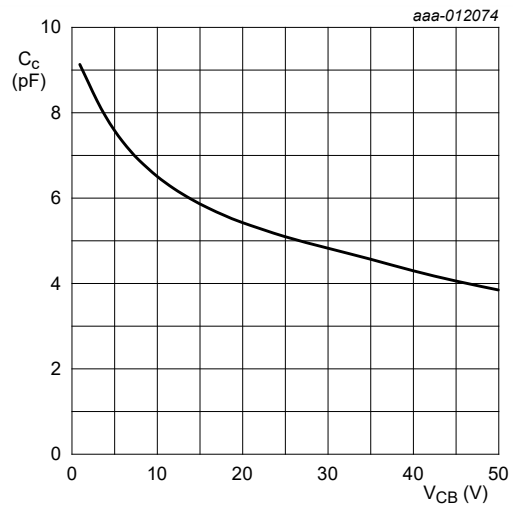
$V_{CE} = 5$  V  
 (1)  $T_{amb} = -40$  °C  
 (2)  $T_{amb} = 25$  °C  
 (3)  $T_{amb} = 100$  °C

**Fig. 7. Off-state input voltage as a function of collector current; typical values**



$T_{amb} = 25$  °C

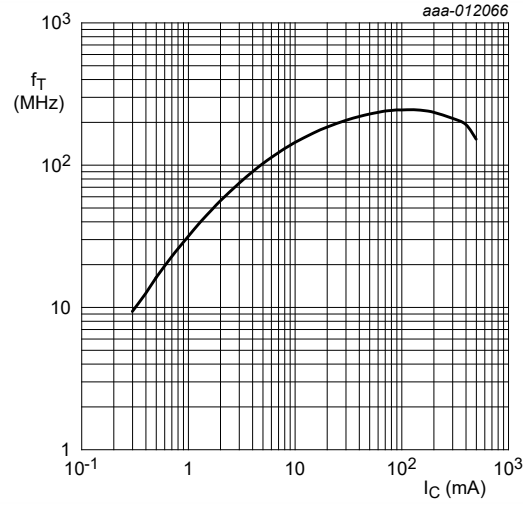
**Fig. 8. Collector current as a function of collector-emitter voltage; typical values**



$f = 1$  MHz  
 $T_{amb} = 25$  °C

**Fig. 9. Collector capacitance as a function of collector-base voltage; typical values**

50 V, 500 mA NPN resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ



f = 100 MHz  
 $T_{amb} = 25\text{ }^\circ\text{C}$   
 $V_{CE} = 5\text{ V}$

Fig. 10. Transition frequency as a function of collector current; typical values of built-in transistor

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

### Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

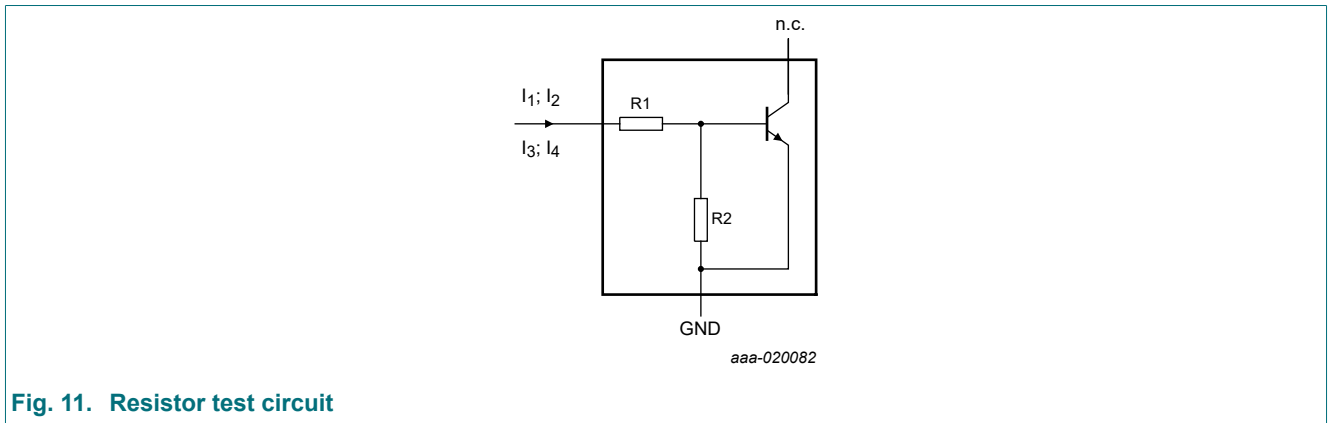


Fig. 11. Resistor test circuit

### Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>
PDTD114ET	10	10	0.7 mA	0.8 mA	-0.45 mA	-0.55 mA

## 12. Package outline

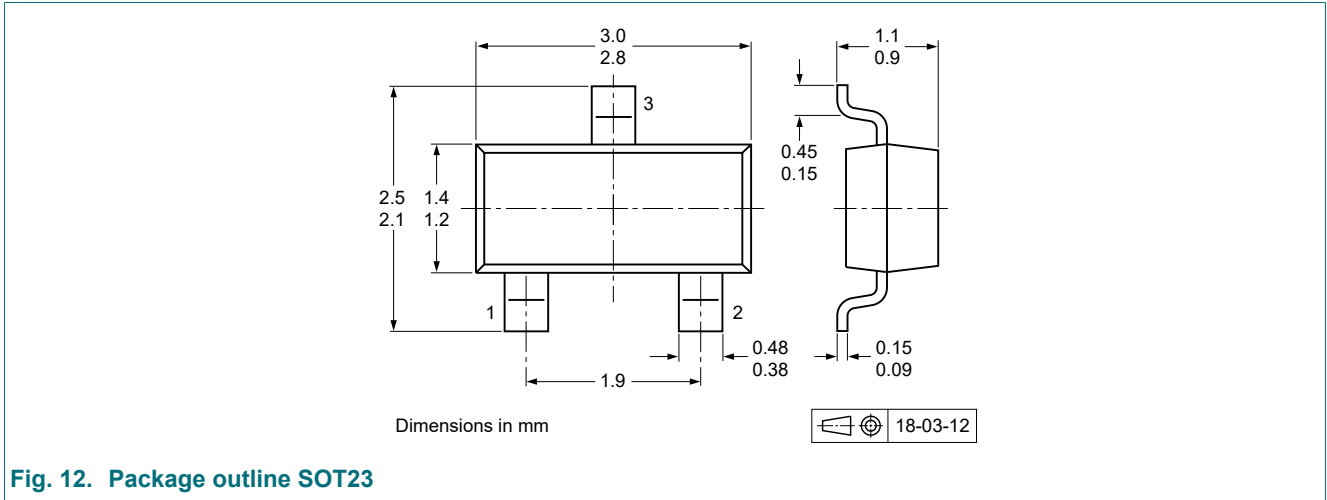


Fig. 12. Package outline SOT23

### 13. Soldering

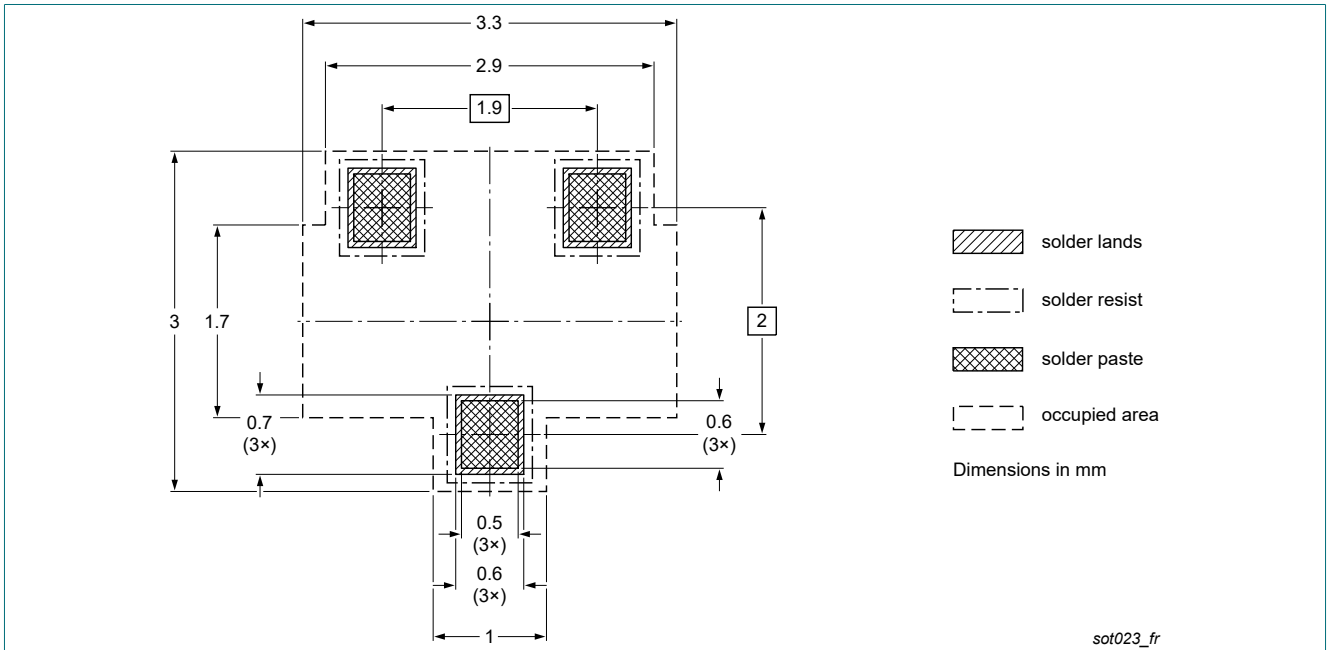


Fig. 13. Reflow soldering footprint for SOT23

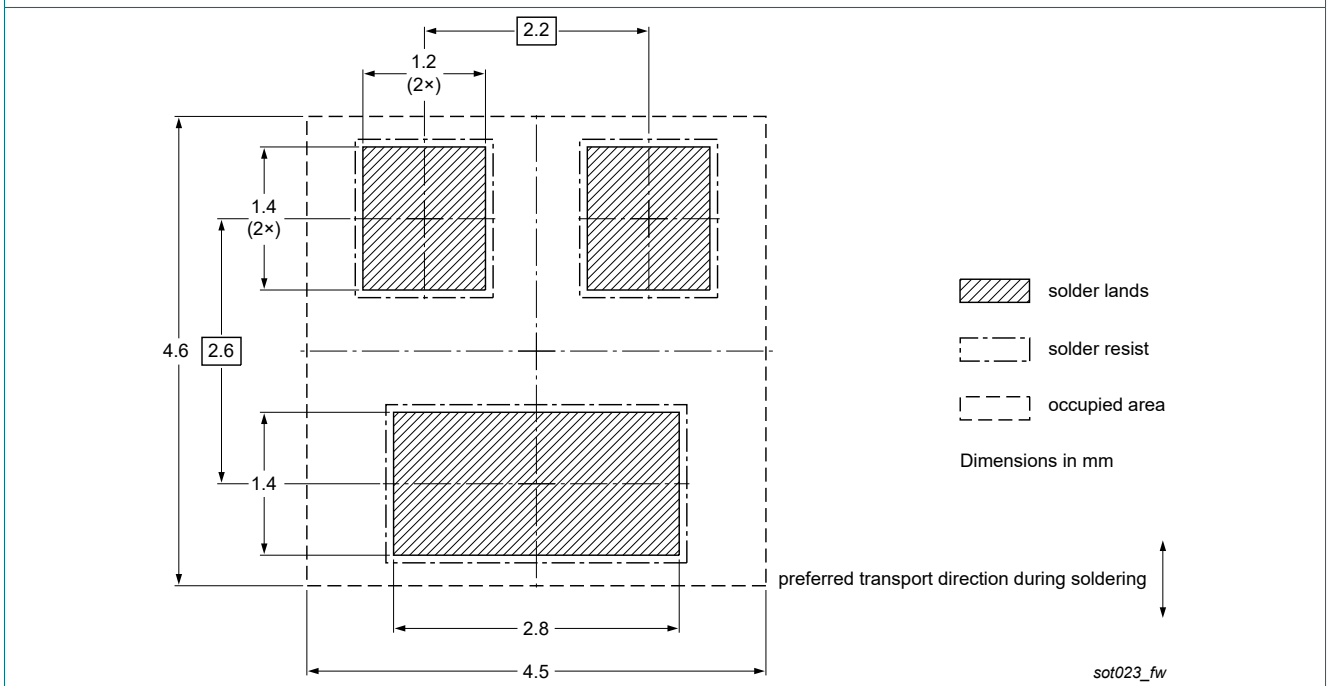


Fig. 14. Wave soldering footprint for SOT23

## 14. Revision history

**Table 9. Revision history**

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTD114ET v.2	20221013	Product data sheet	-	PDTD1XXXT_SER v.1
Modifications:	• Family data sheet reduced to single type data sheet.			
PDTD1XXXT_SER v.1	20140515	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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