

PJE5UFN10A

Ultra Low Capacitance TVS/ESD Protection

V_{RWM}

5 V

Features

- IEC61000-4-2(ESD): ±15kV Air, ±8kV Contact Compliance
- IEC61000-4-4(EFT): 20A(5/50nS)
- IEC61000-4-5(Lightning): 2.5A(8/20μS)
- Low leakage current, maximum 1μA at rated voltage
- Lead free in compliance with EU RoHS 2011/65/EU directive.
- Green molding compound as per IEC61249 Std.
(Halogen Free)

Mechanical Data

- Case: DFN2510-10L, Plastic
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.00004 ounces, 0.0011 grams
- Marking: JE5U

Applications

- USB3.0 Data Line Protection
- High Definition Multi-Media Interface Protection
- Monitors and Flat Panel Displays Notebook computers
- Video Line Protection & Base Stations
- 10/100/1000 Ethernet
- HDSL, IDSL Secondary IC Side Protection
- Control Signal Lines Protection

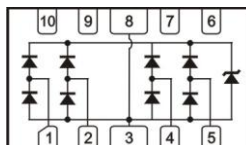
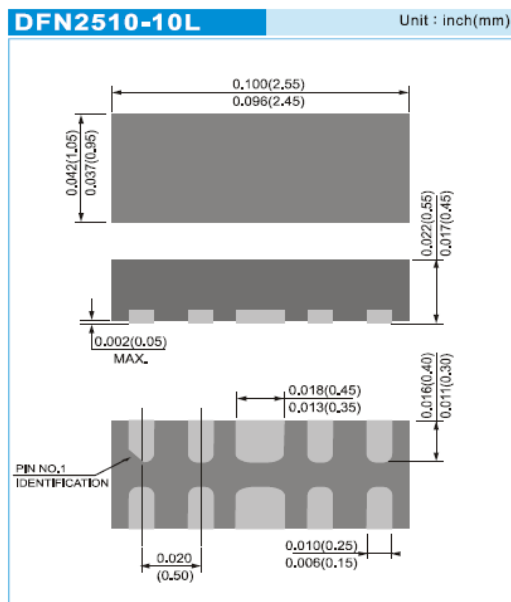


Fig.175(Top View)

Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNITS
ESD IEC61000-4-2(Air)	V_{ESD}	±15	kV
ESD IEC61000-4-2(Contact)		±8	
Operating Junction Temperature Range	T_J	-55 to +150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55 to +150	$^{\circ}\text{C}$



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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	5	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR}=1\text{mA}$, Between any I/O pins to GND	6	-	9	V
Reverse leakage current	I_R	$V_R=5\text{V}$, any I/O pin to GND	-	-	1	μA
Clamping Voltage	V_{CL}	$I_{PP}=1\text{A}$, $t_P=8/20\mu\text{s}$, any I/O pin to GND	-	9.5	12	V
		$I_{PP}=2.5\text{A}$, $t_P=8/20\mu\text{s}$, any I/O pin to GND	-	11	13	
Clamping Voltage TLP ^(Note 1)	V_{CL}	$I_{PP}=4\text{A}$, $t_P=100\text{ns}$, any I/O pin to GND	-	12	-	V
		$I_{PP}=8\text{A}$, $t_P=100\text{ns}$, any I/O pin to GND	-	14	-	
Dynamic Resistance ^(Note 1)	R_{DYN}	$t_P=100\text{ns}$	-	0.5	-	Ω
Off State Junction Capacitance	C_J	0Vdc Bias $f=1\text{MHz}$, Between any I/O pins to GND	-	0.6	0.8	pF
		0Vdc Bias $f=1\text{MHz}$, Between any I/O pins	-	0.35	0.4	

NOTES :

1. Testing using Transmission Line Pulse (TLP) conditions: $Z_0 = 50\Omega$, $t_P = 100\text{ ns}$.



PJE5UFN10A

TYPICAL CHARACTERISTIC CURVES

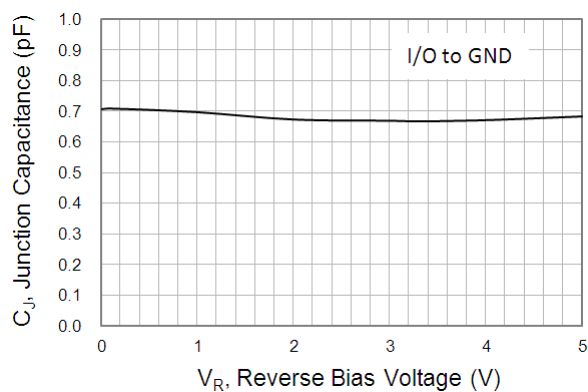


Fig.1 Typical Junction Capacitance

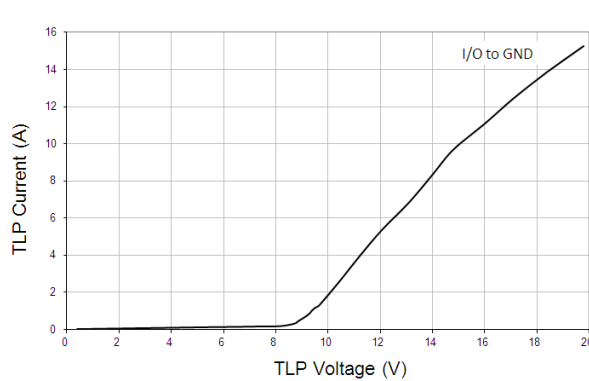


Fig.2 Transmission Line Pulsing (TLP) Measurement

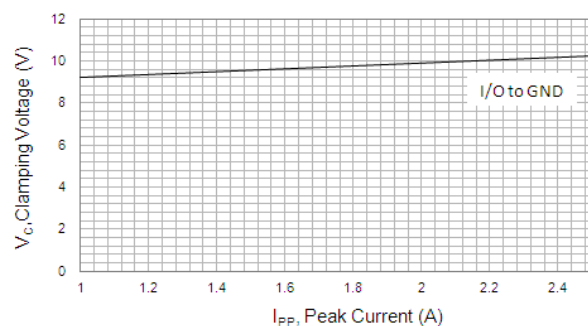


Fig.3 Typical Peak Clamping Voltage(8/20 μ s)

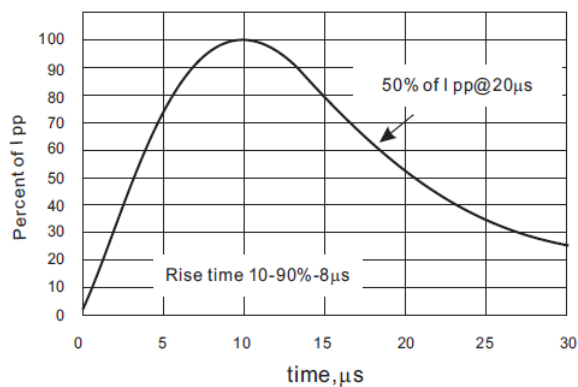


Fig.4 8/20 μ s Pulse Waveform



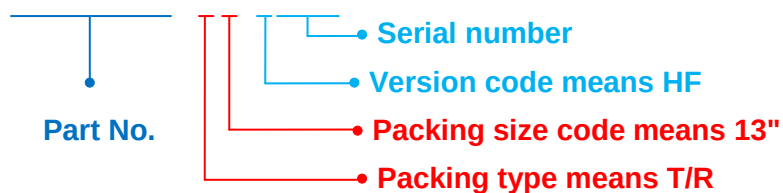
PJE5UFN10A

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing Type	Marking	Version
PJE5UFN10A_R1_00001	DFN2510-10L	5K pcs / 7" reel	JE5U	Halogen free
PJE5UFN10A_R2_00001	DFN2510-10L	12K pcs / 13" reel	JE5U	Halogen free

For example :

RB500V-40_R2_00001



Packing Code XX				Version Code XXXXX		
Packing type	1 st Code	Packing size code	2 nd Code	HF or RoHS	1 st Code	2 nd ~5 th Code
Tape and Ammunition Box (T/B)	A	N/A	0	HF	0	serial number
Tape and Reel (T/R)	R	7"	1	RoHS	1	serial number
Bulk Packing (B/P)	B	13"	2			
Tube Packing (T/P)	T	26mm	X			
Tape and Reel (Right Oriented) (TRR)	S	52mm	Y			
Tape and Reel (Left Oriented) (TRL)	L	PANASERT T/B CATHODE UP (PBCU)	U			
FORMING	F	PANASERT T/B CATHODE DOWN (PBCD)	D			

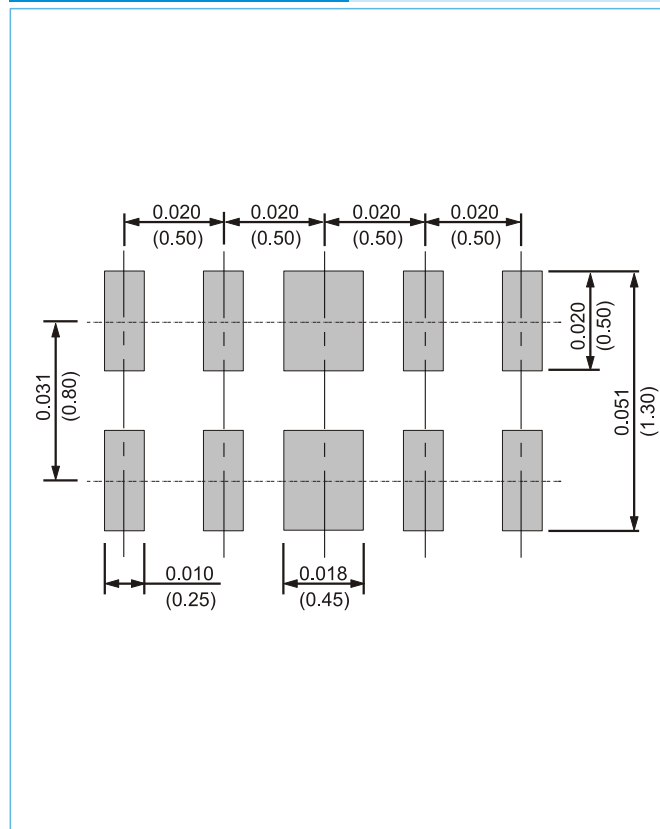


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MOUNTING PAD LAYOUT

DFN2510-10L

Unit : inch(mm)





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