PL133-47

Low-Power DC to 150 MHz 1:4 Fanout Buffer IC

Features

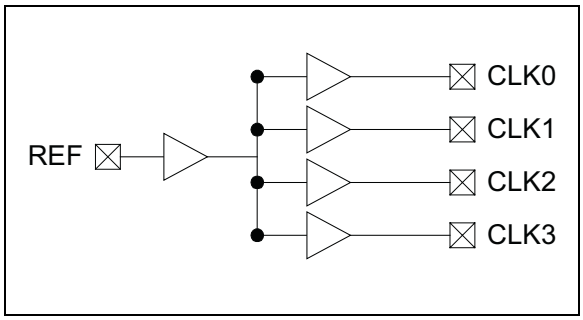
- 1:4 LVCMOS Output Fanout Buffer from DC to150 MHz
- Low Additive Phase Jitter of 60 fs RMS
- 8 mA Output Drive Strength
- Low Power Consumption for Portable Applications
- Automotive Applications Grade Compliant
- Low Input-Output Delay
- Output-Output Skew <250 ps
- 2.5V to 3.3V, ±10% Operation
- 1.8V +10%/–5% Operation up to 67 MHz
- Operating Temperature Range:
  - Commercial: 0°C to +70°C
  - Industrial: –40°C to +85°C
- Available in 8-Pin SOIC Package

General Description

The PL133-47 is an advanced fanout buffer design for high performance, low-power, small form factor applications. The PL133-47 accepts a reference clock input from DC to 150 MHz and provides four outputs of the same frequency.

The PL133-47 is offered in a SOIC-8L package and it offers the best phase noise, additive jitter performance, and lowest power consumption of any comparable IC.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC Input Voltage ..... V_{SS} – 0.5V to +4.6V
Static Discharge Voltage
(Per MIL-STD-883, Method 3015) ..... >2000V

Operating Ratings †

Supply Voltage, V_{DD} ..... 1.71V to 3.63V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input Low Voltage	V_{IL}	—	—	0.3xV_{DD}	V	Note 1
Input High Voltage	V_{IH}	0.7xV_{DD}	—	—	V	Note 1
Input Low Current	I_{IL}	—	—	50	µA	V_{IN} = 0V
Input High Current	I_{IH}	—	—	100	µA	V_{IN} = V_{DD}
Supply Current	I_{DD}	—	—	32	mA	66.67 MHz with unloaded outputs
Output Low Voltage	V_{OL}	—	—	0.5	V	I_O = 8 mA, V_{DD} = 3.3V
		—	—	0.5		I_O = 6 mA, V_{DD} = 2.5V
		—	—	0.5		I_O = 4 mA, V_{DD} = 1.8V
Output High Voltage	V_{OH}	V_{DD} - 0.5	—	—	V	I_O = –8 mA, V_{DD} = 3.3V
		V_{DD} - 0.5	—	—		I_O = –6 mA, V_{DD} = 2.5V
		V_{DD} - 0.5	—	—		I_O = –4 mA, V_{DD} = 1.8V
Load Capacitance	C_L	—	—	30	pF	Load Capacitance, below 100 MHz, V_{DD} > 2.25V
		—	—	10		Load Capacitance between 100 MHz and 134 MHz, V_{DD} > 2.25V
		—	—	5		Load Capacitance, above 134 MHz, V_{DD} > 2.25V
		—	—	15		Load Capacitance, below 67 MHz, 1.71V < V_{DD} < 2.25V
Input Capacitance	C_{IN}	—	—	7	pF	—
Power-Up Time	t_{PU}	0.05	—	50	ms	Power-up time for all V_{DD} to reach minimum specified voltage (power ramps must be monotonic)

Note 1: REF input has a threshold voltage of V_{DD}/2.

SWITCHING CHARACTERISTICS Note 2

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Frequency	f	DC	—	150	MHz	V_{DD} = 3.3V, 2.5V
		DC	—	67	MHz	V_{DD} = 1.8V
Duty Cycle = $t_2 \div t_1$	—	40	50	60	%	Measured at $V_{DD}/2$, Input is 50%
Rise Time	t_3	—	—	1.5	ns	Measured between 0.8V and 2.0V
Fall Time	t_4	—	—	1.5	ns	Measured between 0.8V and 2.0V
Output to Output Skew Note 1	t_5	—	—	250	ps	All outputs equally loaded
Propagation Delay, REF Rising Edge to CLKX Rising Edge Note 1	t_6	1	5	9.2	ns	Measured at $V_{DD}/2$

Note 1: Parameter is guaranteed by design and characterization.

2: All parameters are specified with loaded outputs.

NOISE CHARACTERISTICS

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Additive Phase Jitter	—	—	60	—	fs	V_{DD} = 3.3V, Frequency = 100 MHz Integration range 12 kHz - 20 MHz

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges+85						
Ambient Operating Temperature (T_A)	T_A	0	—	+70	°C	Commercial
		–40		+85		Industrial
Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
8-Lead SOIC	$R_{\theta JA}$	—	103.2	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

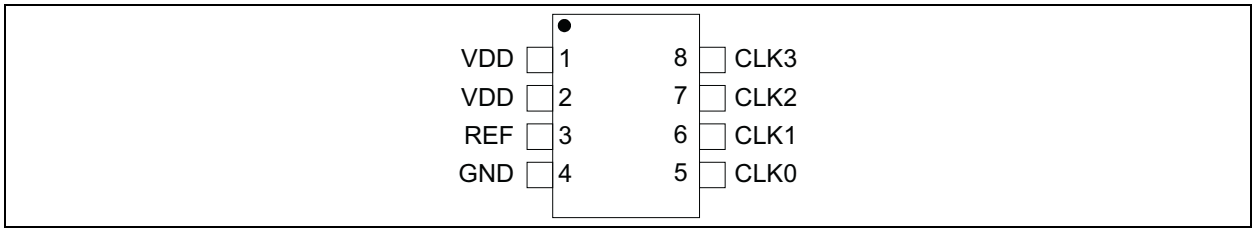


FIGURE 2-1: *Pin Configuration, 8-Lead SOIC Package.*

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	P8in Name	Type	Description
1, 2	VDD	P	Input reference frequency
3	REF	I	Buffered clock output
4	GND	P	Buffered clock output
5	CLK0	O	Buffered clock output
6	CLK1	O	Buffered clock output
7	CLK2	O	VDD connection
8	CLK3	O	GND connection

3.0 NOMINAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

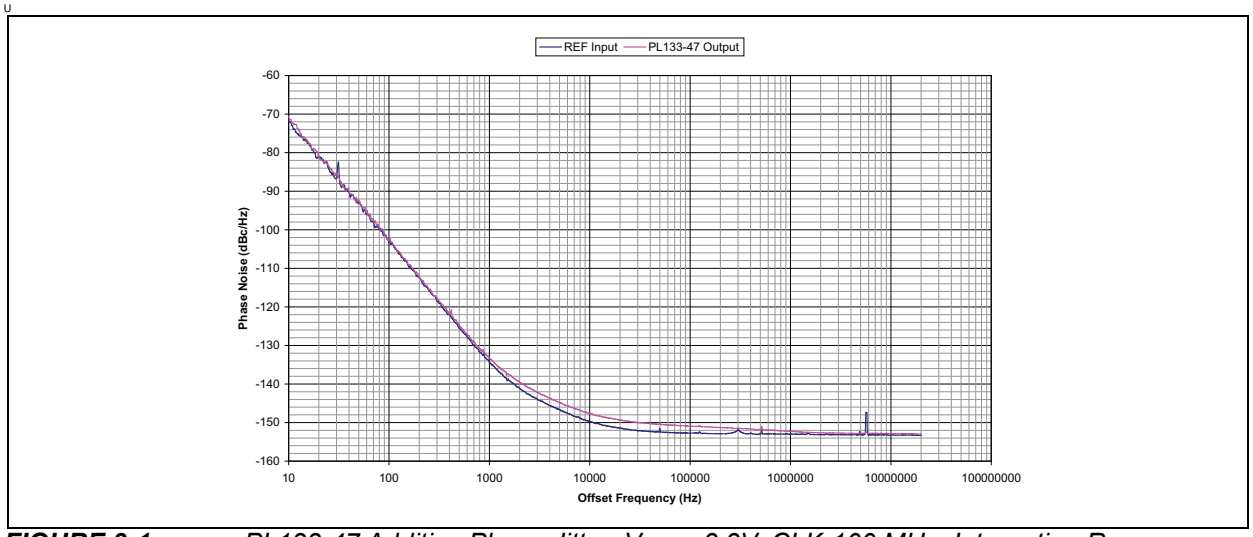


FIGURE 3-1: *PL133-47 Additive Phase Jitter: V_{DD} = 3.3V, CLK-100 MHz, Integration Range 2 kHz - 20 MHz, 0.059 ps Typical.*

When a buffer is used to pass a signal then the buffer will add a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise in the input signal. The noise added by the buffer to the input signal is quantified by the additive phase jitter defined by the following formula:

EQUATION 3-1:

$$AdditivePhaseJitter = \sqrt{(OutputPhaseJitter)^2 - (InputPhaseJitter)^2}$$

4.0 SWITCHING WAVEFORMS

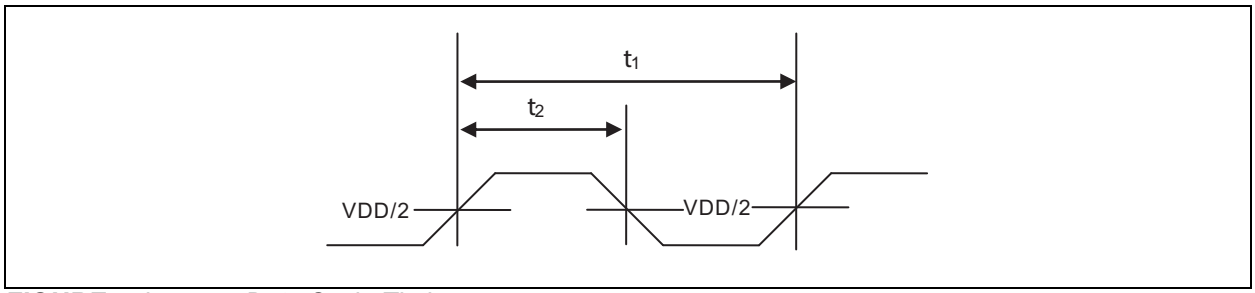


FIGURE 4-1: *Duty Cycle Timing.*

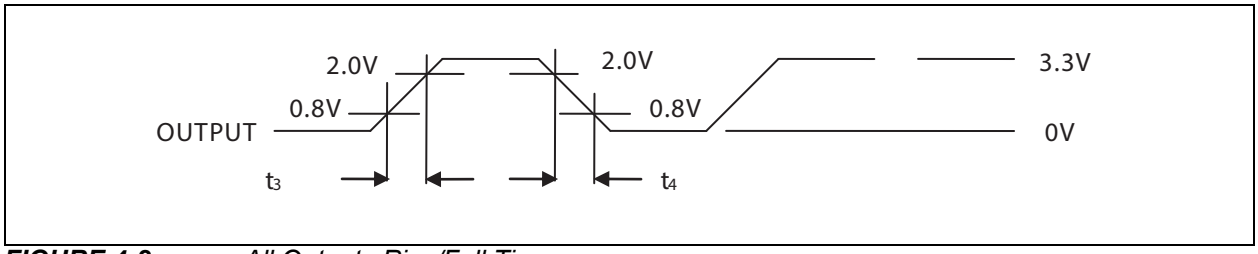


FIGURE 4-2: *All Outputs Rise/Fall Time.*

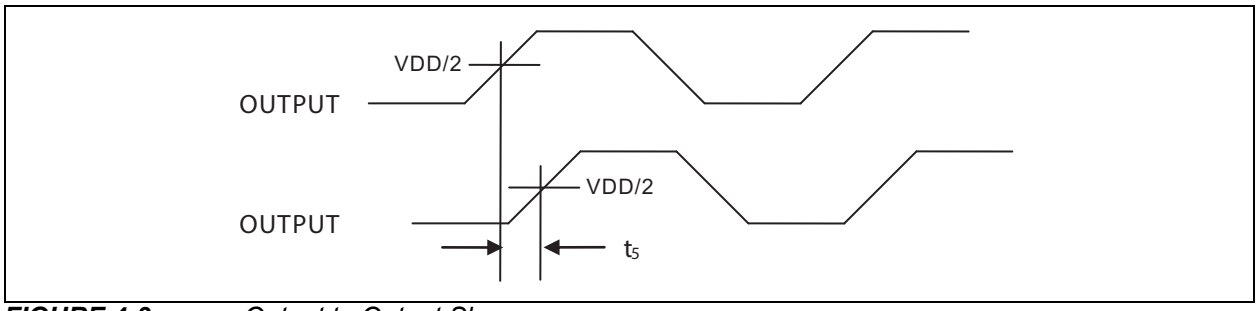


FIGURE 4-3: *Output to Output Skew.*

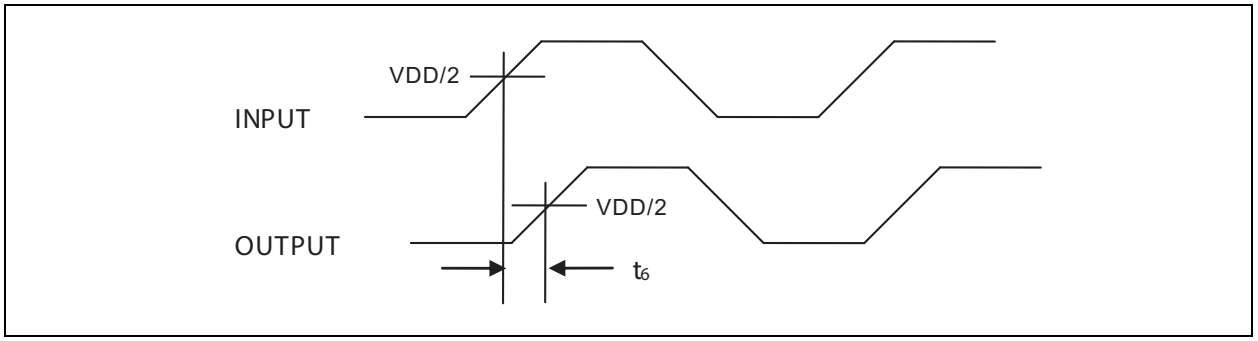


FIGURE 4-4: *Input-Output Propagation Delay.*

5.0 TEST CIRCUIT

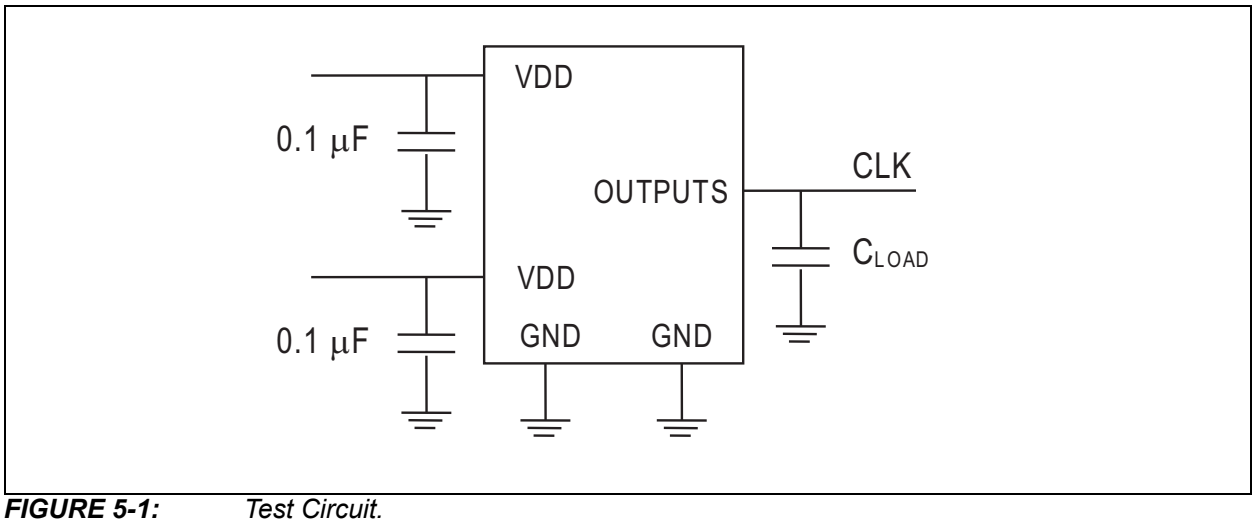


FIGURE 5-1: *Test Circuit.*

6.0 LAYOUT RECOMMENDATIONS

The following guidelines are to assist you with a performance optimized PCB design:

6.1 Signal Integrity and Termination Considerations

- Keep traces short
- Trace = Inductor. With a capacitive load this equals ringing
- Long trace = Transmission Line. Without proper termination this will cause reflections ringing and waveforms degradations.
- Use stripline or microstrip with defined impedance for long traces (> 1 inch)
- Match traces on one side of the board to avoid reflections bouncing back and forth.

6.2 Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependant. Typical values to use are 0.1 µF for designs using frequencies <50 MHz and 0.01 µF for designs using frequencies >50 MHz

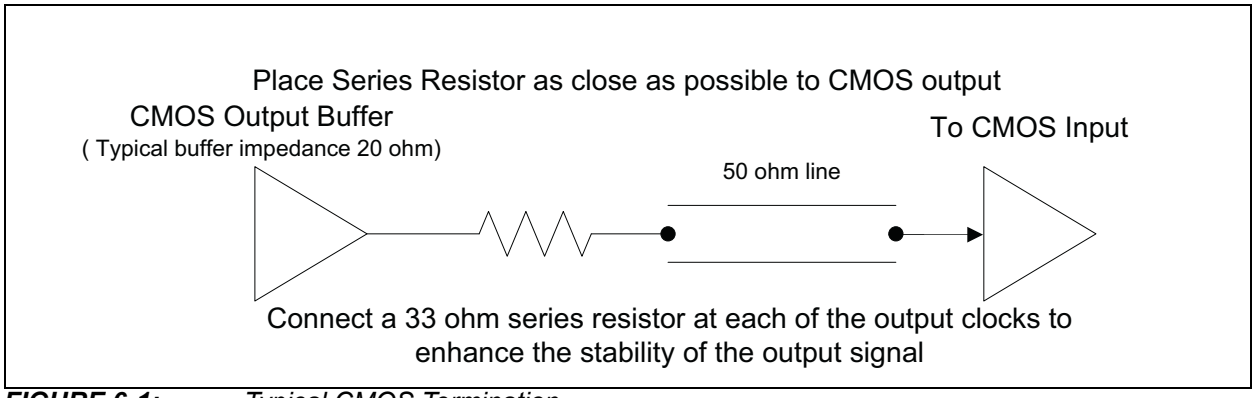


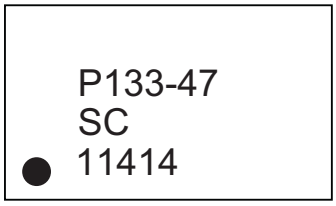
FIGURE 6-1: *Typical CMOS Termination.*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

8-Lead SOIC*

Example

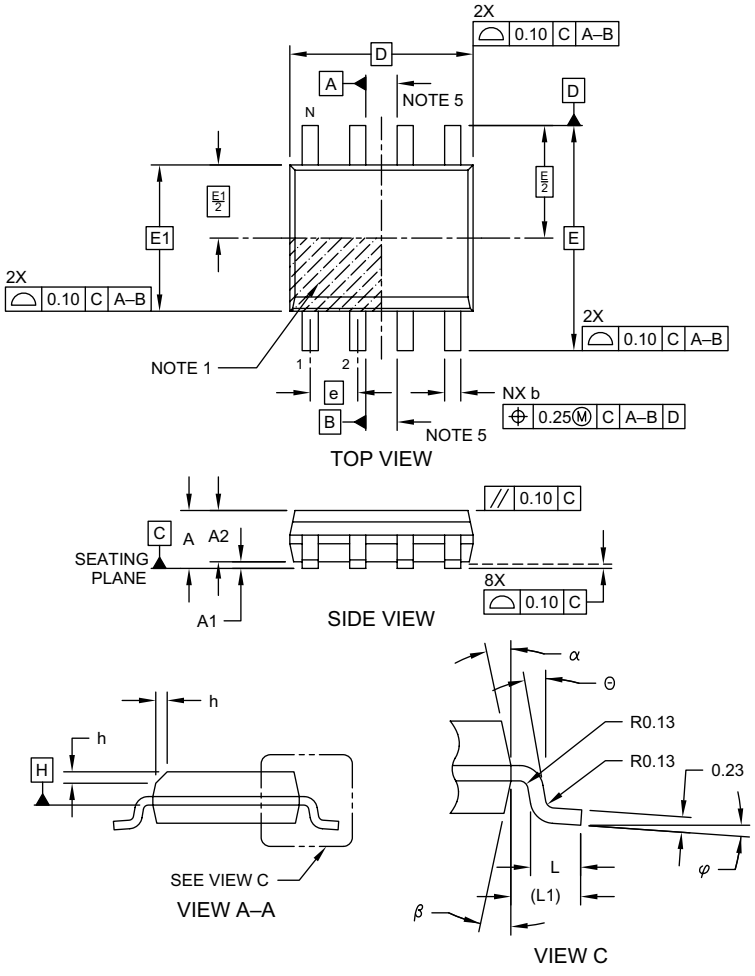


Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOIC Package Outline and Recommended Land Pattern

8-Lead Plastic Small Outline (MSB) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-MSB Rev F Sheet 1 of 2

8-Lead SOIC Package Outline and Recommended Land Pattern

8-Lead Plastic Small Outline (MSB) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

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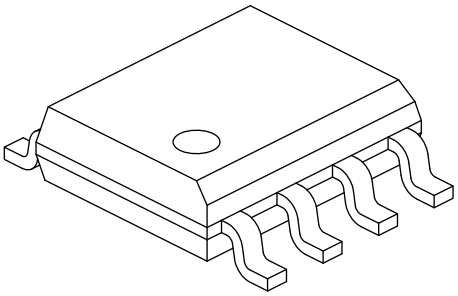


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

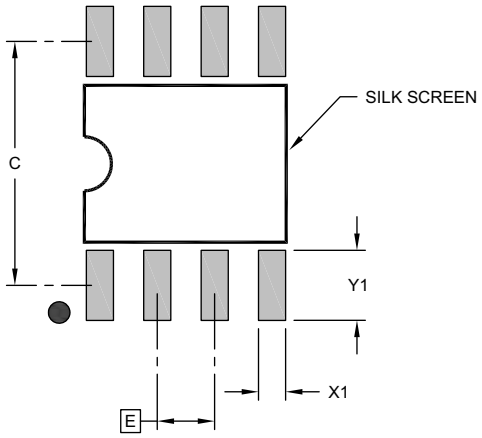
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-MSB Rev F Sheet 2 of 2

8-Lead SOIC Package Outline and Recommended Land Pattern

8-Lead Plastic Small Outline (MSB) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-MSB Rev F

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2022)

- Converted Micrel document PL133-47 to Microchip data sheet DS20006670A.
- Minor grammatical changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X
Device	Package	Temperature Range	Media Type

Device:	PL133-47:		Low-Power DC to 150 MHz 1:4 Fanout Buffer IC
Package:	S	=	3.90 mm SOIC (Plastic Small Outline) Package
Temperature Range:	C	=	0°C to +70°C (Commercial)
	I	=	–40°C to +85°C (Industrial)
Media Type:	(blank)	=	100/Tube
	R	=	2,500/Reel

Examples:

a) PL133-47SC	Low-Power DC to 150 MHz 1:4 Fanout Buffer IC, SOIC Package,0°C to +70°C, 100/Tube
b) PL133-47SC-R	Low-Power DC to 150 MHz 1:4 Fanout Buffer IC, SOIC Package, 0°C to +70°C, 2,500/Reel
c) PL133-47SI	Low-Power DC to 150 MHz 1:4 Fanout Buffer IC, SOIC Package, –40°C to +85°C, 100/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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