



PMN120ENE

60 V, N-channel Trench MOSFET

14 December 2017

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Logic-level compatible
- Very fast switching
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

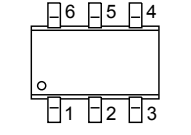
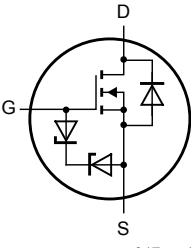
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3.1	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 2.4\text{ A}; T_j = 25\text{ °C}$	-	96	123	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>TSOP6 (SOT457)</p>	 <p>017aaa255</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN120ENE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN120ENE	3K

8. Limiting values

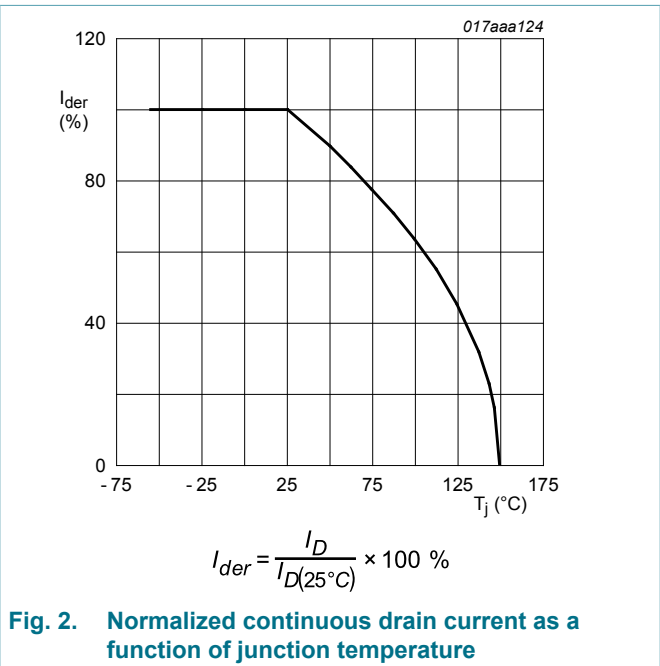
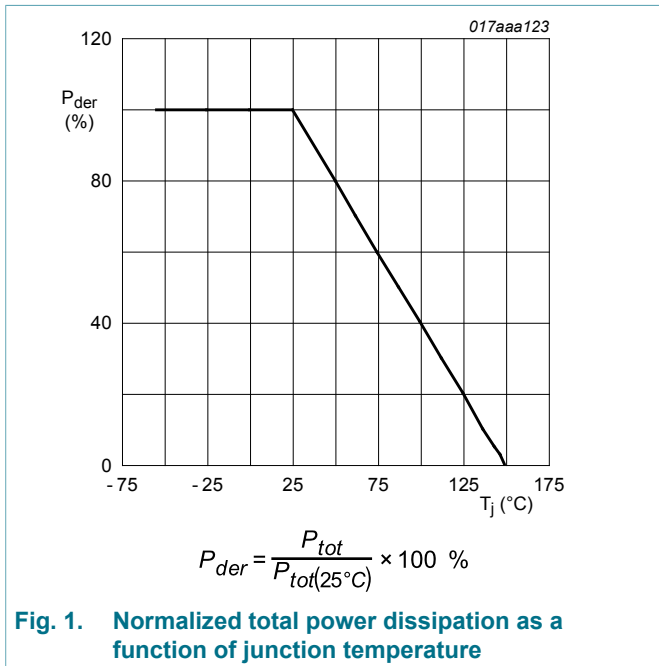
Table 5. Limiting values

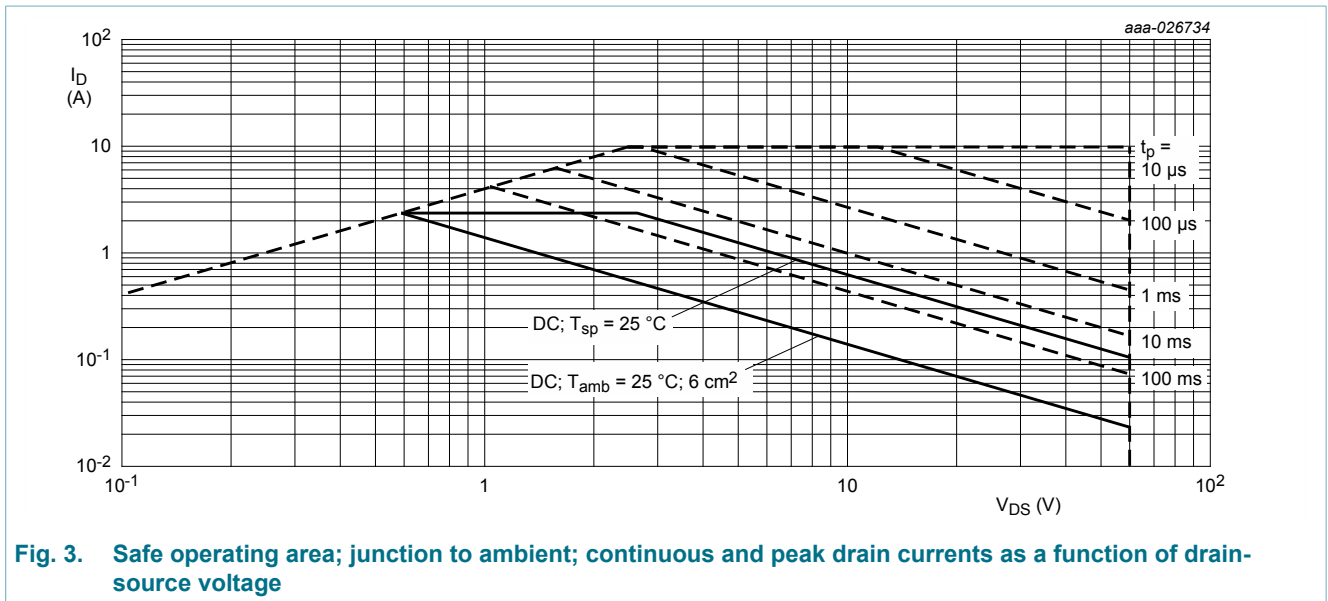
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	3.1	A
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	2.4	A
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	1.5	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	10	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	570	mW
			[1]	-	1.4	W
		T _{sp} = 25 °C		-	6.25	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.4	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



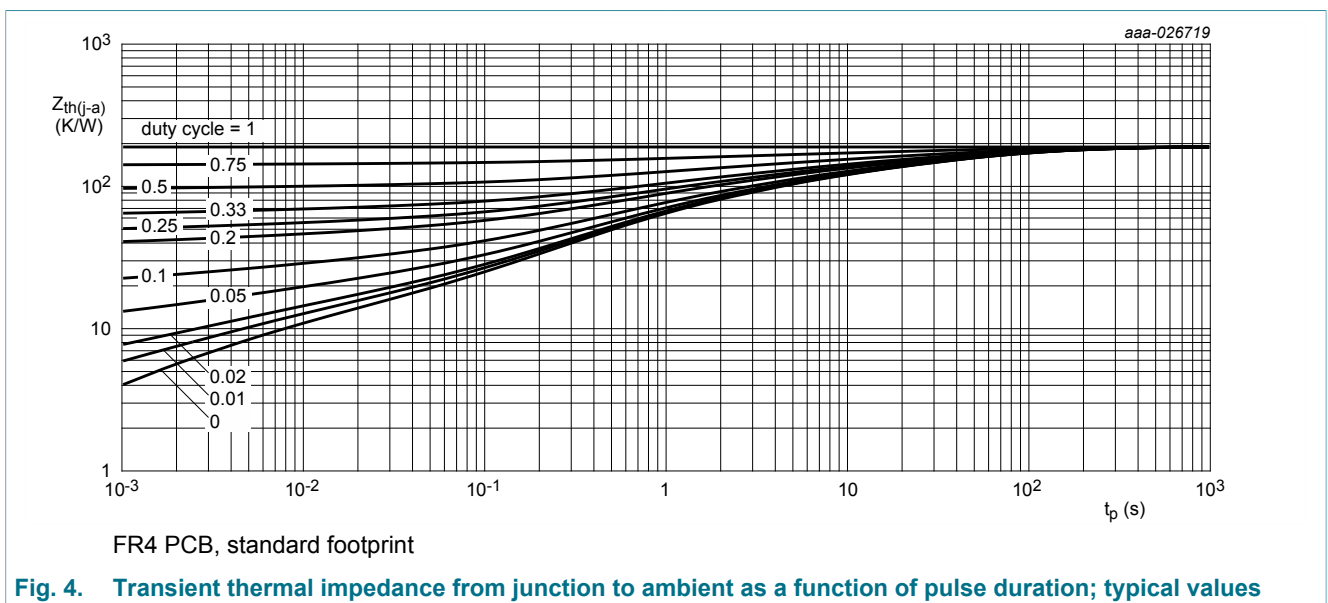


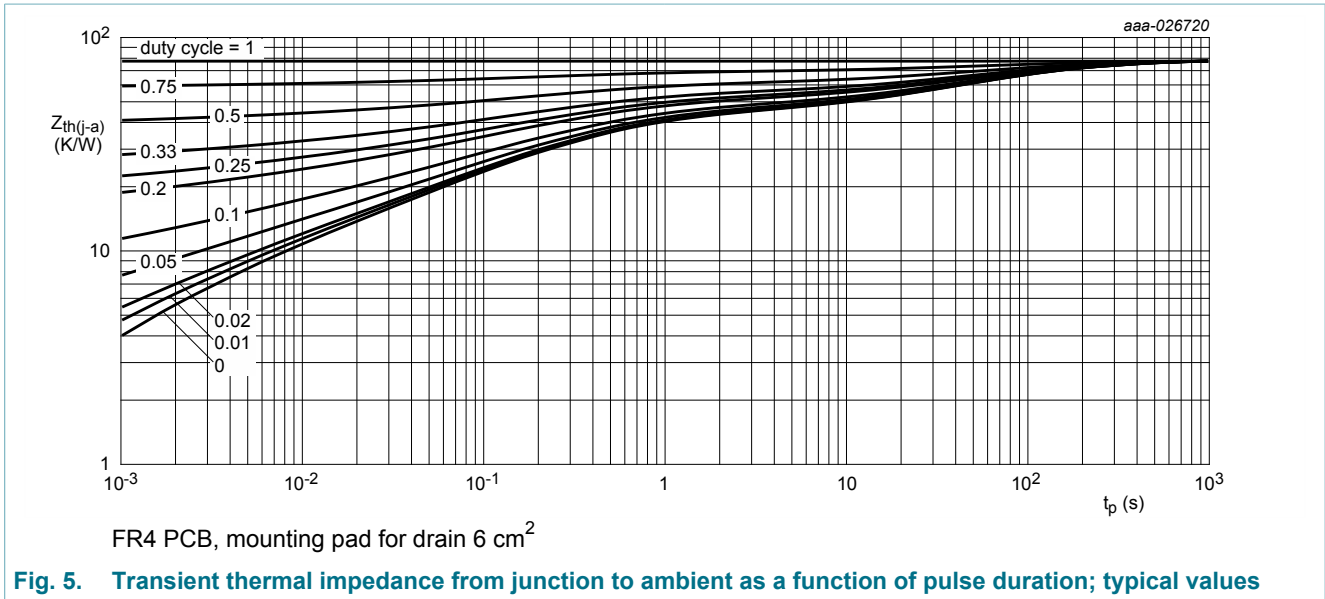
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	190	220	K/W
			[2]	-	78	90	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	15	20	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm²





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	1.3	1.7	2.7	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 2.4 A$; $T_j = 25 \text{ }^\circ C$	-	96	123	m Ω
		$V_{GS} = 10 V$; $I_D = 2.4 A$; $T_j = 150 \text{ }^\circ C$	-	192	246	m Ω
		$V_{GS} = 4.5 V$; $I_D = 2.2 A$; $T_j = 25 \text{ }^\circ C$	-	108	146	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 0.9 A$; $T_j = 25 \text{ }^\circ C$	-	10.2	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	10	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V$; $I_D = 2.1 A$; $V_{GS} = 10 V$; $T_j = 25 \text{ }^\circ C$	-	5.9	7.4	nC
Q_{GS}	gate-source charge		-	0.6	-	nC
Q_{GD}	gate-drain charge		-	1.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	275	-	pF
C_{oss}	output capacitance		-	24	-	pF
C_{rss}	reverse transfer capacitance		-	17	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 30 V$; $I_D = 2.1 A$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ C$	-	6	-
t_r	rise time	-		9	-	ns
$t_{d(off)}$	turn-off delay time	-		16	-	ns
t_f	fall time	-		6	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.4 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.8	1.2	V

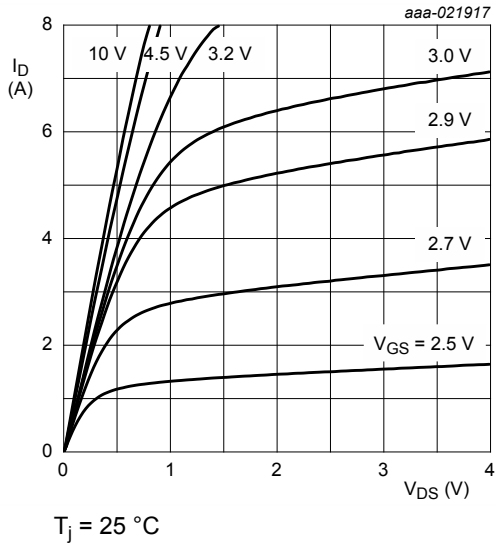


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

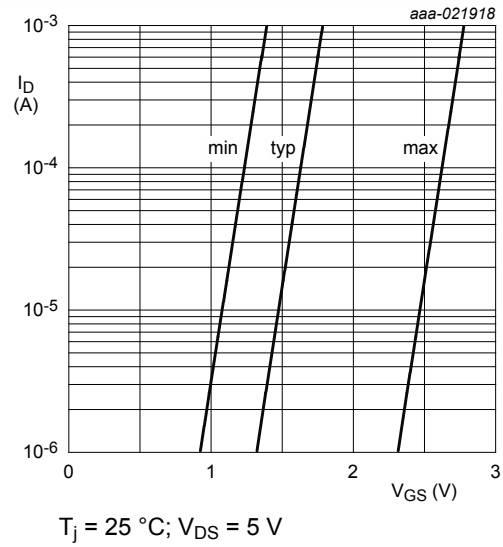


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

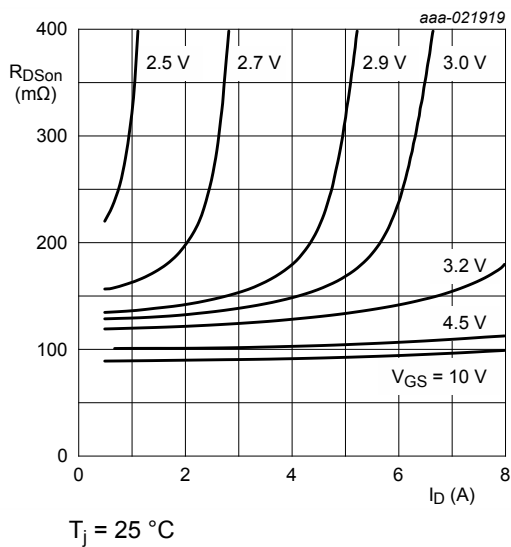


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

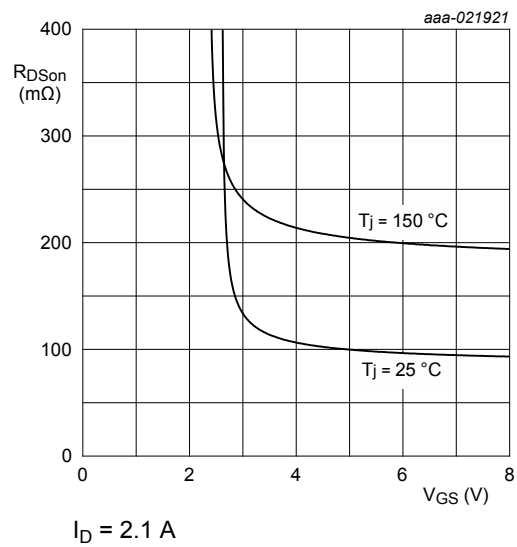
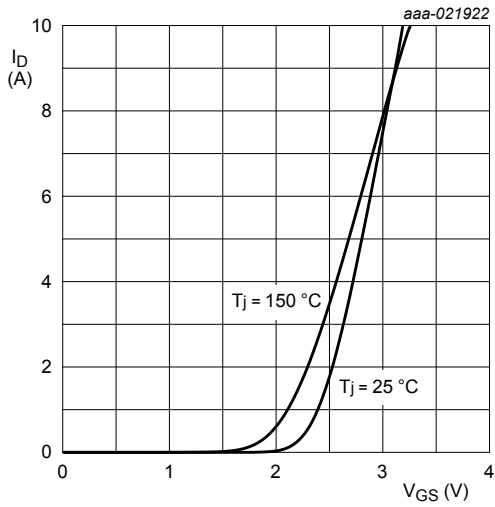
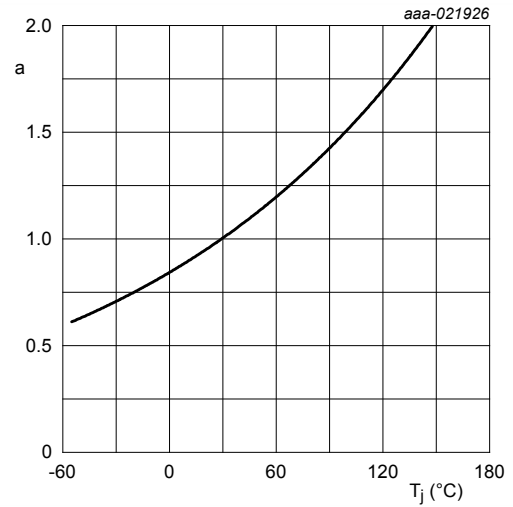


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



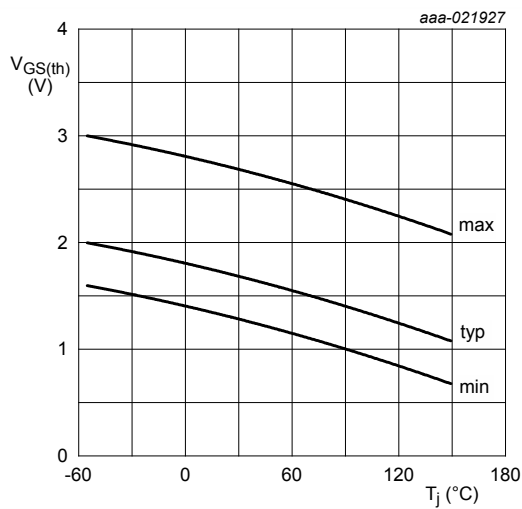
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



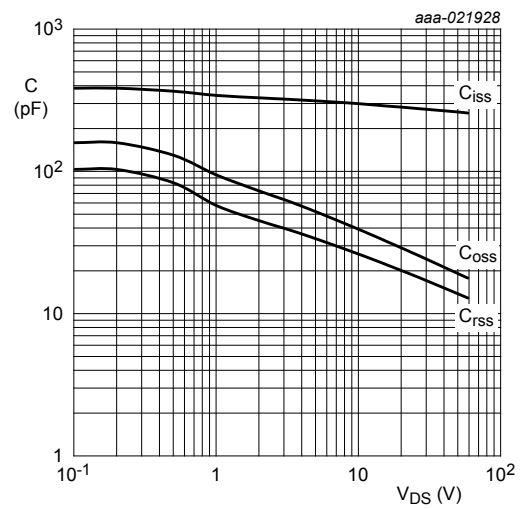
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



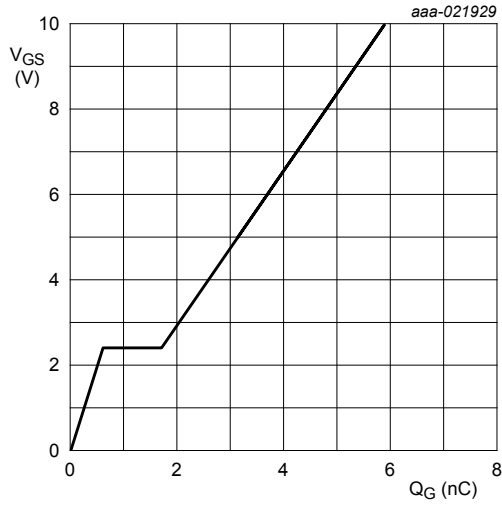
$$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 2.1 \text{ A}$; $V_{DS} = 30 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

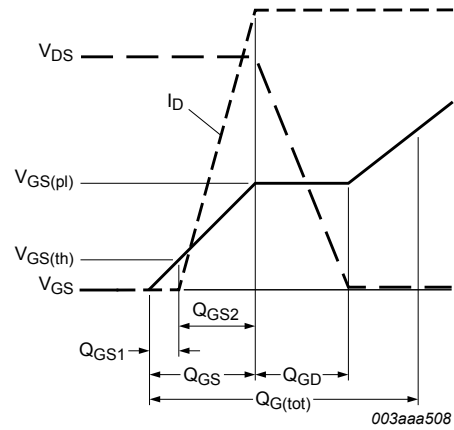
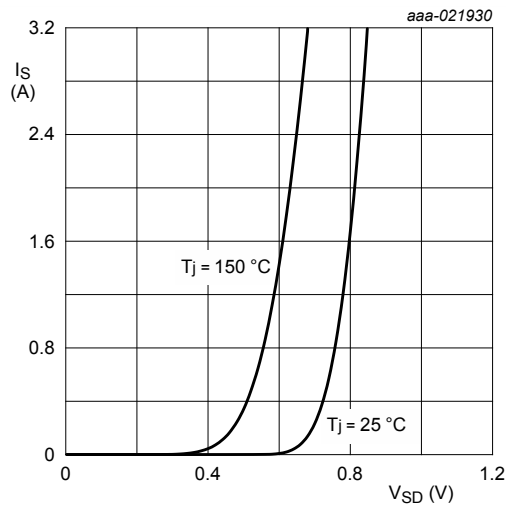


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

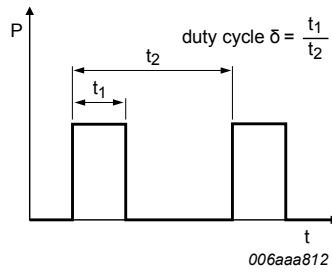


Fig. 17. Duty cycle definition

12. Package outline

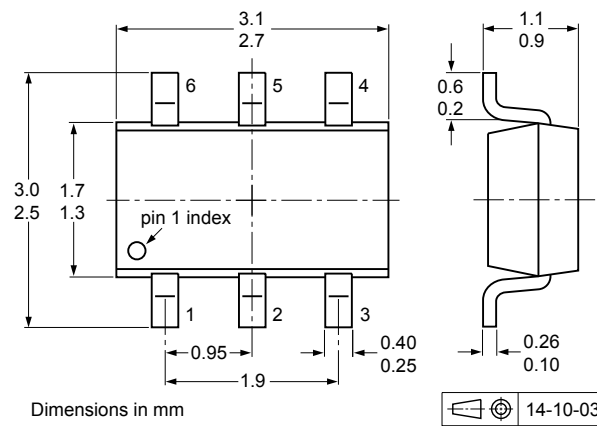


Fig. 18. Package outline TSOP6 (SOT457)

13. Soldering

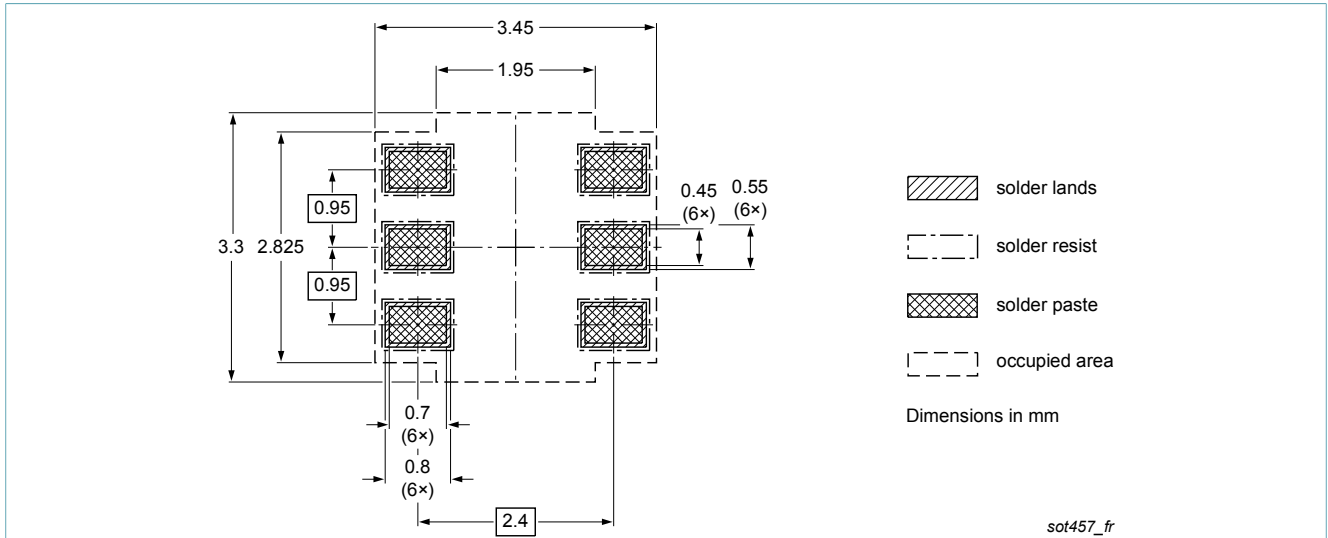


Fig. 19. Reflow soldering footprint for TSOP6 (SOT457)

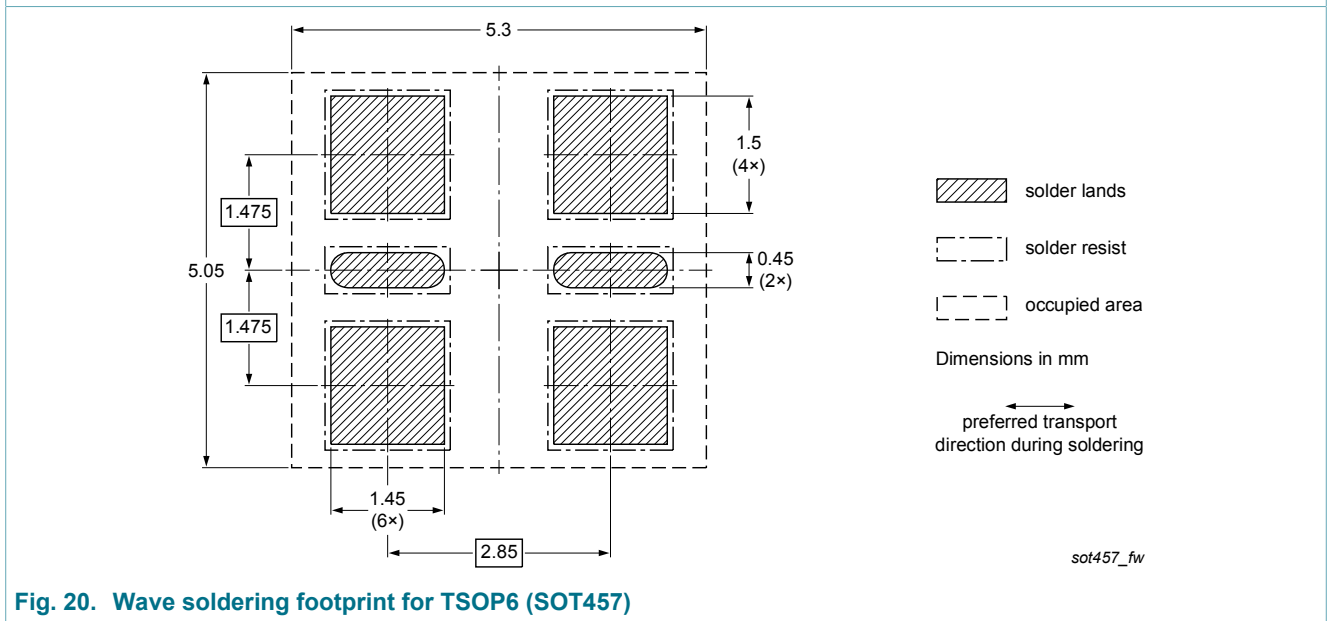


Fig. 20. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN120ENE v.2	20171214	Product data sheet	-	PMN120ENE v.1
Modifications:	<ul style="list-style-type: none">Characteristics, temperature condition removed from gate resistance.			
PMN120ENE v.1	20171127	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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