



PMPB29XNEA

30 V, N-channel Trench MOSFET

10 September 2018

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 500 V HBM (class H1B)
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

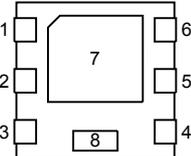
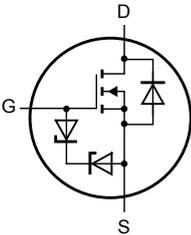
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	5	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}$	-	28	33	mΩ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa255</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB29XNEA	DFN2020MD-6	DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1220

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB29XNEA	4H

8. Limiting values

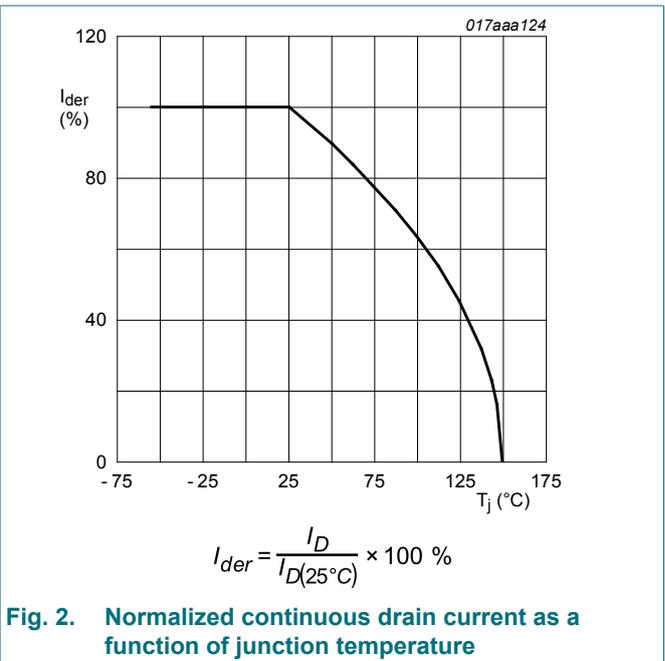
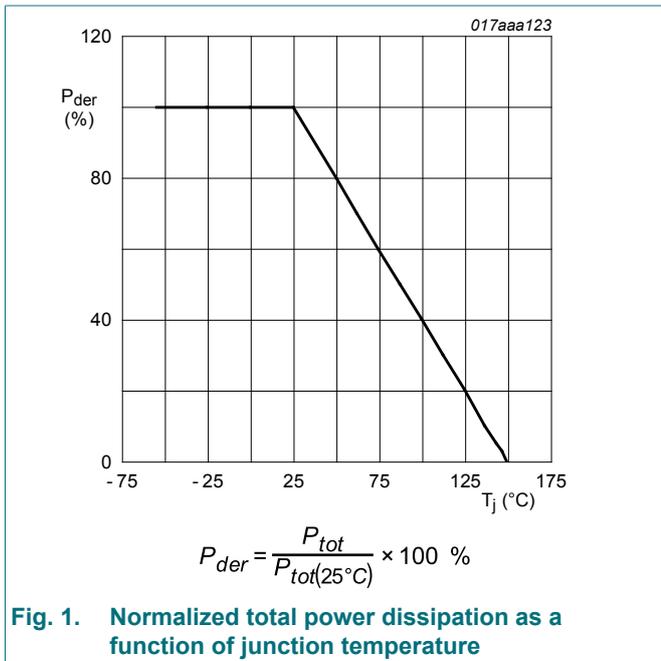
Table 5. Limiting values

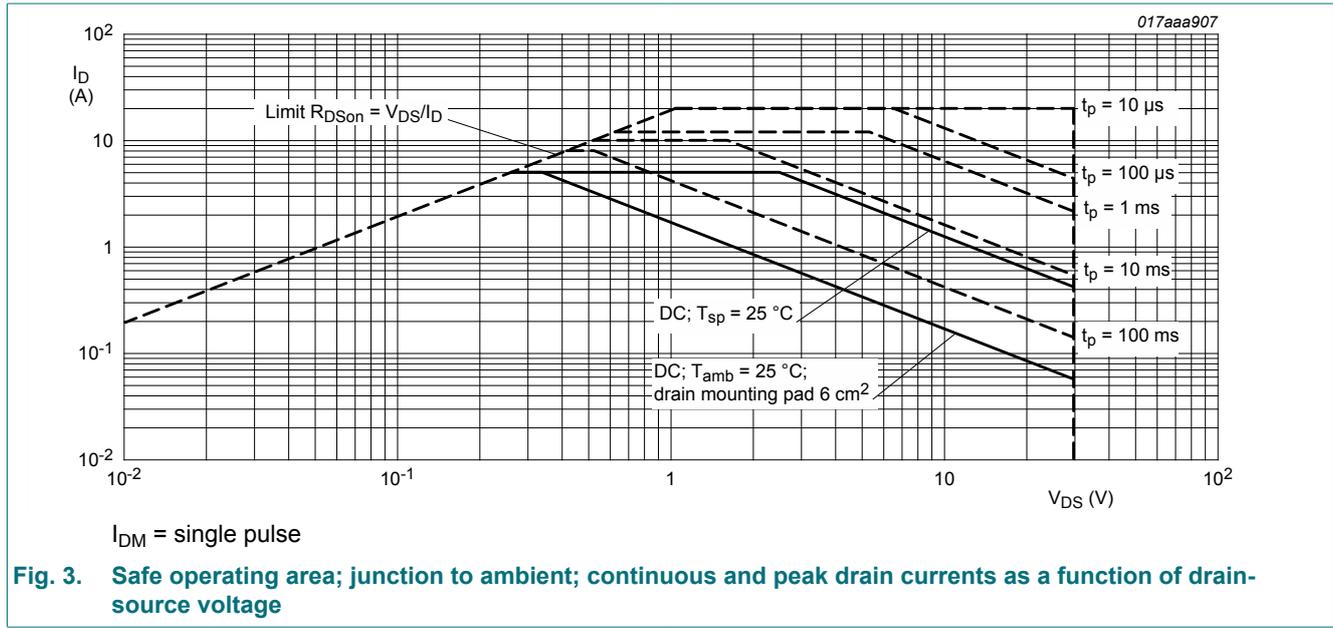
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	5	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	3.2	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	12	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[1]	-	1.7	W
		T _{sp} = 25 °C		-	12.5	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.9	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[2]	-	500	V
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = 0.75 A; DUT in avalanche (unclamped)		-	11.8	mJ

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Measured between all pins.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

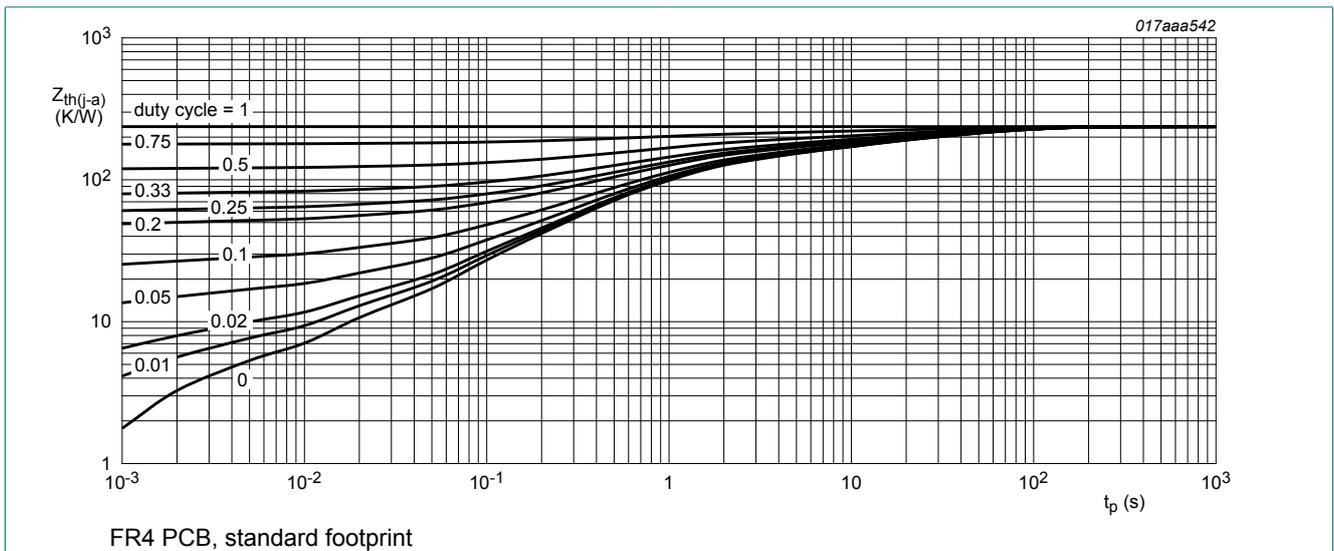


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

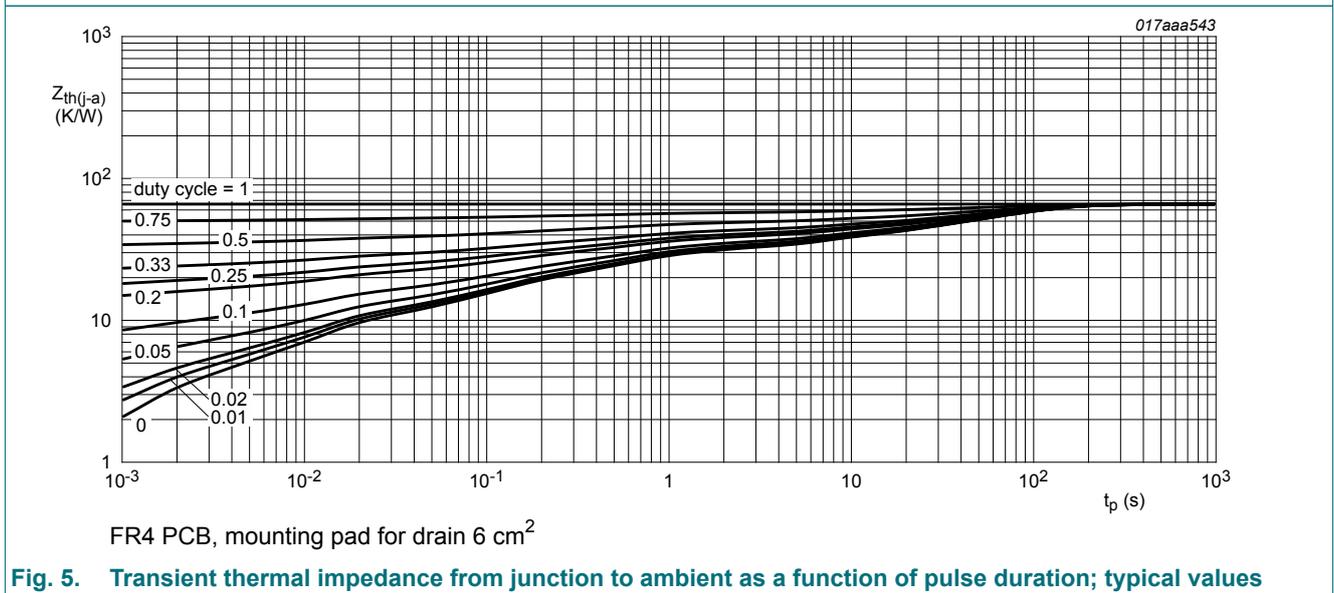


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	0.4	0.65	0.9	V
I_{DSS}	drain leakage current	$V_{DS} = 20 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -8 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-10	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 V$; $I_D = 5 A$; $T_j = 25 \text{ }^\circ C$	-	28	33	m Ω
		$V_{GS} = 4.5 V$; $I_D = 5 A$; $T_j = 150 \text{ }^\circ C$	-	46	54	m Ω
		$V_{GS} = 2.5 V$; $I_D = 3 A$; $T_j = 25 \text{ }^\circ C$	-	32	40	m Ω
		$V_{GS} = 1.8 V$; $I_D = 1.9 A$; $T_j = 25 \text{ }^\circ C$	-	37	50	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 5 A$; $T_j = 25 \text{ }^\circ C$	-	30	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ C$	-	1.8	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V$; $I_D = 5 A$; $V_{GS} = 4.5 V$; $T_j = 25 \text{ }^\circ C$	-	12.4	18.6	nC
Q_{GS}	gate-source charge		-	1.2	-	nC
Q_{GD}	gate-drain charge		-	2.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 15 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	1150	-	pF
C_{oss}	output capacitance		-	110	-	pF
C_{rss}	reverse transfer capacitance		-	85	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V$; $I_D = 5 A$; $V_{GS} = 4.5 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$	-	8	-	ns
t_r	rise time		-	17	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
t_f	fall time		-	32	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.9 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.6	1.2	V
t_{rr}	reverse recovery time	$I_S = 1.9 A$; $di_S/dt = -100 A/\mu s$;	-	9	-	ns
Q_r	recovered charge	$V_{GS} = 0 V$; $V_{DS} = 15 V$; $T_j = 25 \text{ }^\circ C$	-	2	-	nC

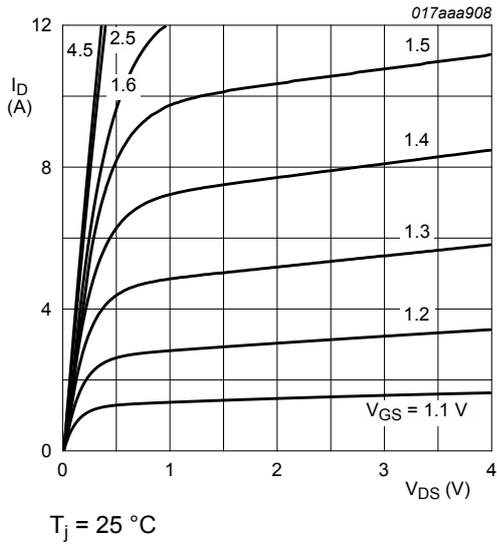


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

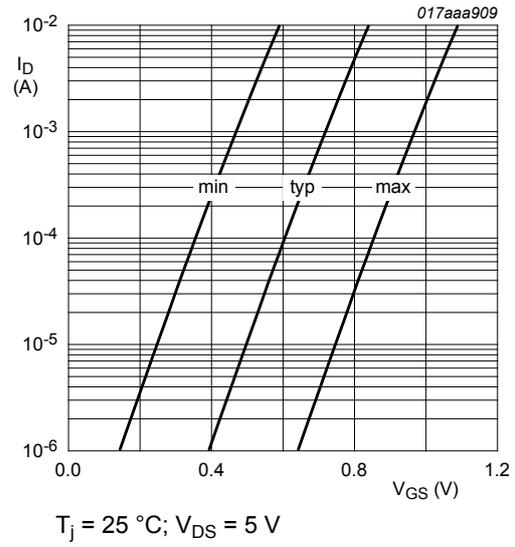


Fig. 7. Subthreshold drain current as a function of gate-source voltage

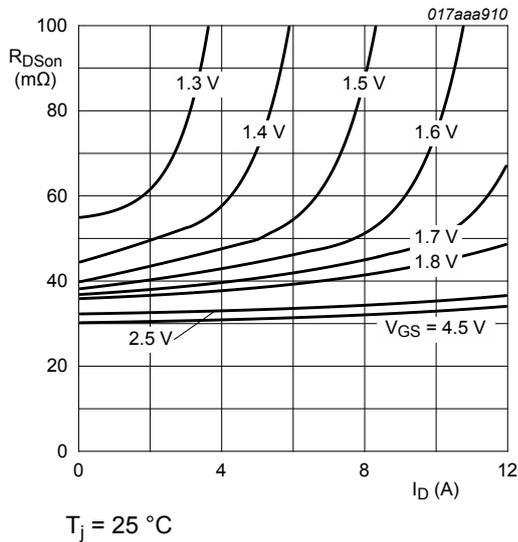


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

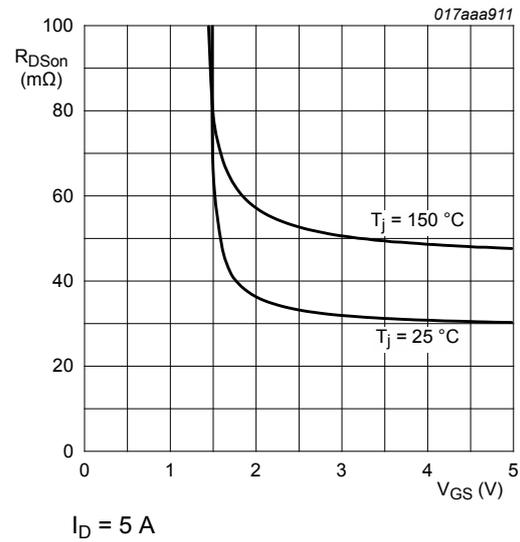
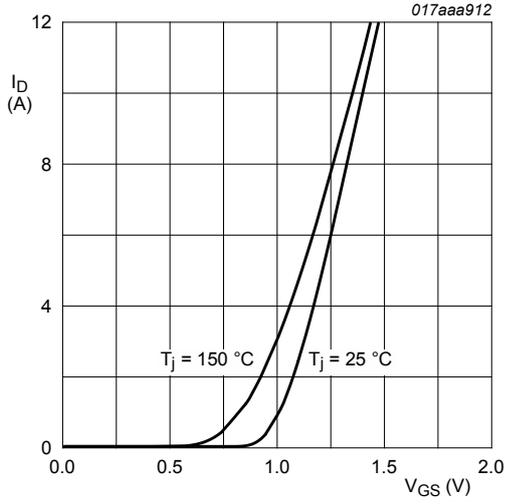
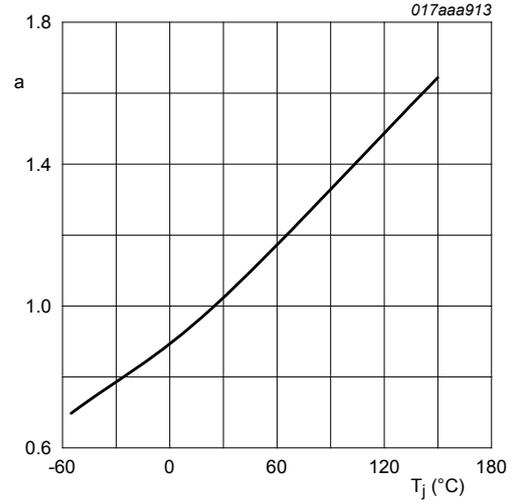


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



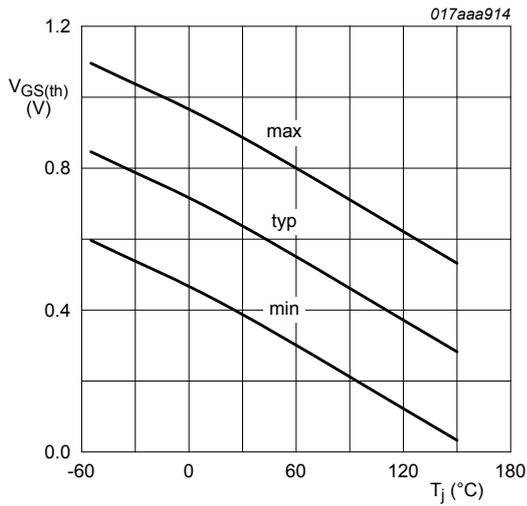
$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



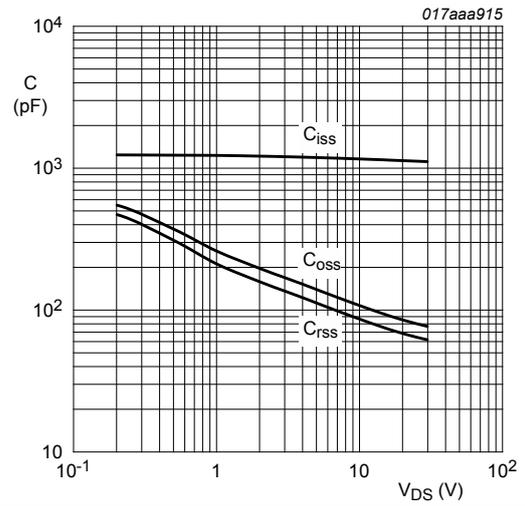
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values



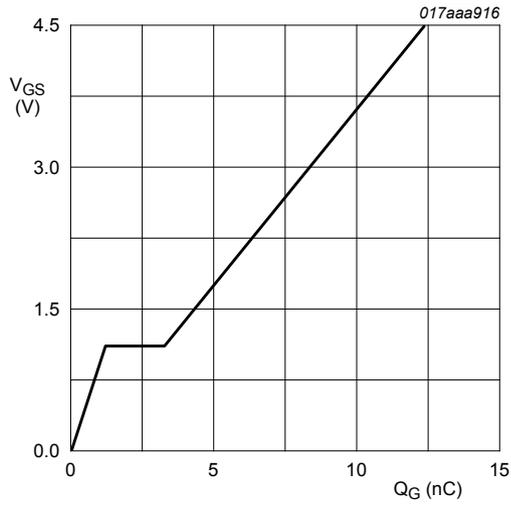
$$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

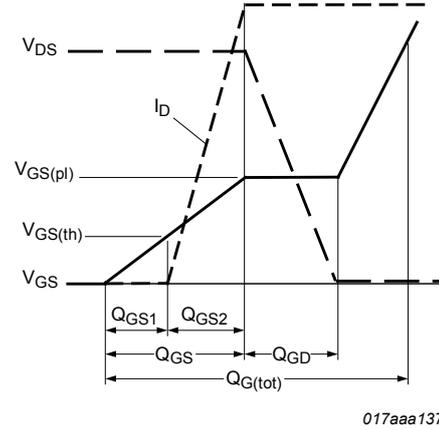
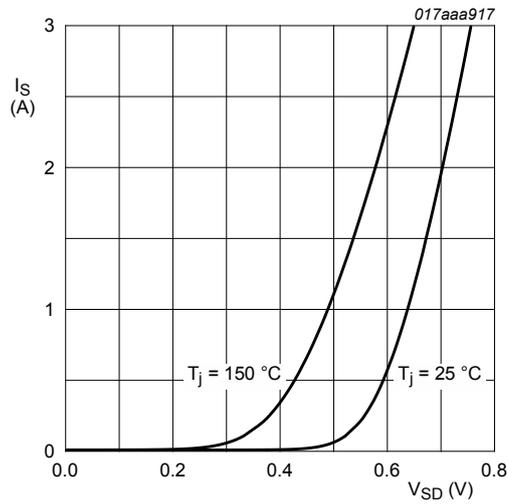


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

13. Soldering

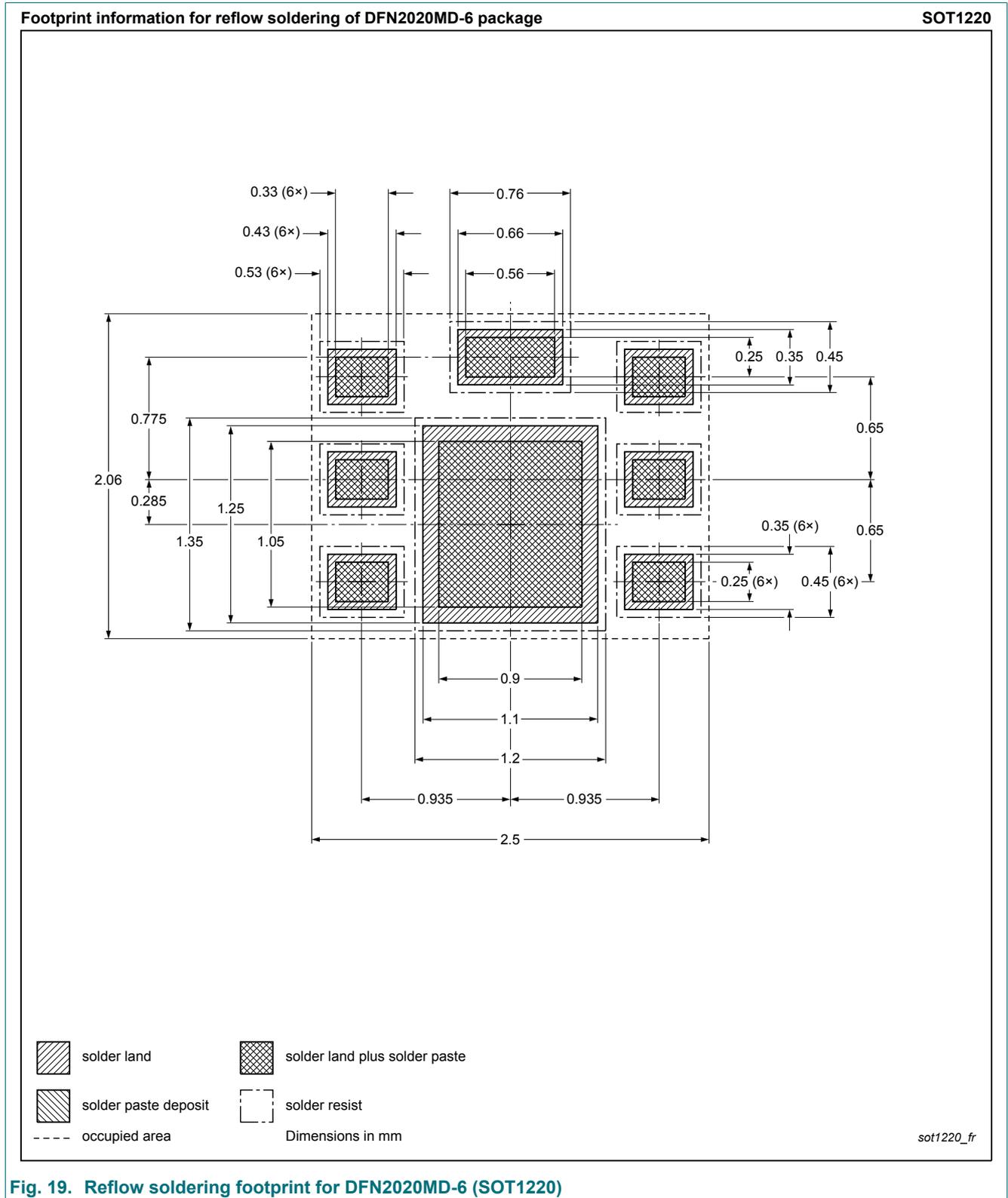


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB29XNEA v.1	20180910	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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