



PSMN0R9-30ULD

N-channel 30 V, 0.87 mΩ, 300 A logic level MOSFET in SOT1023A enhanced package for UL2595, using NextPowerS3 Schottky-Plus Technology

23 May 2018

Product data sheet

1. General description

SOT1023A with improved creepage and clearance to meet UL2595 requirements. 300 Amp logic level gate drive N-channel enhancement mode MOSFET in LPAK56 package. NextPowerS3 portfolio utilising Nexperia's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- Improved creepage and clearance – meets the requirements of UL2595
- 300 A capability
- Avalanche rated, 100% tested at $I_{AS} = 190$ A
- Ultra low Q_G , Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 μ A leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 150 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- Brushed and brushless motor control
- Battery powered appliances where enhanced creepage and clearance is required to meet UL2595
- For non-UL2595 applications please use PSMN0R9-30YLD

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$		-	-	30	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	300	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	227	W
T_j	junction temperature			-55	-	150	°C

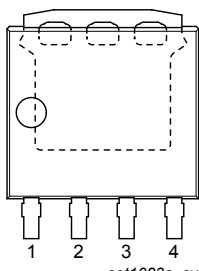
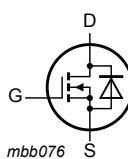
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 10	-	0.79	1.09	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10	-	0.65	0.87	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 15 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13	-	13.5	-	nC
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 15 V; V _{GS} = 10 V; Fig. 12 ; Fig. 13	-	109	-	nC
Source-drain diode						
S	softness factor	I _S = 25 A; di/dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 15 V; Fig. 16	-	0.9	-	

[1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p style="text-align: center;">sot1023a_sv LFAK56-UL2595 (SOT1023A)</p>	 <p style="text-align: center;">mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN0R9-30ULD	LFAK56-UL2595	plastic, single-ended surface-mounted package (LFAK56); 4 leads; 1.27 mm pitch	SOT1023A

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7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN0R9-30ULD	0D93UL

8. Limiting values

Table 5. Limiting values

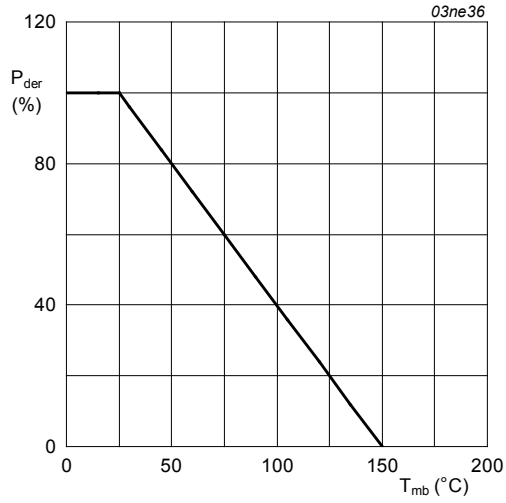
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$		-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	30	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	227	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	300	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	284	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	1592	A
T_{stg}	storage temperature			-55	150	°C
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM		2	-	kV
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	242	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	1800	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 6.1\text{ ms}$	[2]	-	2575	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 30\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	190	A

[1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

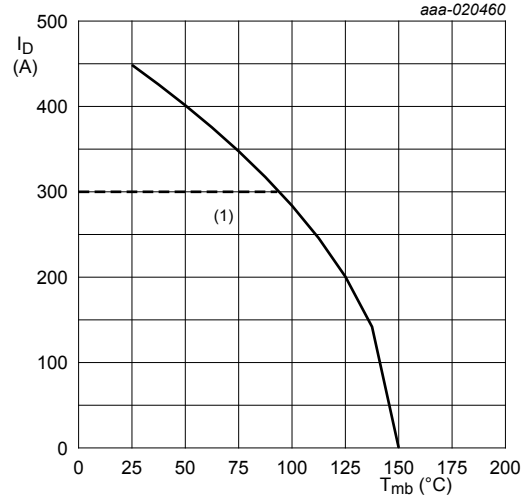
[2] Protected by 100% test

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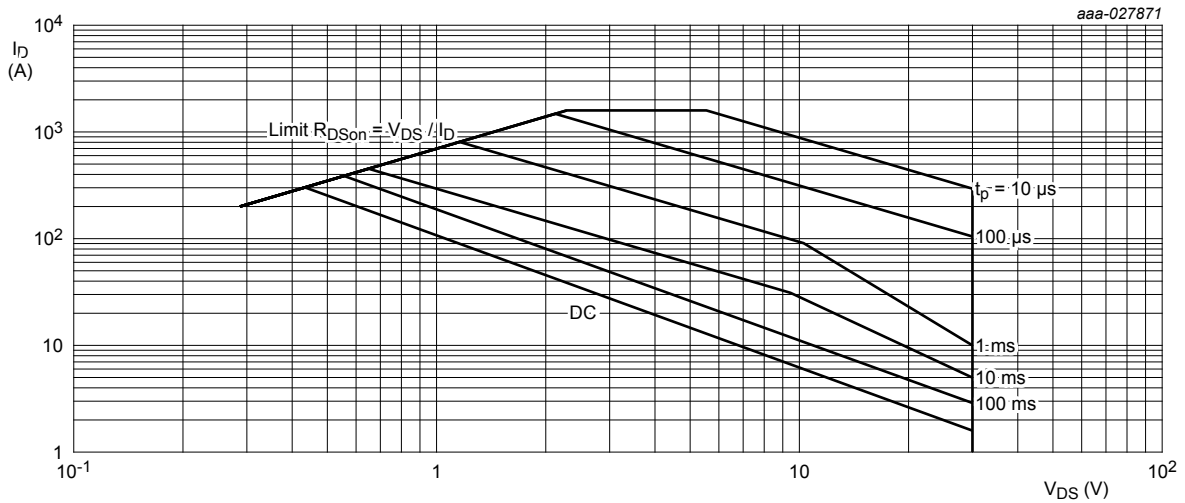
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



(1) 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature
 $V_{GS} \geq 10V$

Fig. 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.45	0.55	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W

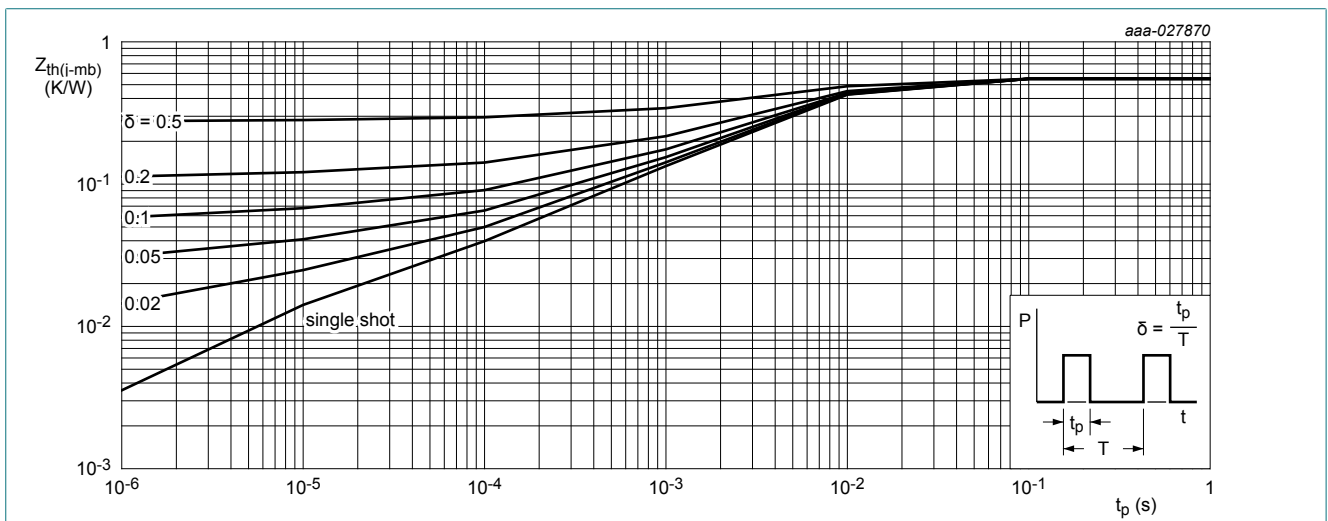


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-005750

aaa-005751

Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 board; 2oz copper

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.5	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-4.5	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	3.7	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; Fig. 10	-	0.79	1.09	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 \text{ }^\circ C$; Fig. 10 ; Fig. 11	-	-	1.8	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; Fig. 10	-	0.65	0.87	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150 \text{ }^\circ C$; Fig. 10 ; Fig. 11	-	-	1.44	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.4	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V$; Fig. 12 ; Fig. 13	-	109	-	nC
		$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V$; Fig. 12 ; Fig. 13	-	51	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 0 V$	-	99	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V$; Fig. 12 ; Fig. 13	-	15.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	10.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.8	-	nC
Q_{GD}	gate-drain charge		-	13.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 15 V$; Fig. 12 ; Fig. 13	-	2.4	-	V
C_{iss}	input capacitance	$V_{DS} = 15 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 14	-	7668	-	pF
C_{oss}	output capacitance		-	2914	-	pF
C_{rss}	reverse transfer capacitance		-	445	-	pF

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 0.6\ \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\ \Omega$	-	38.1	-	ns	
t_r	rise time		-	49.8	-	ns	
$t_{d(off)}$	turn-off delay time		-	63	-	ns	
t_f	fall time		-	42.6	-	ns	
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	83.11	-	nC	
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 15}$	-	0.76	1.2	V	
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; \text{Fig. 16}$	-	52	-	ns	
Q_r	recovered charge		[1]	-	67	-	nC
t_a	reverse recovery rise time		-	-	27.4	-	ns
t_b	reverse recovery fall time		-	-	24.7	-	ns
S	softness factor		-	-	0.9	-	

[1] includes capacitive recovery

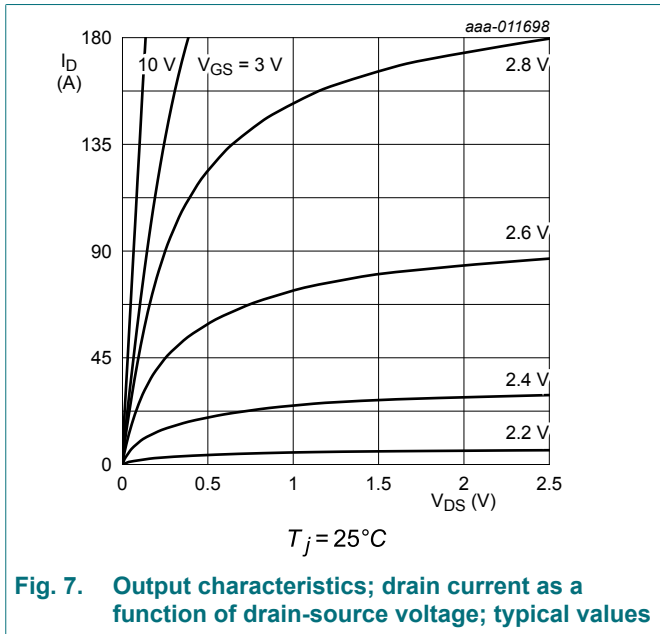


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

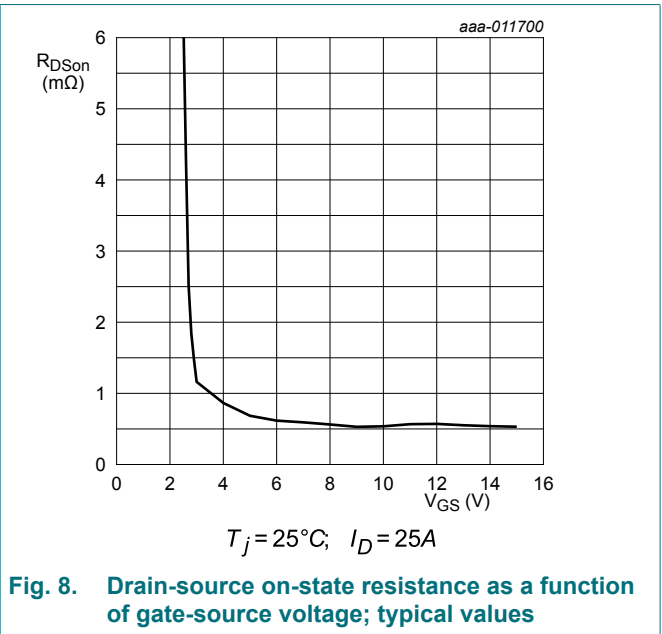


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

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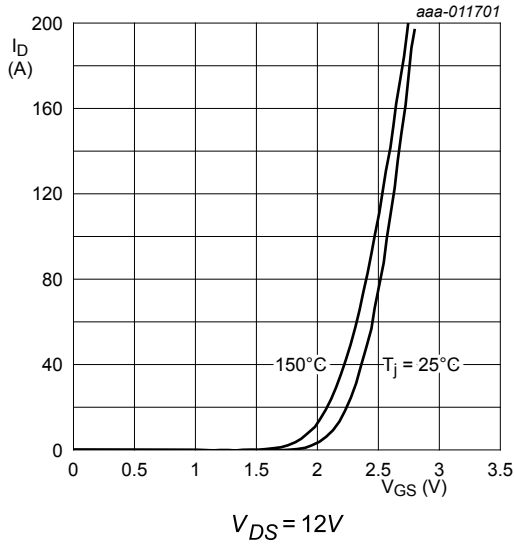


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

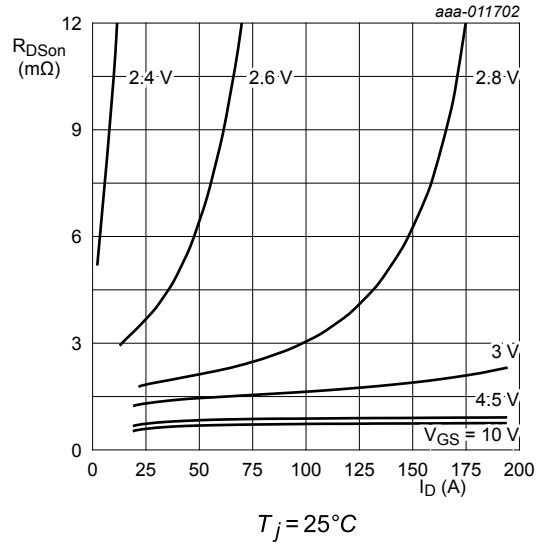
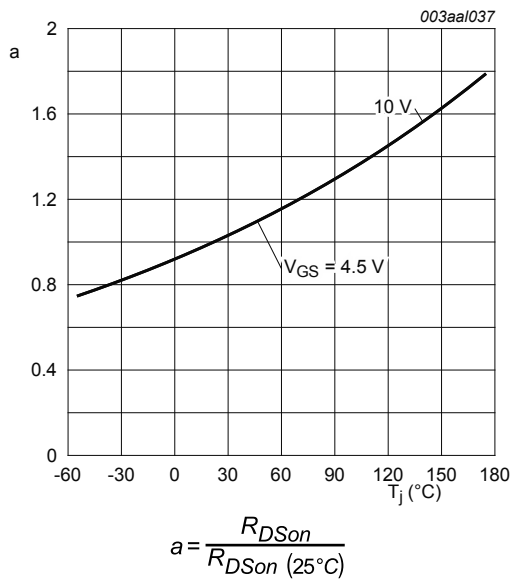


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

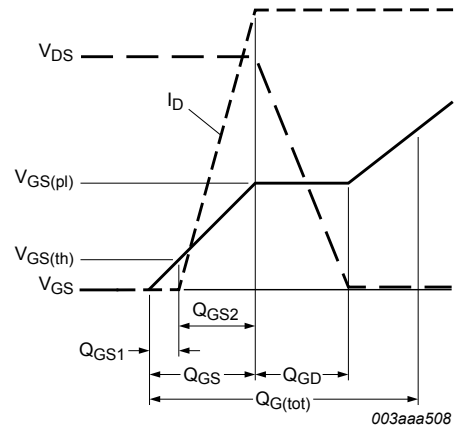


Fig. 12. Gate charge waveform definitions

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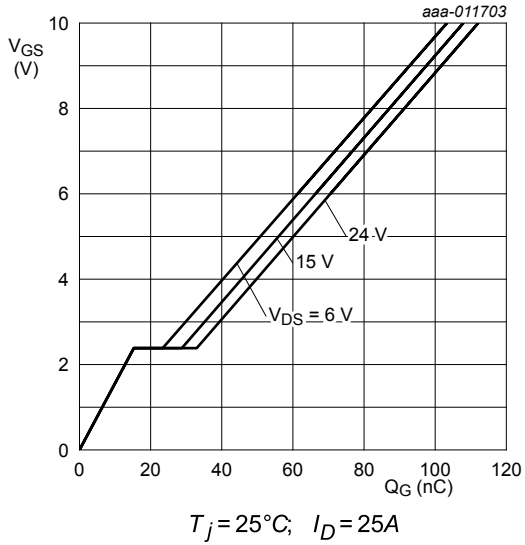


Fig. 13. Gate-source voltage as a function of gate charge; typical values

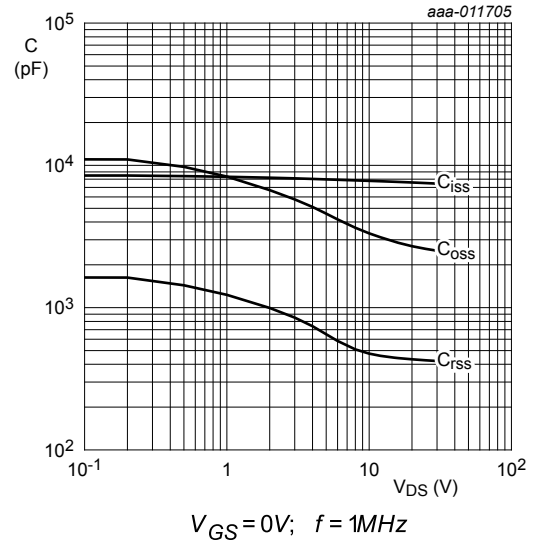


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

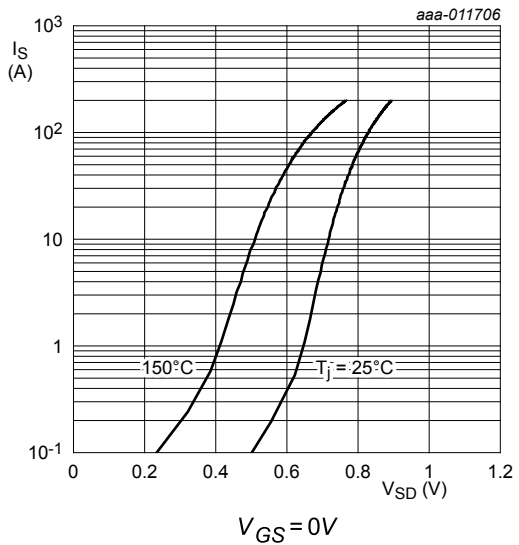


Fig. 15. Source current as a function of source-drain voltage; typical values

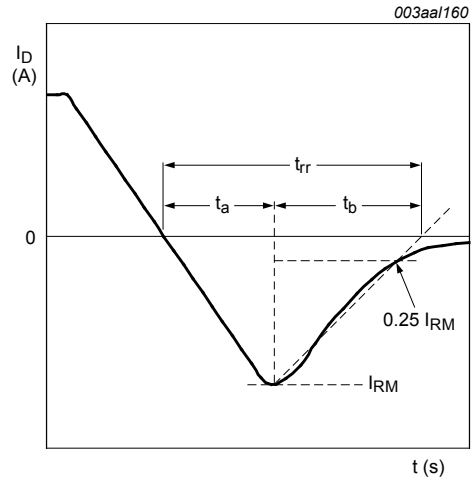


Fig. 16. Reverse recovery timing definition

11. Package outline

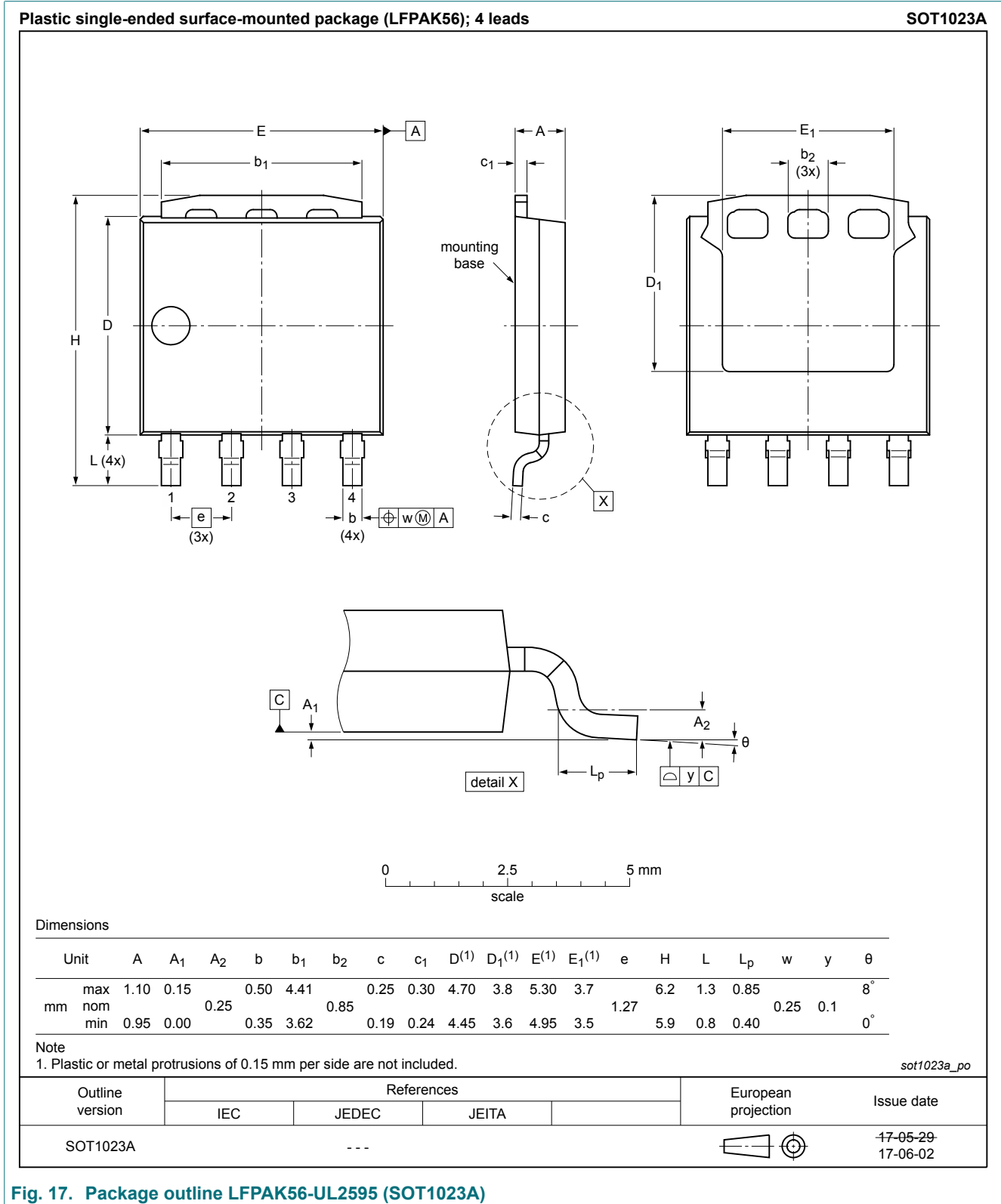


Fig. 17. Package outline LPAK56-UL2595 (SOT1023A)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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