



PSMN6R9-100YSF

NextPower 100 V, 7 mΩ N-channel MOSFET in LPAK56 package

8 December 2017

Product data sheet

1. General description

NextPower 100 V standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial & consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Qualified to 175 °C
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LPAK56 package
- Wave-solderable LPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- LED lighting
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

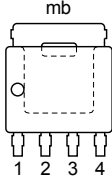
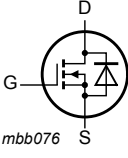
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	90	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	238	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	5.6	7	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 12 ; Fig. 13	-	10.3	-	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; Fig. 16	-	52.4	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R9-100YSF	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN6R9-100YSF	6F9S10

8. Limiting values

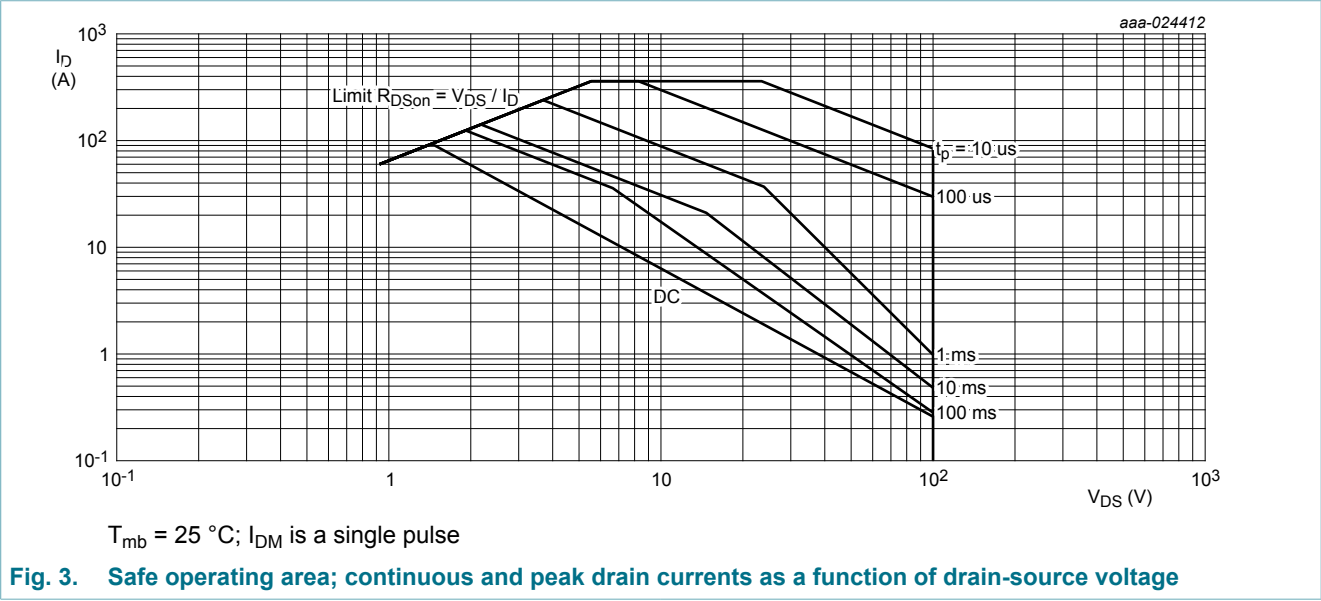
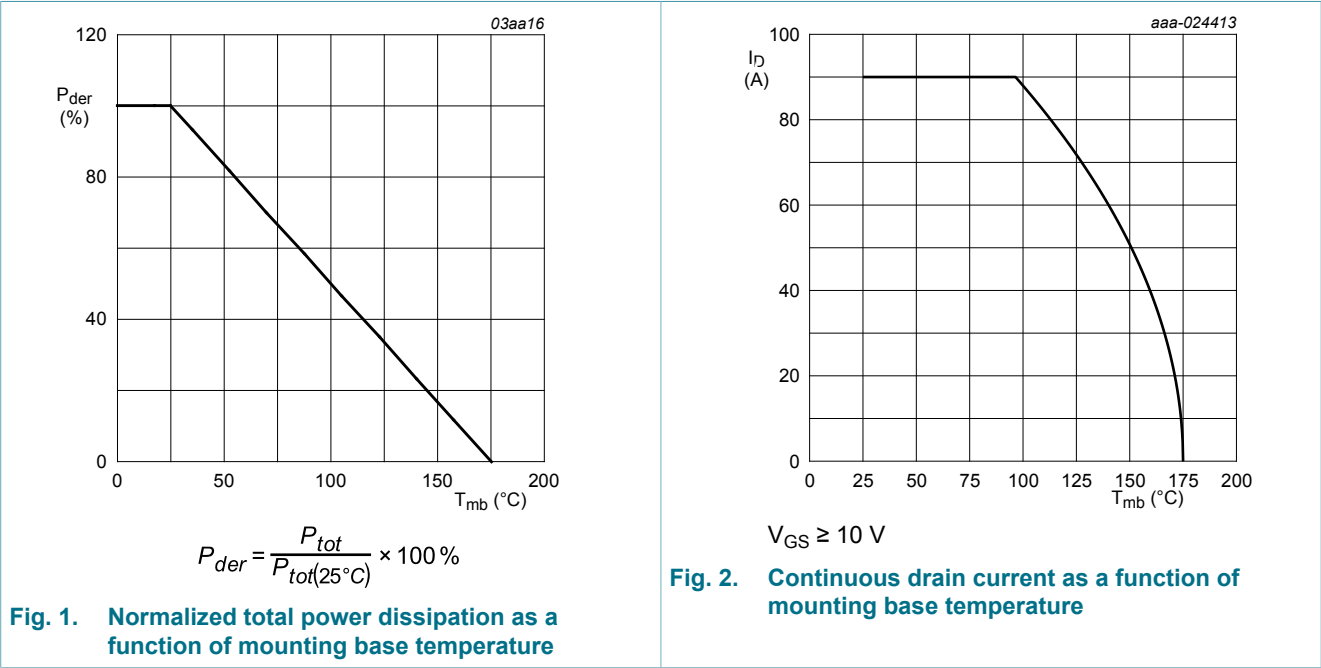
Table 5. Limiting values

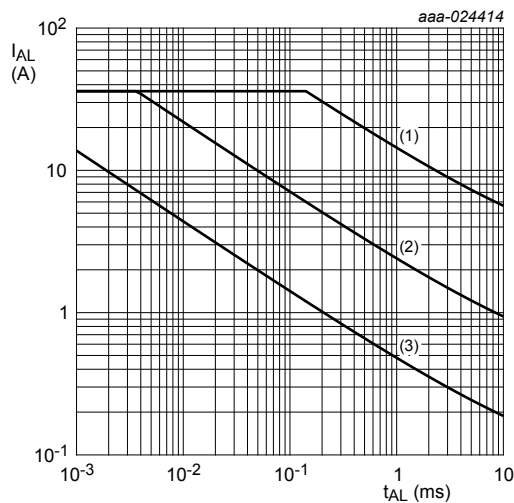
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	238	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	90	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	88	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	360	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	90	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	360	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 36 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 4; Unclamped	[1]	-	321	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[1]	-	36	A

[1] Protected by 100% test





(1) $T_{j\text{ (init)}} = 25\text{ }^{\circ}\text{C}$; (2) $T_{j\text{ (init)}} = 150\text{ }^{\circ}\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.56	0.63	K/W

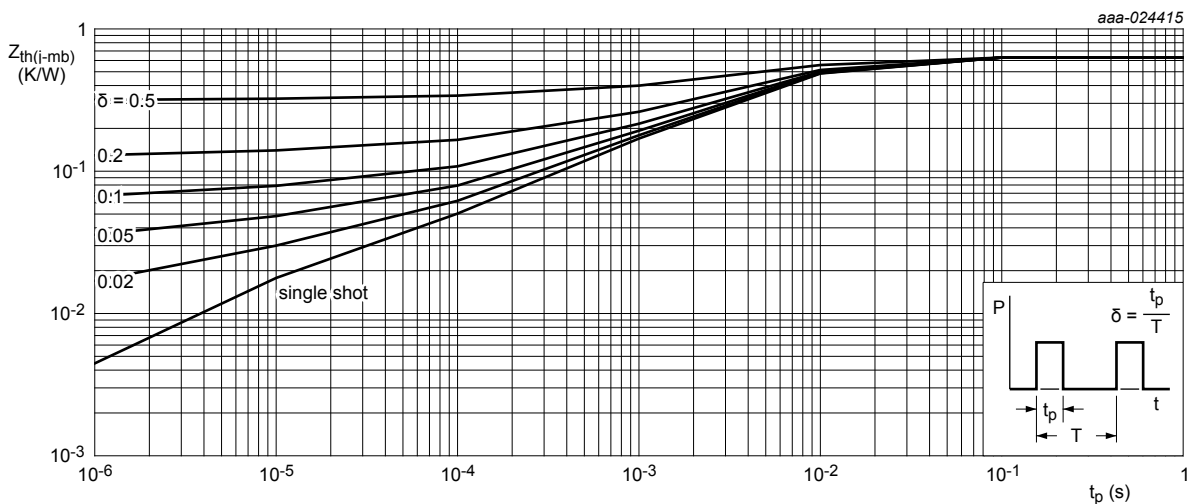


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	100	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = -55 ^\circ C$	-	3.7	-	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = 175 ^\circ C$	-	2	-	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_j = 25 ^\circ C$; Fig. 9	2	3.3	4	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_j \leq 175 ^\circ C$	-	-8.4	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	0.02	5	μA
		$V_{DS} = 100 V$; $V_{GS} = 0 V$; $T_j = 125 ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	5	100	nA
		$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	5	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 25 ^\circ C$; Fig. 10	-	5.6	7	mΩ
		$V_{GS} = 7 V$; $I_D = 25 A$; $T_j = 25 ^\circ C$; Fig. 10	-	6.6	10.2	mΩ
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 100 ^\circ C$; Fig. 11	-	8.9	10.9	mΩ
		$V_{GS} = 10 V$; $I_D = 25 A$; $T_j = 175 ^\circ C$; Fig. 11	-	12.5	15.4	mΩ
R_G	gate resistance	$f = 1 MHz$	-	0.9	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A$; $V_{DS} = 50 V$; $V_{GS} = 10 V$; Fig. 12 ; Fig. 13	-	50.3	-	nC
		$I_D = 0 A$; $V_{DS} = 0 V$; $V_{GS} = 10 V$	-	20.9	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A$; $V_{DS} = 50 V$; $V_{GS} = 10 V$; Fig. 12 ; Fig. 13	-	17.1	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	9.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	7.2	-	nC
Q_{GD}	gate-drain charge		-	10.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A$; $V_{DS} = 50 V$; Fig. 12 ; Fig. 13	-	5.1	-	V
C_{iss}	input capacitance	$V_{DS} = 50 V$; $V_{GS} = 0 V$; $f = 1 MHz$; $T_j = 25 ^\circ C$; Fig. 14	-	3570	-	pF
C_{oss}	output capacitance		-	722	-	pF
C_{rss}	reverse transfer capacitance		-	19	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 V$; $R_L = 2 \Omega$; $V_{GS} = 10 V$; $R_{G(ext)} = 5 \Omega$; $T_j = 25 ^\circ C$	-	14.8	-	ns
t_r	rise time		-	14.2	-	ns

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t _{d(off)}	turn-off delay time			-	27.6	-	ns
t _f	fall time			-	16	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 15		-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; Fig. 16		-	45.4	-	ns
Q _r	recovered charge			-	52.4	-	nC

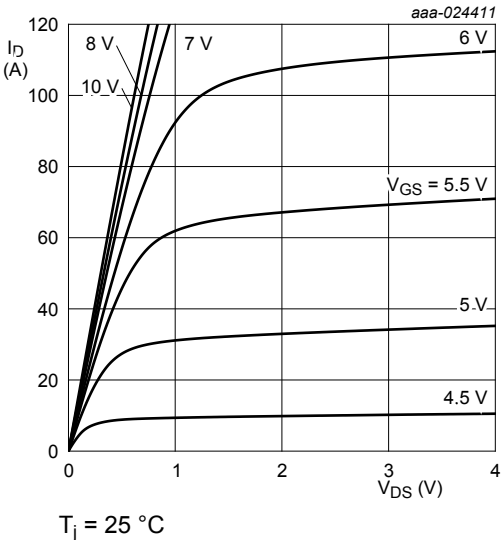


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

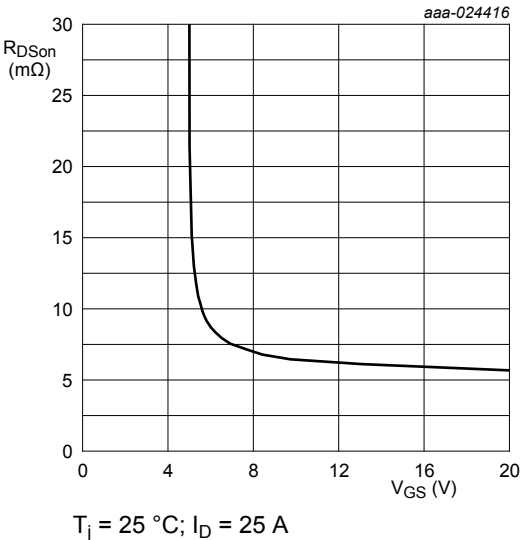


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

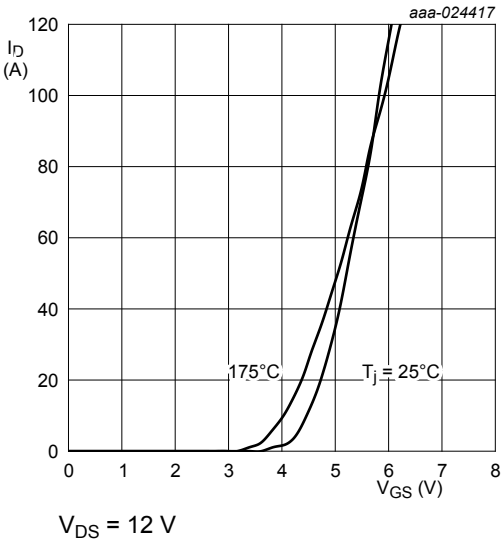


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

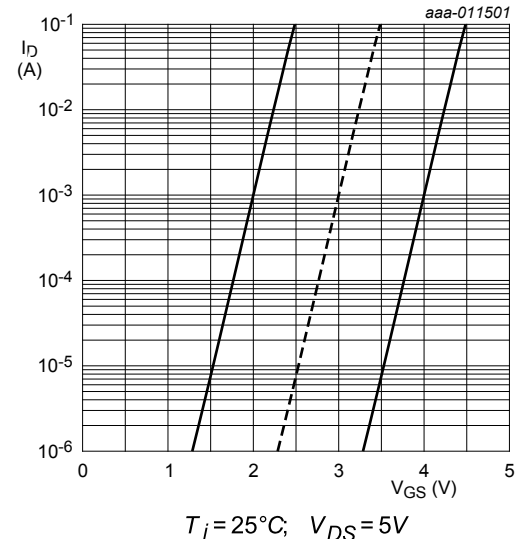


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

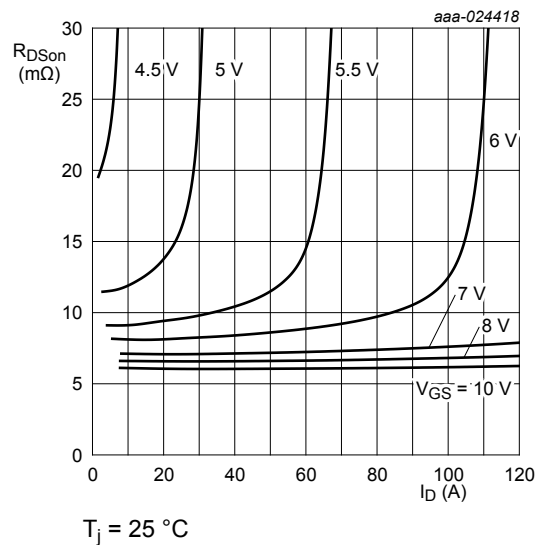


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

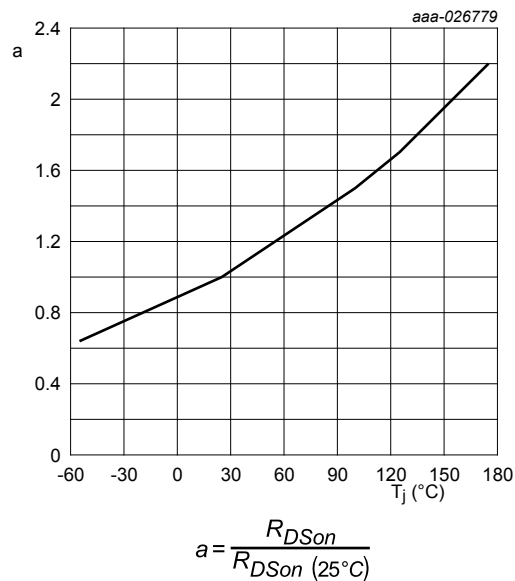


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

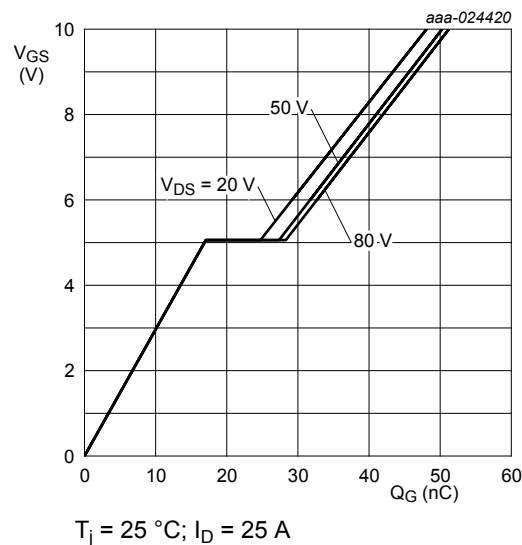


Fig. 12. Gate-source voltage as a function of gate charge; typical values

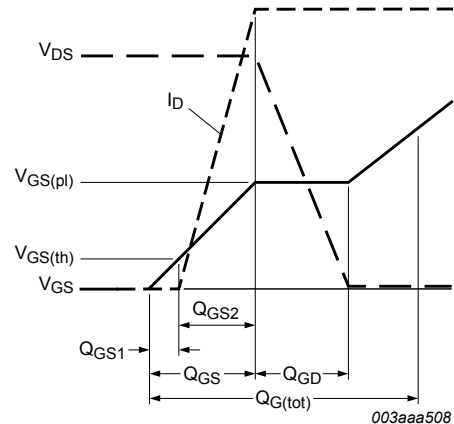


Fig. 13. Gate charge waveform definitions

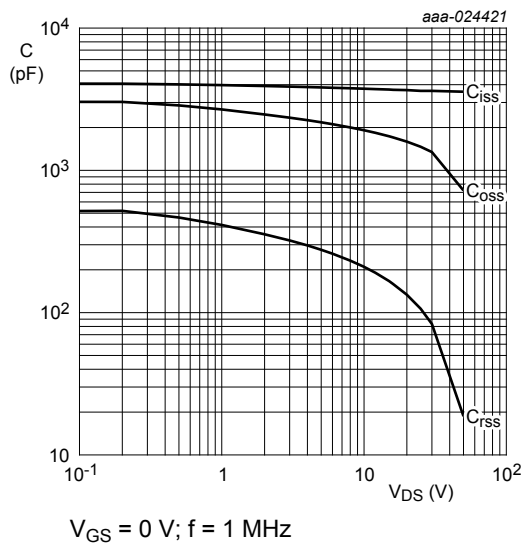


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

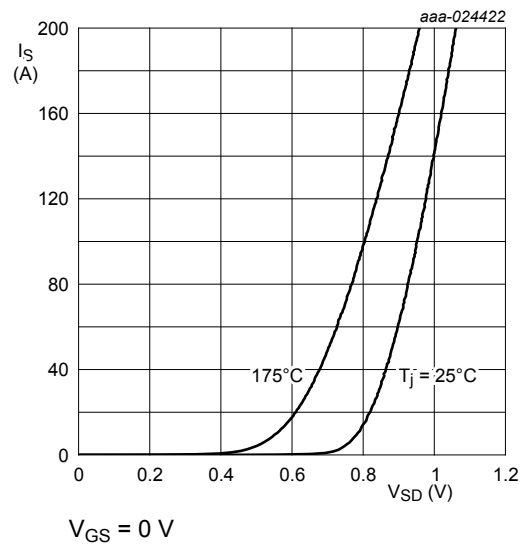


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

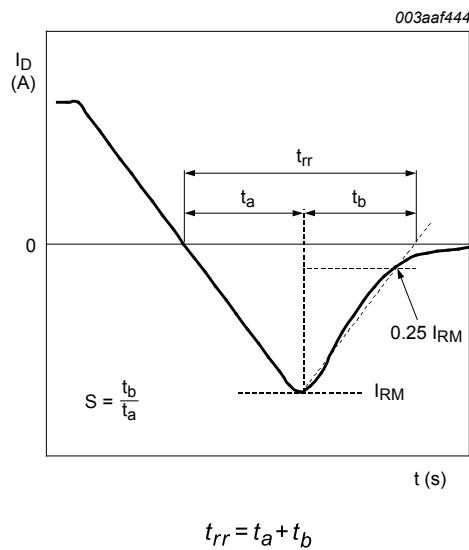


Fig. 16. Reverse recovery waveform definitions

11. Package outline

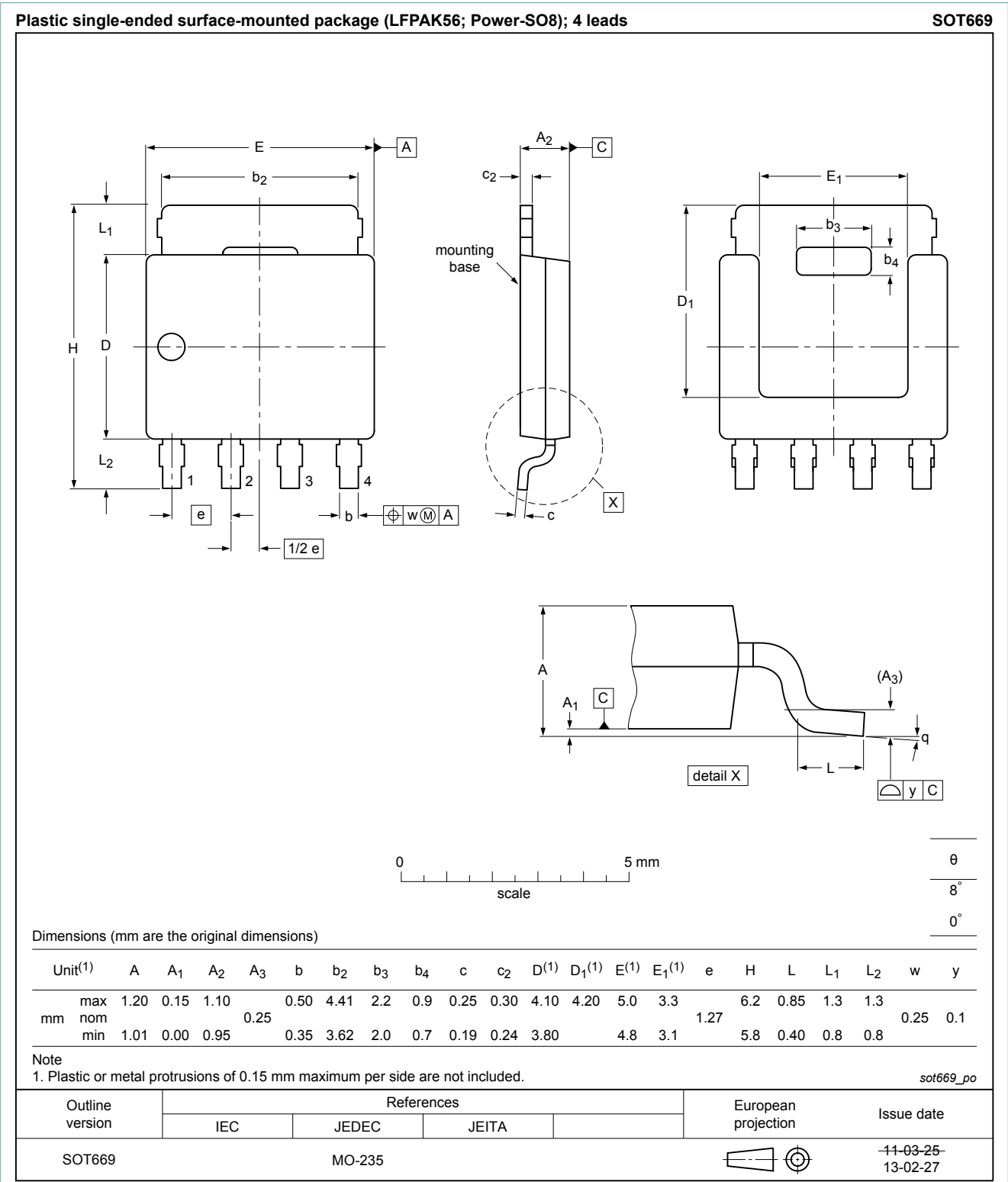


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

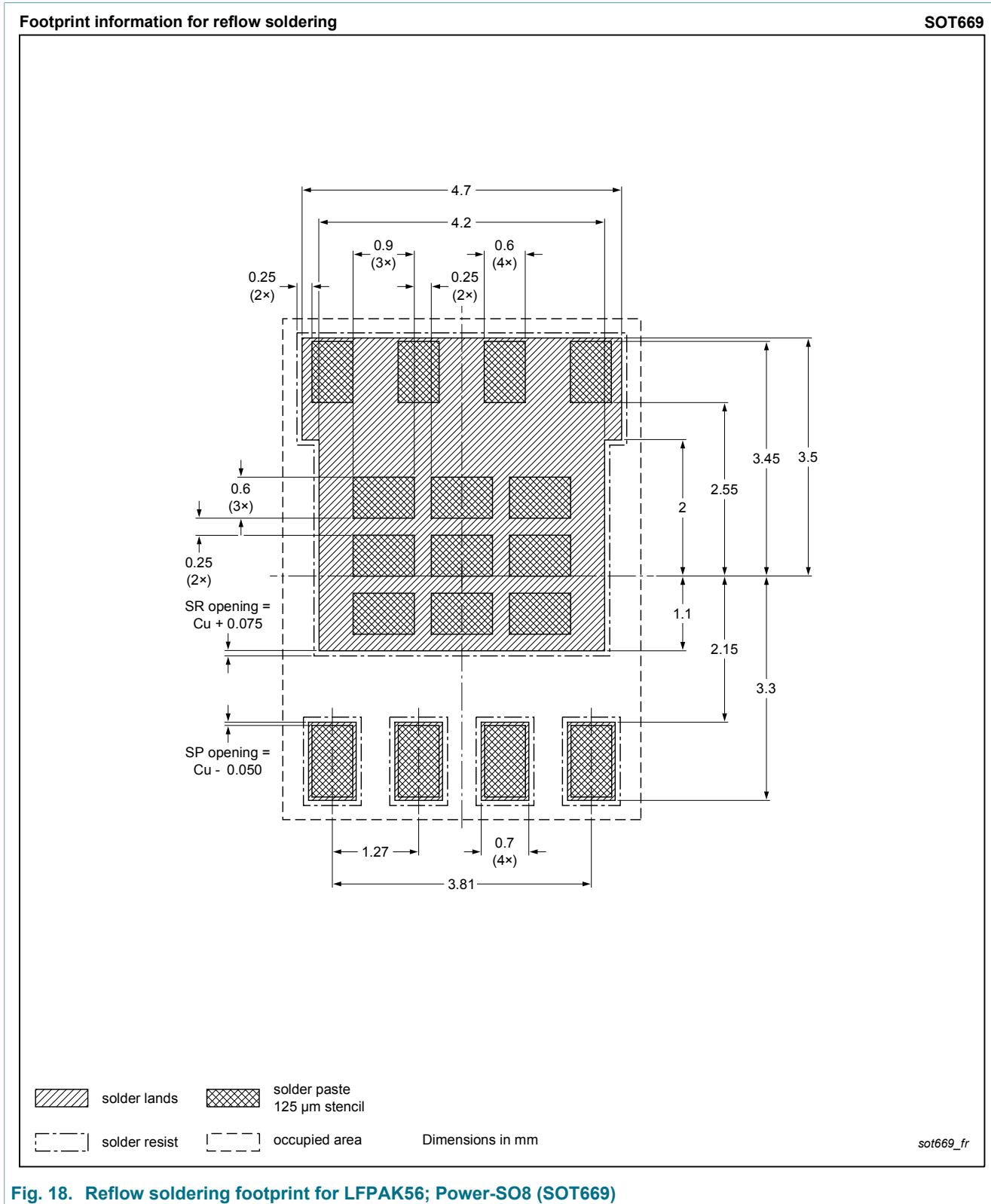


Fig. 18. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LPAK56 package

SOT669

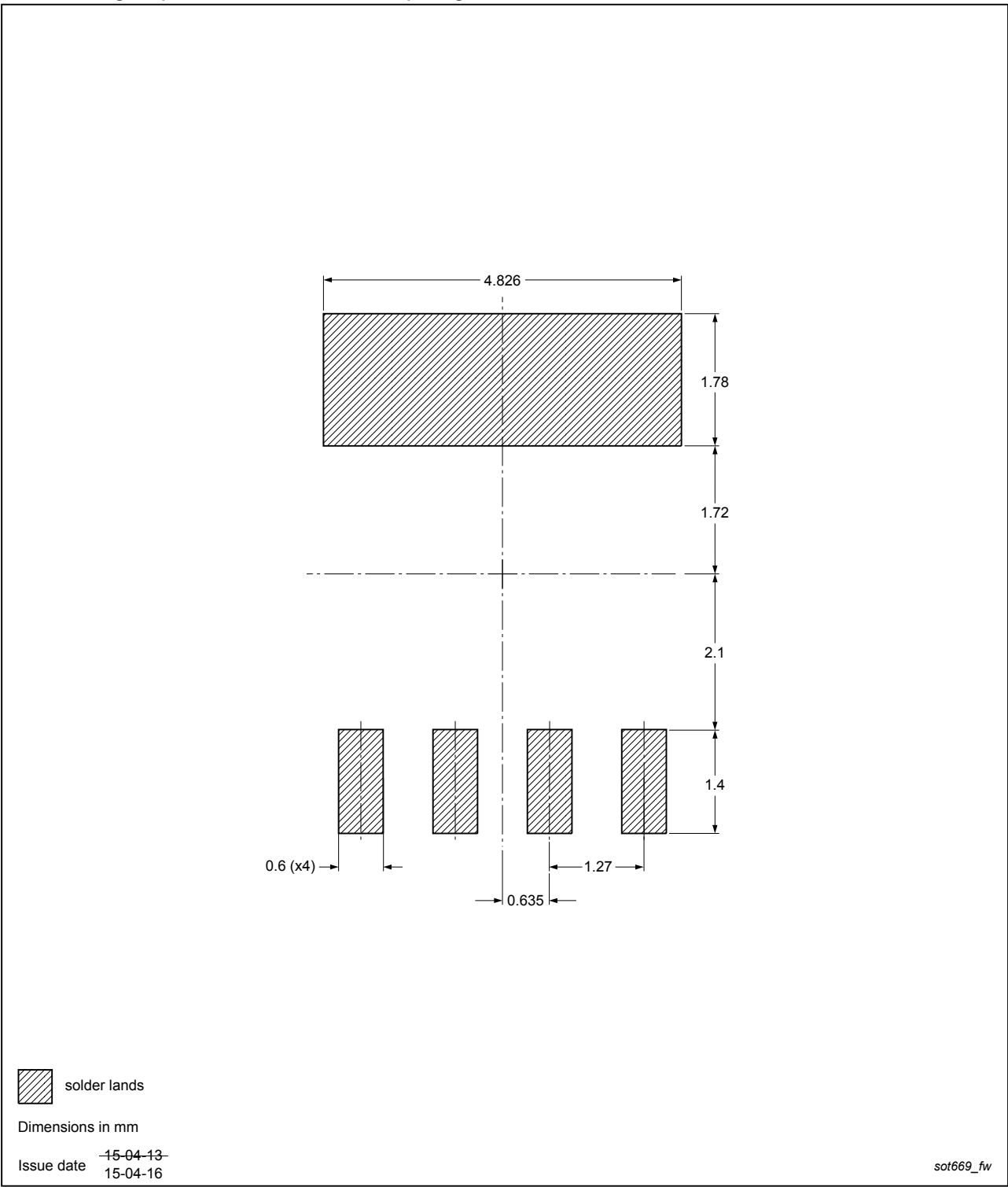


Fig. 19. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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