



PSMN8R5-40MLD

N-channel 40 V, 8.5 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

10 February 2020

Product data sheet

1. General description

60 A, logic level N-channel enhancement mode MOSFET in 175 °C LPAK33 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high efficiency applications at high switching frequencies.

2. Features and benefits

- Avalanche rated, 100% tested
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{RR} , Q_G and Q_{GD} for high system efficiency, especially at high switching frequencies
- Low spiking and ringing for low EMI designs
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Brushless DC motor drive
- LED lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	60	A
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 15 A; T _j = 25 °C; Fig. 10		-	7.2	8.5	mΩ
		V _{GS} = 4.5 V; I _D = 15 A; T _j = 25 °C; Fig. 10		-	9	11	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 15 A; V _{DS} = 20 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		0.6	2.1	4.2	nC

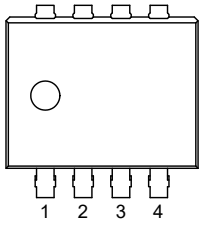
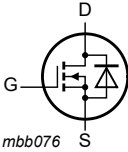
N-channel 40 V, 8.5 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	$I_D = 15\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 12 ; Fig. 13	12	19	27	nC

[1] 60A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK33 (SOT1210)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

6. Marking

Table 3. Marking codes

Type number	Marking code
PSMN8R5-40MLD	8D5L40

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed	-	45	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	59	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	60	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	42	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	239	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	59	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	239	A

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Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 25 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 80 μs	[2]	-	46	mJ
		I _D = 15 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 180 μs	[2]	-	70	mJ

- [1] 60A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Protected by 100% test

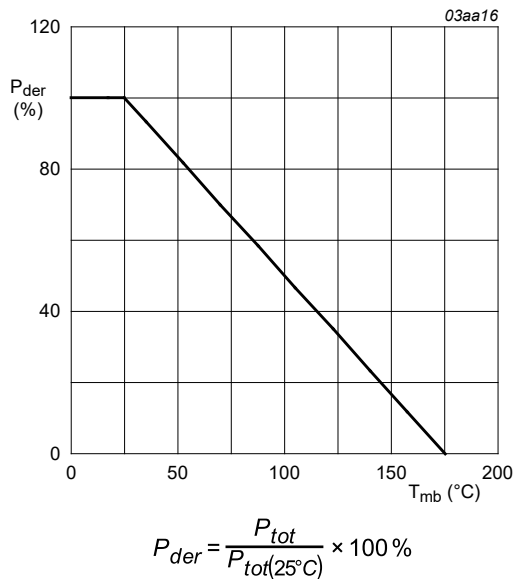
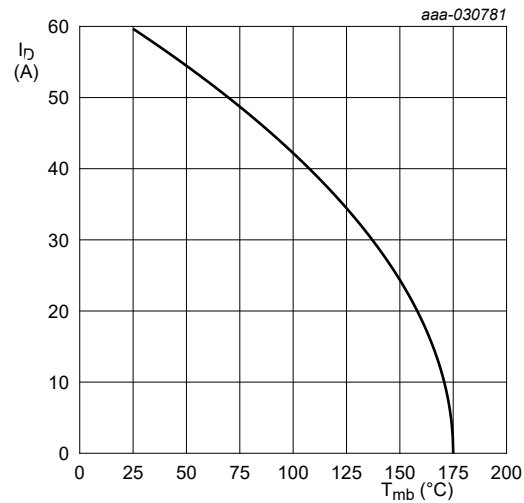


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

(1) 60A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

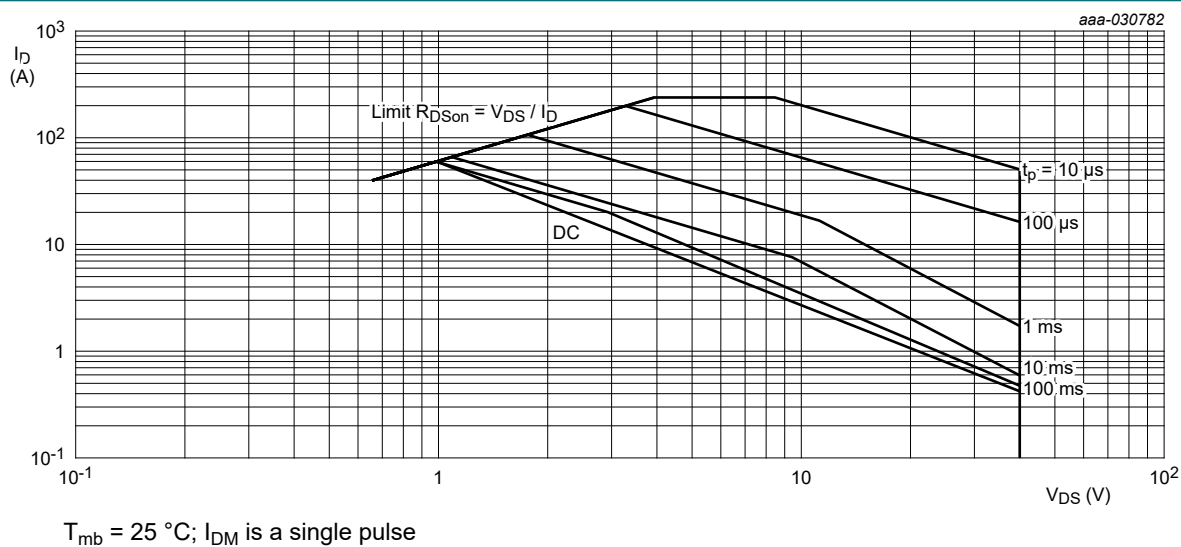


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	2.33	2.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	130	-	K/W

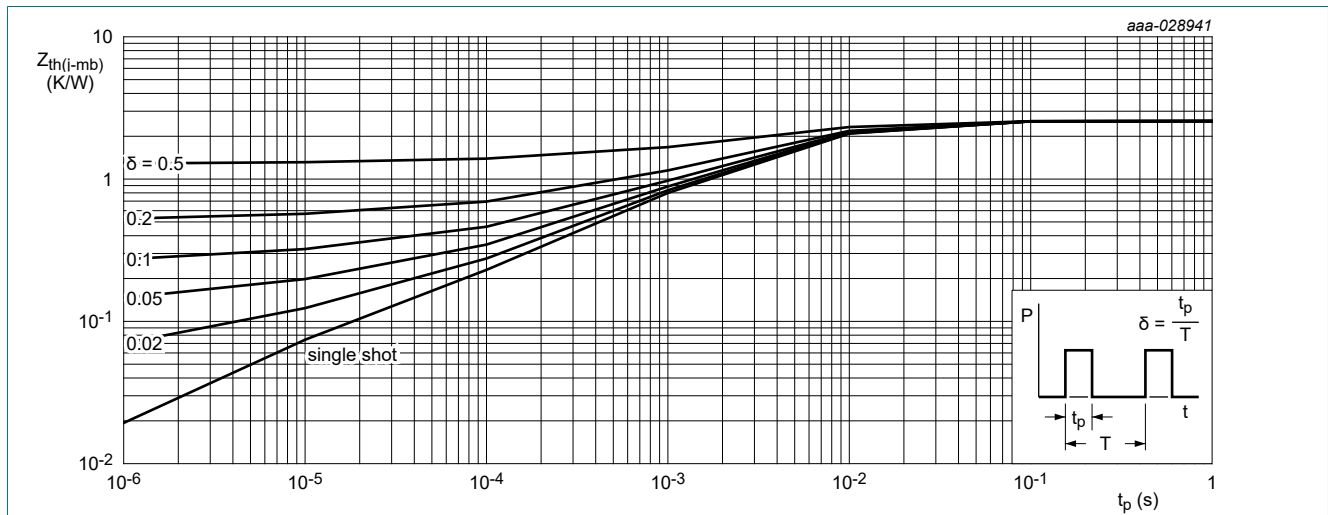


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

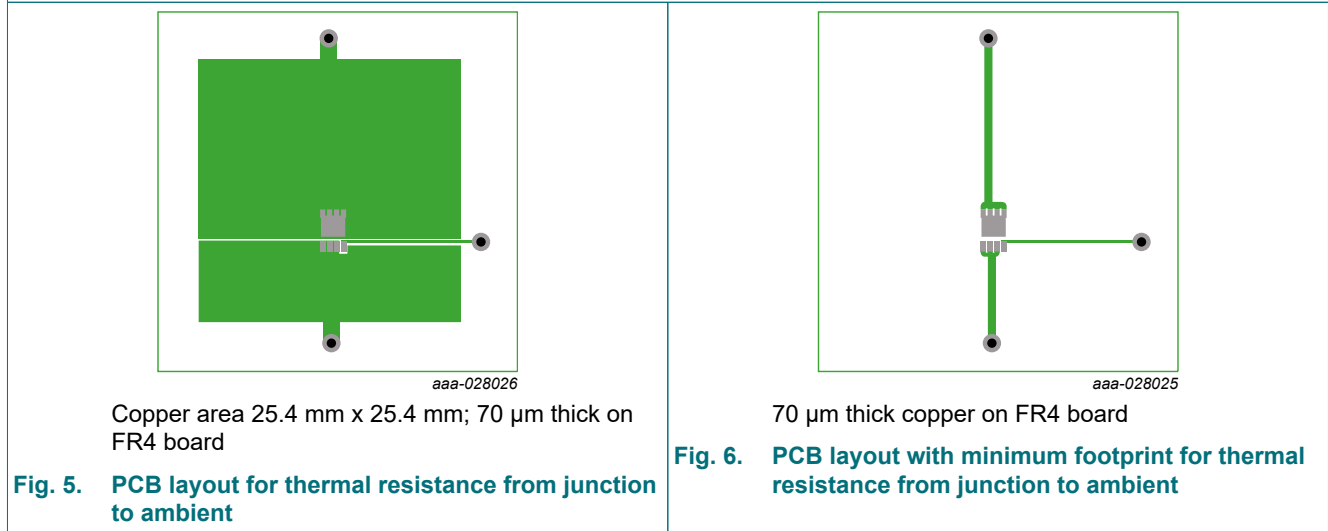


Fig. 5. PCB layout for thermal resistance from junction to ambient

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	40	-	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = -55 ^\circ C$	36	-	-	V

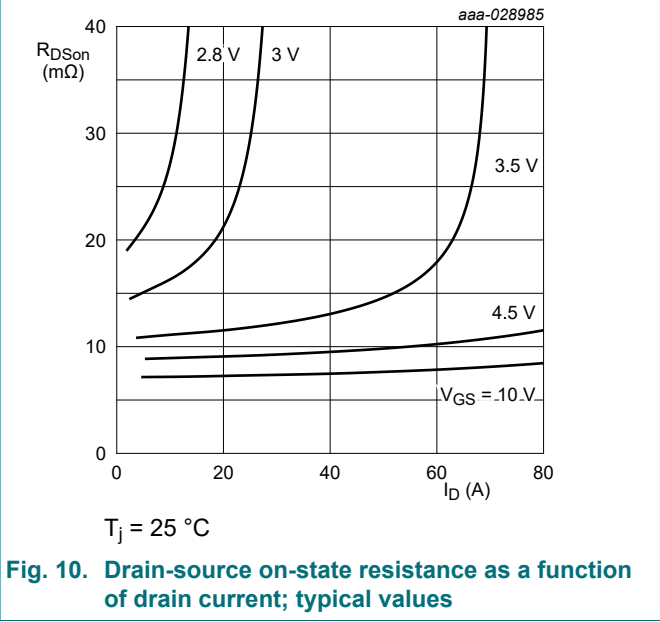
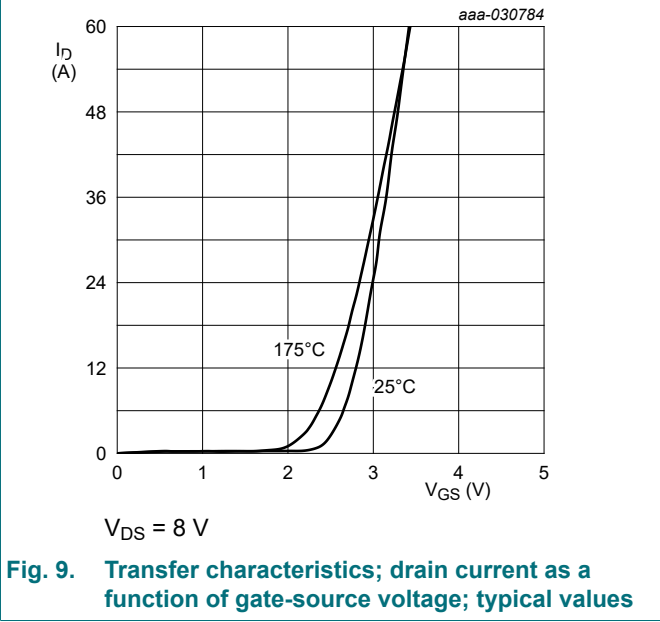
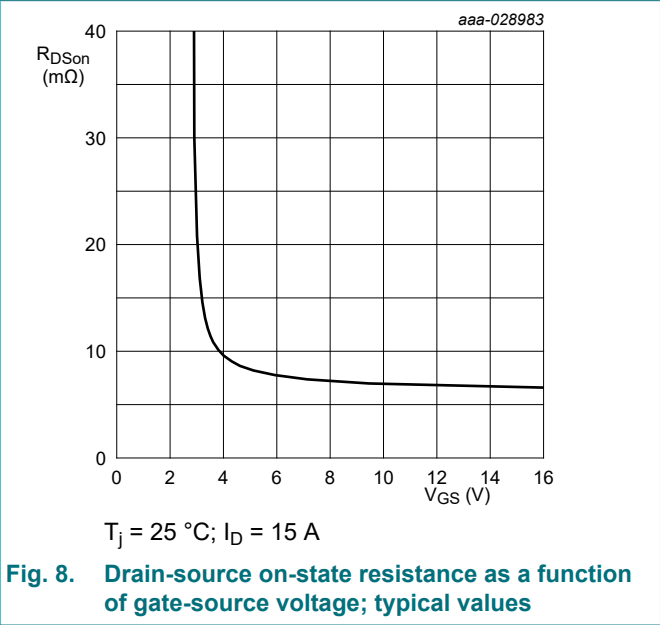
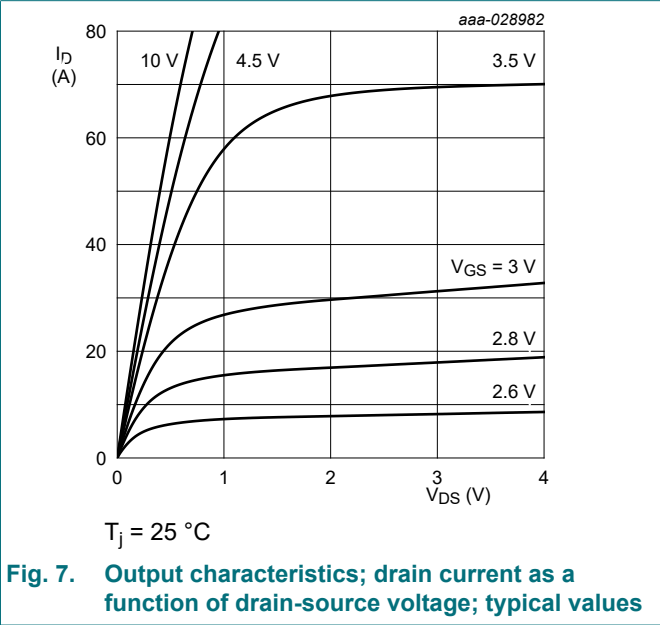
N-channel 40 V, 8.5 mΩ, logic level MOSFET in LPAK33 using NextPower-S3 technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	1.45	1.77	2.15	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	-4.2	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 32 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$	-	0.3	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -16 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 10	-	7.2	8.5	mΩ
		$V_{GS} = 10 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 175 \text{ }^\circ\text{C}$; Fig. 11	-	-	16.5	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 10	-	9	11	mΩ
		$V_{GS} = 4.5 \text{ V}$; $I_D = 15 \text{ A}$; $T_j = 175 \text{ }^\circ\text{C}$; Fig. 11	-	-	21.4	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$	0.3	0.8	2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}$; $V_{DS} = 20 \text{ V}$; $V_{GS} = 10 \text{ V}$; Fig. 12 ; Fig. 13	12	19	27	nC
		$I_D = 15 \text{ A}$; $V_{DS} = 20 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 12 ; Fig. 13	6	9	13	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 10 \text{ V}$	-	10	-	nC
Q_{GS}	gate-source charge	$I_D = 15 \text{ A}$; $V_{DS} = 20 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; Fig. 12 ; Fig. 13	2.1	3.6	5.4	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		1.2	2.1	3.2	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		0.9	1.5	2.3	nC
Q_{GD}	gate-drain charge		0.6	2.1	4.2	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15 \text{ A}$; $V_{DS} = 20 \text{ V}$; Fig. 12 ; Fig. 13	-	2.8	-	V
C_{iss}	input capacitance	$V_{DS} = 20 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 14	842	1296	1814	pF
C_{oss}	output capacitance		249	383	536	pF
C_{rss}	reverse transfer capacitance		15	49	108	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 \text{ V}$; $R_L = 1.2 \text{ } \Omega$; $V_{GS} = 4.5 \text{ V}$; $R_{G(ext)} = 5 \text{ } \Omega$	-	9.5	-	ns
t_r	rise time		-	9.4	-	ns
$t_{d(off)}$	turn-off delay time		-	11	-	ns
t_f	fall time		-	5.6	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}$; $V_{DS} = 20 \text{ V}$; $f = 1 \text{ MHz}$; $T_j = 25 \text{ }^\circ\text{C}$	-	11.4	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 15 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 15	-	0.85	1	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 15\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; Fig. 16		-	22	-	ns
Q_r	recovered charge		[1]	-	15	-	nC
t_a	reverse recovery rise time			-	13	-	ns
t_b	reverse recovery fall time			-	8.2	-	ns

[1] includes capacitive recovery



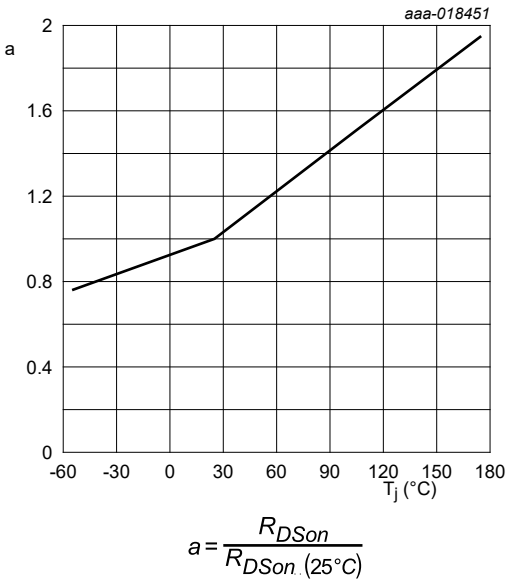


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

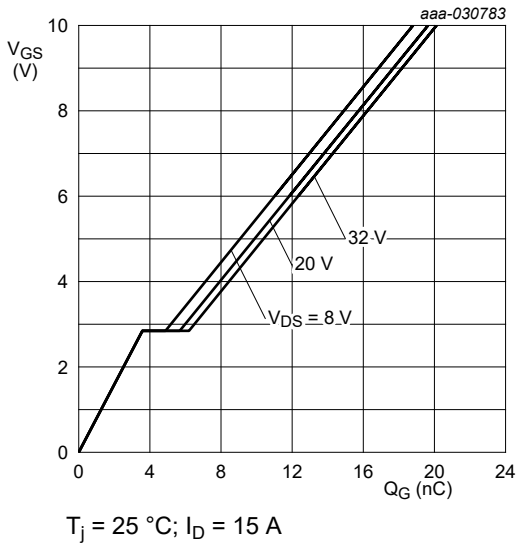


Fig. 12. Gate-source voltage as a function of gate charge; typical values

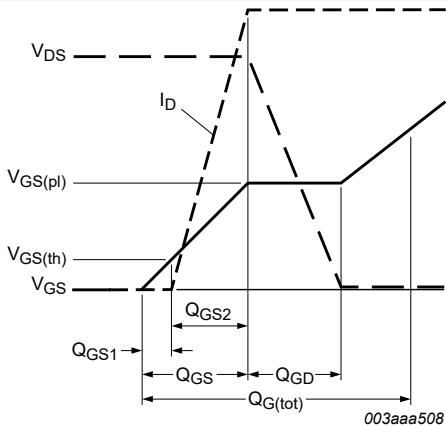


Fig. 13. Gate charge waveform definitions

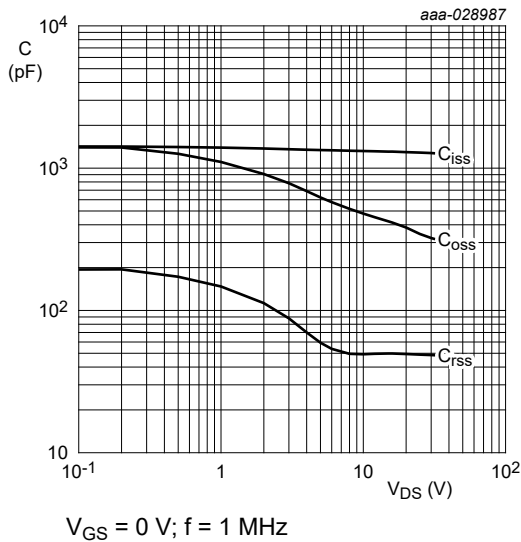
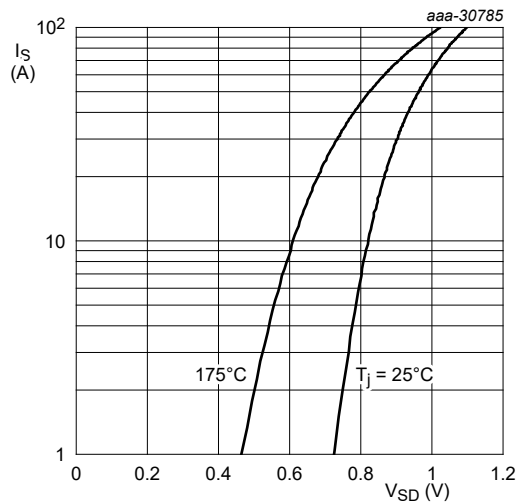


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

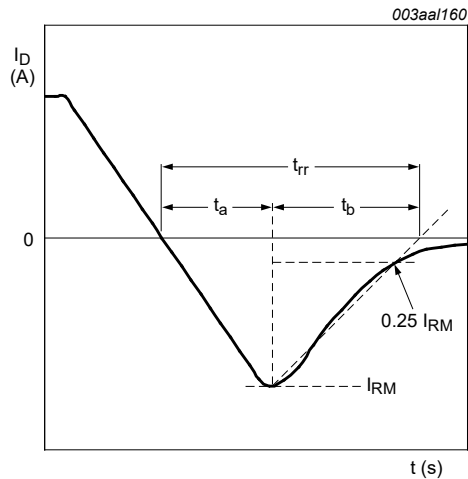


Fig. 16. Reverse recovery timing definition

10. Package outline

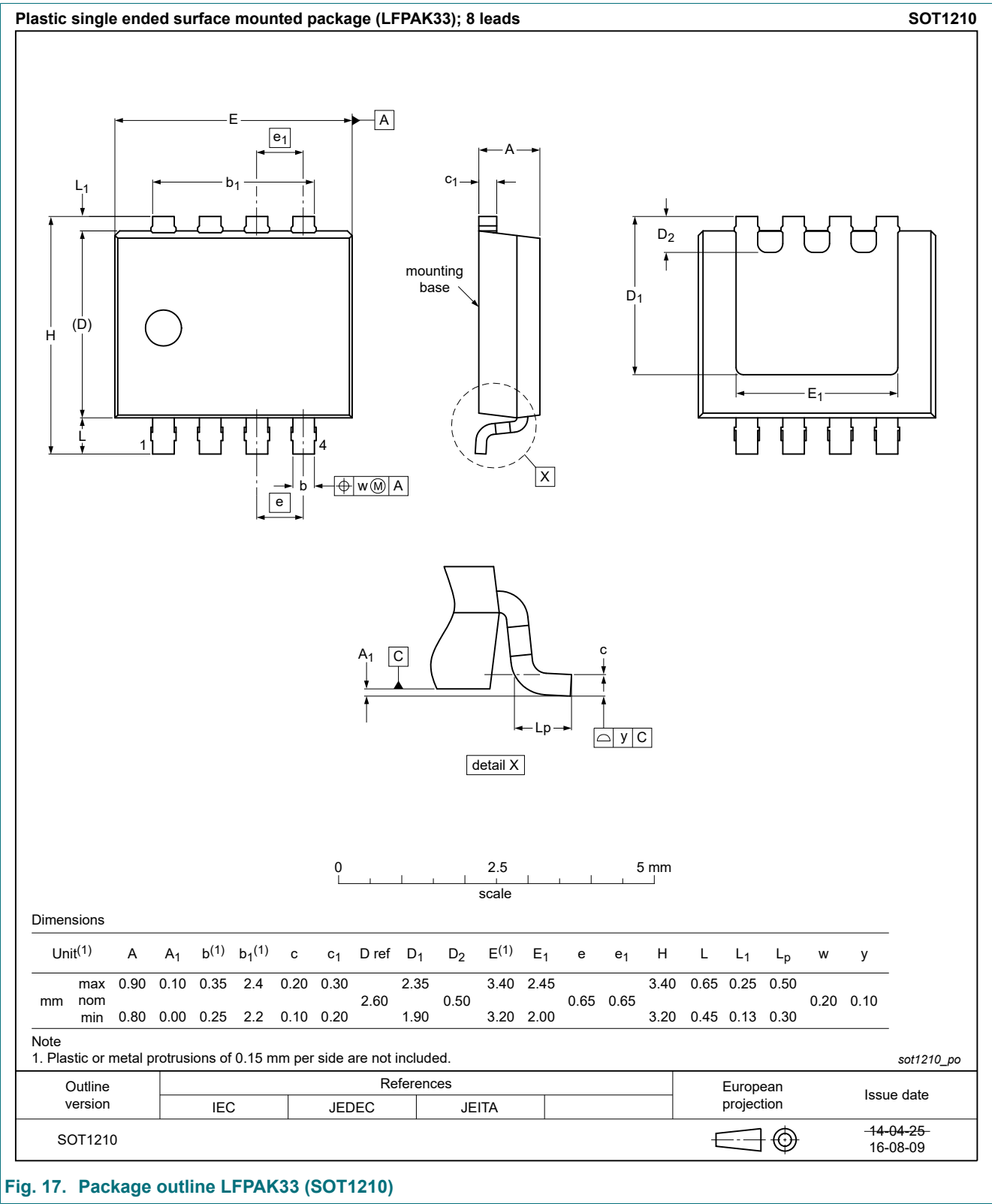


Fig. 17. Package outline LPAK33 (SOT1210)

11. Soldering

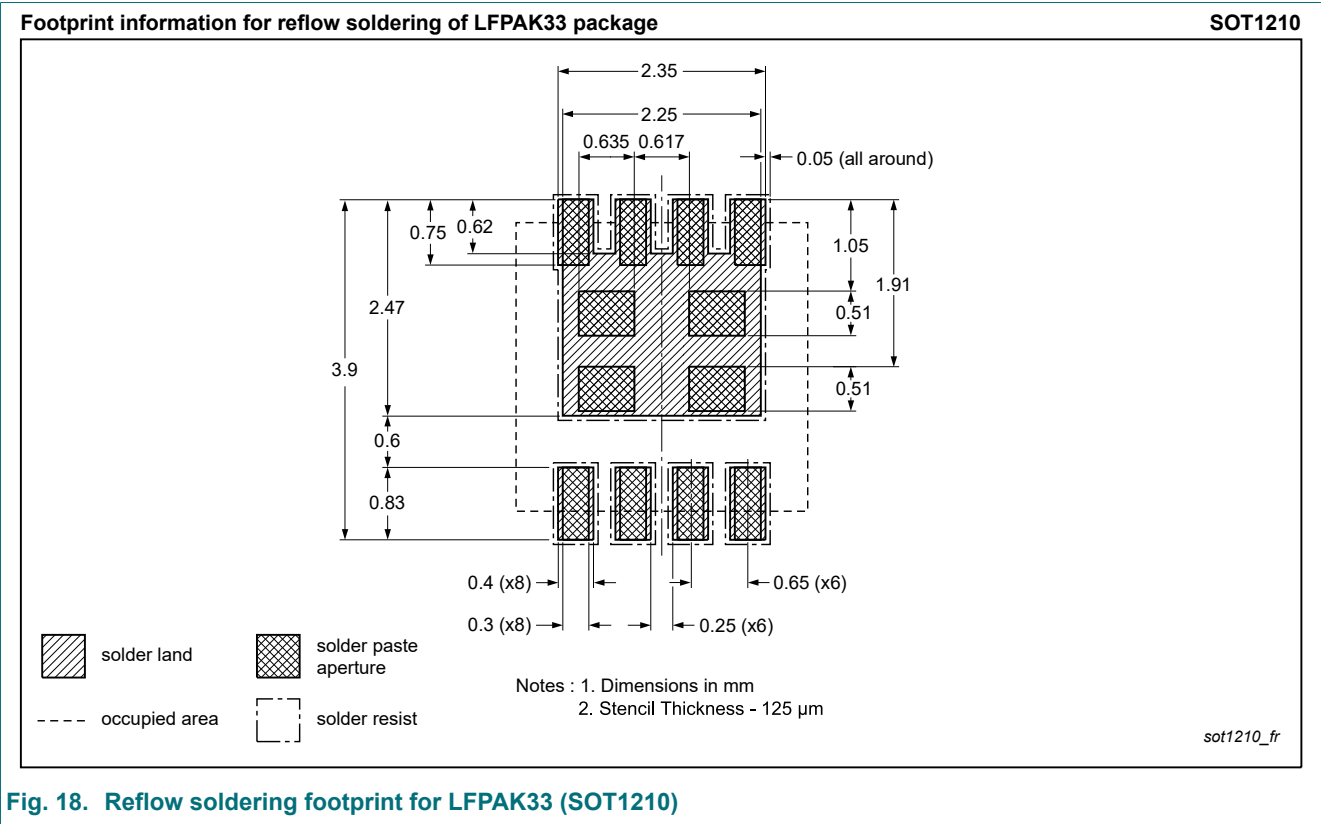


Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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