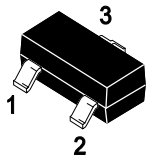
S-LP2309LT1G

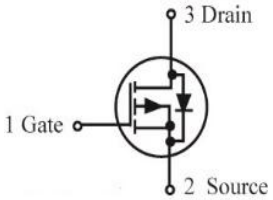
P-Channel 60V (D-S) MOSFET

1. FEATURES

- RDS(ON)≤ 215mΩ , Vgs@-10V.
- RDS(ON)≤ 260mΩ , Vgs@-4.5V.
- Super high density cell design for extremely low RDS(ON).
- Exceptional on-resistance and maximum DC current capability.
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.



SOT23(TO-236)



2. APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
S-LP2309LT1G	P09	3000/Tape&Reel
S-LP2309LT3G	P09	10000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter		Symbol	Limits		Unit
Drain–Source Voltage		VDSS	-60		V
Gate–to–Source Voltage – Continuous		VGS	±20		V
Continuous Drain Current	Ta=25℃	ID	-1.9		A
	Ta=70℃		-1.5		
Pulsed Drain Current		IDM	-7.6		
Maximum Power Dissipation	Ta=25℃	PD	1.4		W
	Ta=70℃		0.9		
Junction Temperature		Tj	150		℃
Storage Temperature Range		Tstg	-55~+150		℃
Thermal Resistance-Junction to Ambient(Note 1)		RθJA	t≤10s	170	℃/W
			Steady State	225	
Thermal Resistance-Junction to Case(Note 1)		RθJC	90		

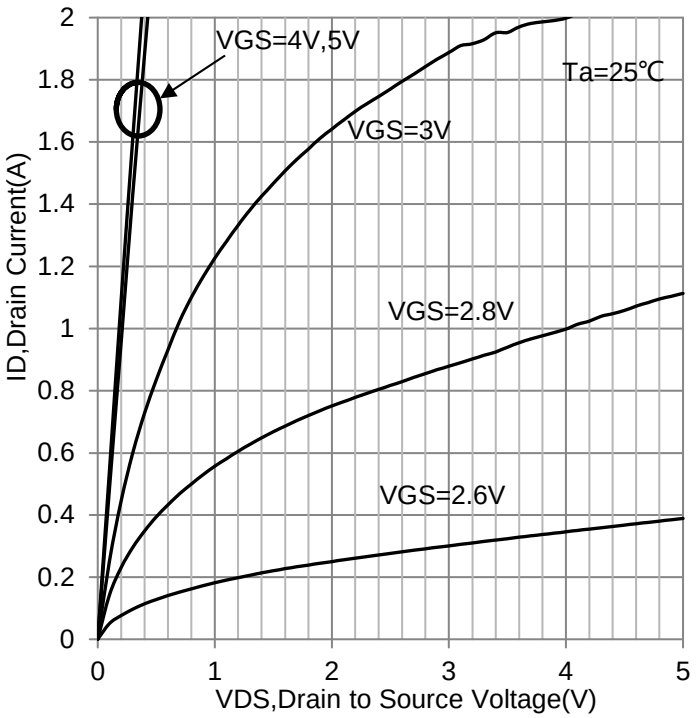
1.The device mounted on 1in ² FR4 board with 2 oz copper

5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

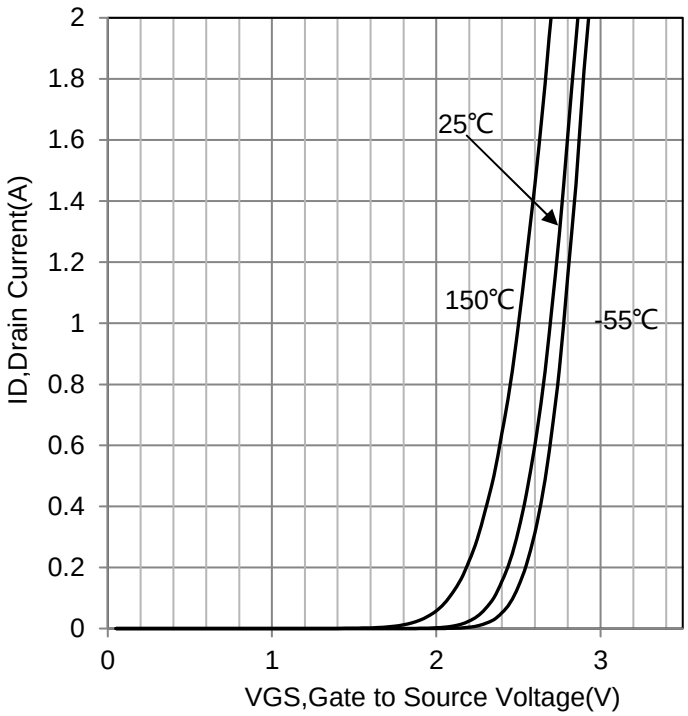
Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)		VBRDSS	-60	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = -250μA)		VGS(th)	-1	-	-3	V
Gate Leakage Current (VDS =0V, VGS =±20V)		IGSS	-	-	±100	nA
Zero Gate Voltage Drain Current (VGS = 0V, VDS = -60 V)		IDSS	-	-	-10	μA
Static Drain–Source On–State Resistance (VGS = -10 V, ID = -1.8 A) (VGS = -4.5 V, ID = -1.4 A)		RDS(on)	- -	170 200	215 260	mΩ
Forward Voltage (VGS = 0 V, IS = -1.2 A)		VSD	-	-	-1.2	V
DYNAMIC						
Total Gate Charge (VGS = -4.5 V, ID =-1A,VDS= -48 V)		Qg	-	4.06	-	nC
Gate-Source Charge (VGS = -4.5 V, ID =-1A,VDS= -48 V)		Qgs	-	1.04	-	
Gate-Drain Charge (VGS = -4.5 V, ID =-1A,VDS= -48 V)		Qgd	-	2.1	-	
Input Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -30 V)		Ciss	-	373	-	pF
Output Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -30 V)		Coss	-	24.2	-	
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz,VDS= -30 V)		Crss	-	17.4	-	
Turn-On Delay Time	(VDS = -30V, RL= 30Ω ID = -1A, VGS = -10V RG = 3.1Ω)	td(on)	-	3.6	-	ns
Rise Time		tr	-	3.6	-	
Turn-Off Delay Time		td(off)	-	16.7	-	
Fall Time		tf	-	2.9	-	
Gate-Resistance (VGS = 0 V, VDS=0V,f=1MHz)		Rg	-	6.5	-	Ω

2.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

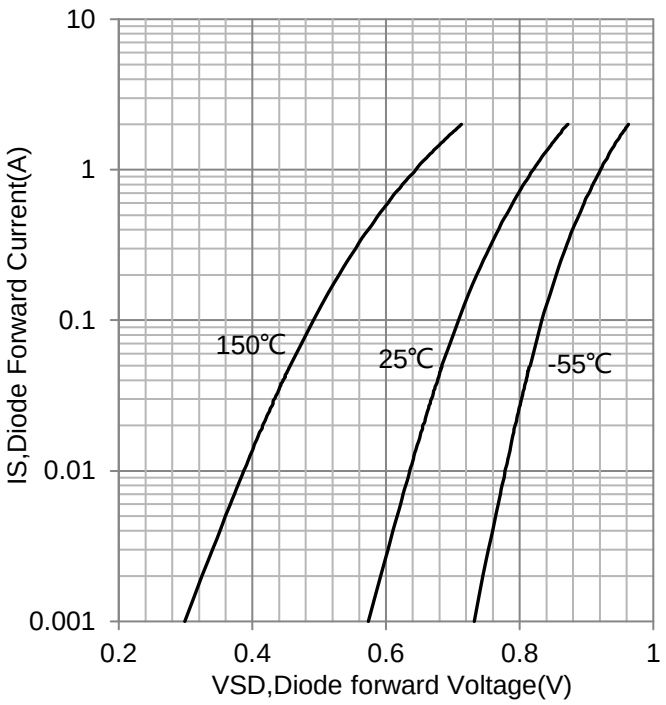
6.ELECTRICAL CHARACTERISTICS CURVES



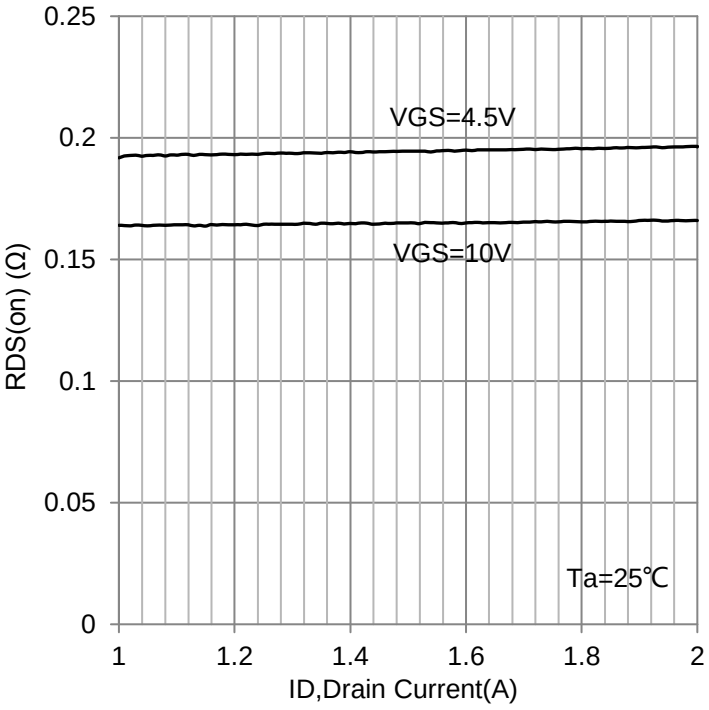
ID vs. VDS



ID vs. VGS

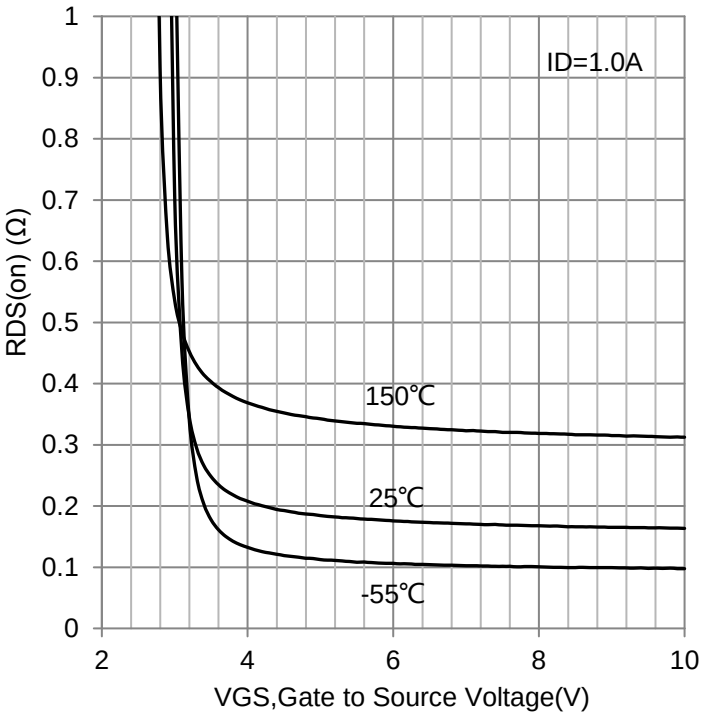


IS vs. VSD

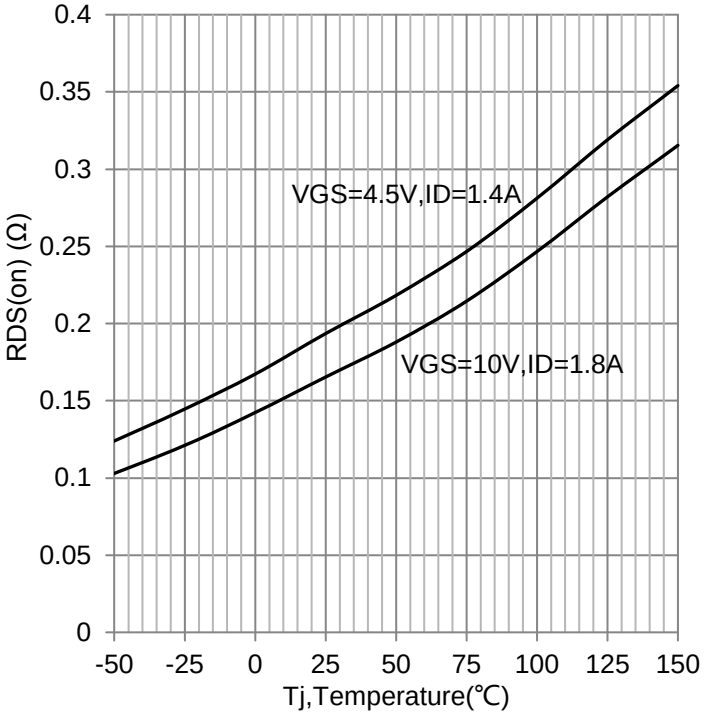


RDS(on) vs. ID

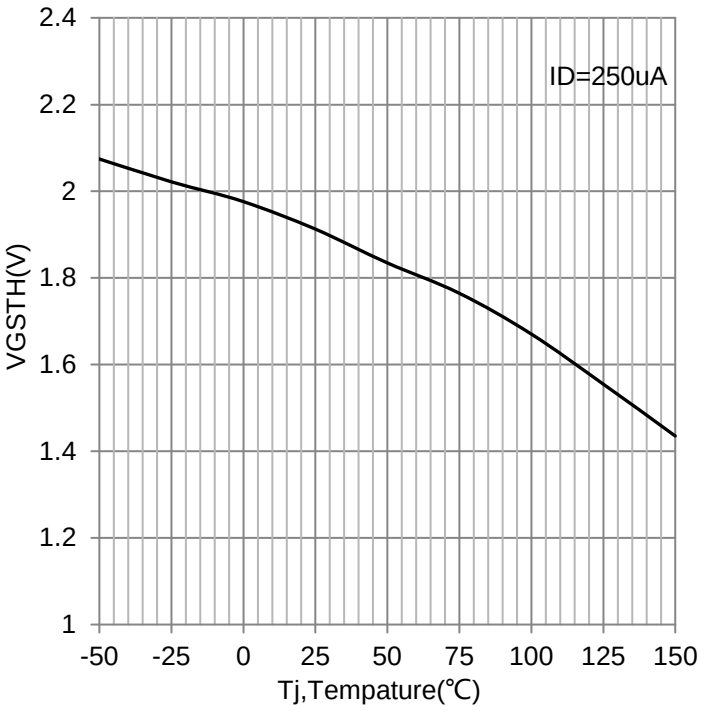
6.ELECTRICAL CHARACTERISTICS CURVES(Con.)



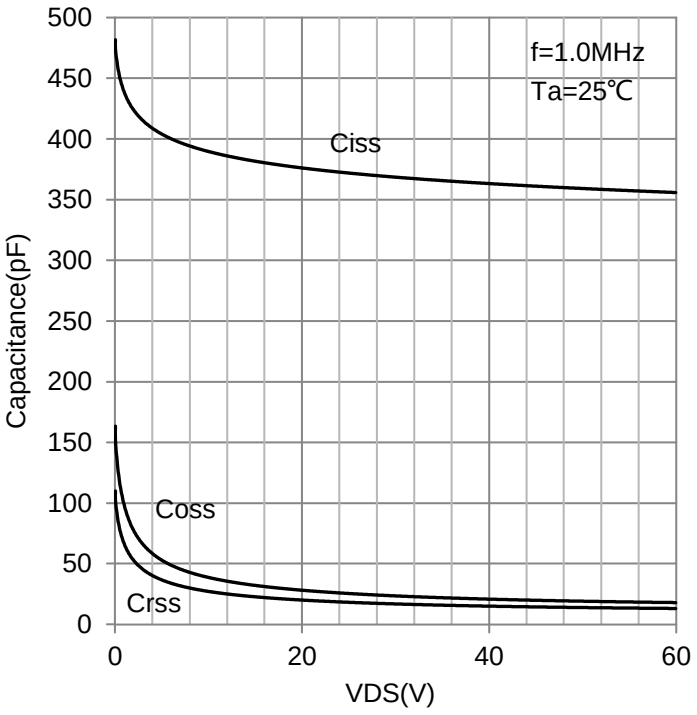
RDS(on) vs. VGS



RDS(on) vs. Tj

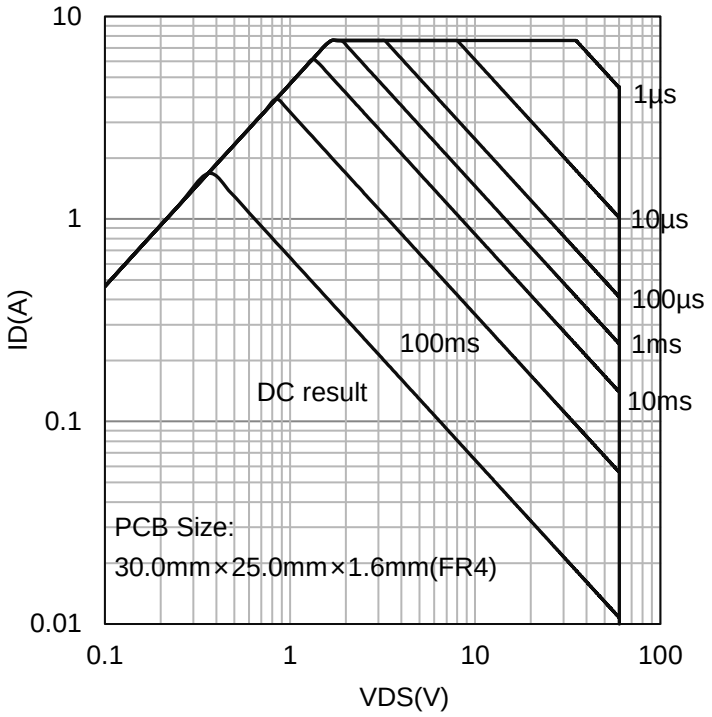


VGSTH vs. Tj



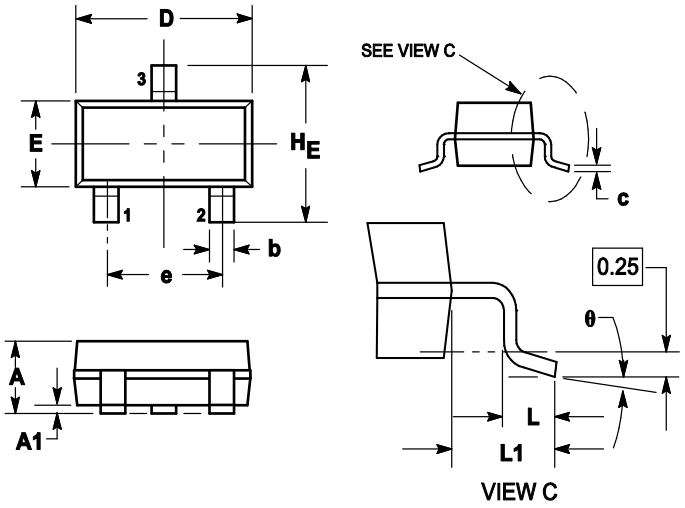
Capacitance

6.ELECTRICAL CHARACTERISTICS CURVES(Con.)



Safe Operating Area

7.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

8.SOLDERING FOOTPRINT