

N- and P-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	60	0.028 at V _{GS} = 10 V	5.3	6 nC
		0.031 at V _{GS} = 4.5 V	4.7	
P-Channel	- 60	0.050 at V _{GS} = - 10 V	- 4.9	8 nC
		0.060 at V _{GS} = - 4.5 V	- 4.5	

FEATURES

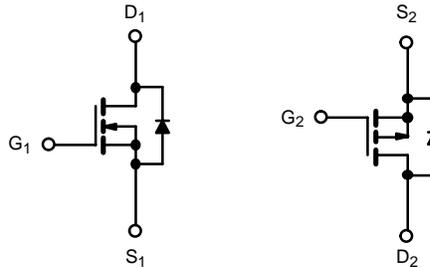
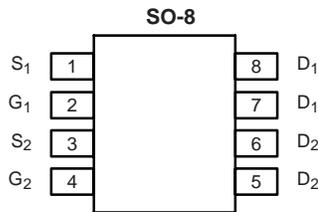
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested

APPLICATIONS

- CCFL Inverter



RoHS
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	60	- 60	V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	5.3	- 4.9	A
		T _C = 70 °C	4.3	- 4.2	
		T _A = 25 °C	4.3 ^{b, c}	- 4.0 ^{b, c}	
		T _A = 70 °C	3.4 ^{b, c}	- 3.4 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	20	- 25	A	
Source Drain Current Diode Current	I _S	T _C = 25 °C	2.6		- 2.8
		T _A = 25 °C	1.7 ^{b, c}		- 1.7 ^{b, c}
Pulsed Source-Drain Current	I _{SM}	20	- 25	mJ	
Single Pulse Avalanche Current	I _{AS}	11	15		
Single Pulse Avalanche Energy	E _{AS}	6.1	11	W	
Maximum Power Dissipation	P _D	T _C = 25 °C	3.1		3.4
		T _C = 70 °C	2		2.2
		T _A = 25 °C	2 ^{b, c}		2 ^{b, c}
		T _A = 70 °C	1.3 ^{b, c}	1.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, d}	R _{thJA}	55	62.5	53	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	R _{thJF}	33	40	30	37		

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 110 °C/W for N-Channel and P-Channel.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	60			V	
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-60				
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		55		mV	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-50			
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-6		mV	
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		4			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1		3	V	
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1		-3		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			100	nA	
			P-Ch			-100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA	
			P-Ch			-1		
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			10		
			P-Ch			-10		
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	20			A	
		$V_{DS} \leq -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-25				
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$	N-Ch		0.026	0.028	Ω	
		$V_{GS} = -10\text{ V}, I_D = -3.1\text{ A}$	P-Ch		0.055	0.060		
		$V_{GS} = 4.5\text{ V}, I_D = 3.9\text{ A}$	N-Ch		0.029	0.035		
		$V_{GS} = -4.5\text{ V}, I_D = -0.2\text{ A}$	P-Ch		0.060	0.070		
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 4.3\text{ A}$	N-Ch		15		S	
		$V_{DS} = -15\text{ V}, I_D = -3.1\text{ A}$	P-Ch		8.5			
Dynamic^a								
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		665		μF	
			P-Ch		650			
Output Capacitance	C_{oss}		P-Channel $V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		75		
				P-Ch		95		
Reverse Transfer Capacitance	C_{rss}			N-Ch		40		
				P-Ch		60		
Total Gate Charge	Q_g		$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.3\text{ A}$	N-Ch		13	20	nC
				P-Ch		14.5	22	
		$V_{DS} = 30\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 4.3\text{ A}$	N-Ch		6	9		
			P-Ch		8	12		
Gate-Source Charge	Q_{gs}	$V_{DS} = -30\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -3.1\text{ A}$	N-Ch		2.3			
Gate-Drain Charge	Q_{gd}		P-Ch		2.2			
			N-Ch		2.6			
P-Ch			3.7					
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch		2	3	Ω	
			P-Ch		14	20		

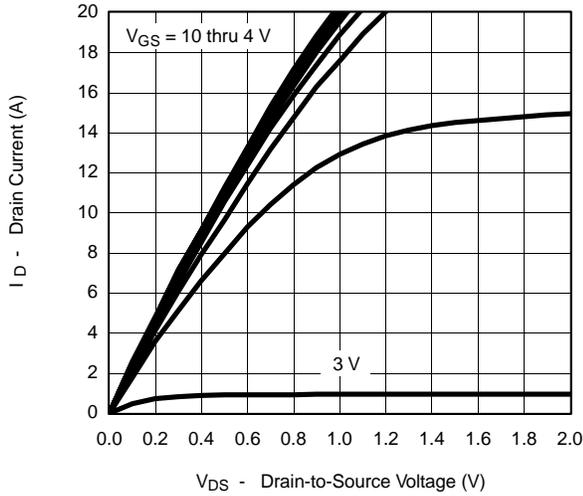
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit		
Dynamic^a								
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 30\text{ V}$, $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		15	25	ns	
Rise Time	t_r		P-Ch		30	45		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -30\text{ V}$, $R_L = 12.5\ \Omega$ $I_D \cong -2.4\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 1\ \Omega$	N-Ch		65	100		
			P-Ch		70	105		
Fall Time	t_f		N-Ch		15	25		
			P-Ch		40	60		
Turn-On Delay Time	$t_{d(on)}$		N-Channel $V_{DD} = 30\text{ V}$, $R_L = 8.8\ \Omega$ $I_D \cong 3.4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$	N-Ch		10		15
				P-Ch		10		15
Rise Time	t_r			N-Ch		15		25
				P-Ch		13		20
Turn-Off Delay Time	$t_{d(off)}$	N-Ch			20	30		
		P-Ch			35	55		
Fall Time	t_f	N-Ch			10	15		
		P-Ch			30	45		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch			2.6	A	
			P-Ch			-2.8		
Pulse Diode Forward Current ^a	I_{SM}		N-Ch			20	A	
			P-Ch			-25		
Body Diode Voltage	V_{SD}	$I_S = 1.7\text{ A}$	N-Ch		0.8	1.2	V	
		$I_S = -2\text{ A}$	P-Ch		-0.8	-1.2		
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 1.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		30	60	ns	
			P-Ch		30	50		
Body Diode Reverse Recovery Charge	Q_{rr}	P-Channel $I_F = -2\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	N-Ch		32	50	nC	
			P-Ch		35	60		
Reverse Recovery Fall Time	t_a		N-Ch		25		ns	
			P-Ch		16			
Reverse Recovery Rise Time	t_b	N-Ch		5		ns		
		P-Ch		14				

Notes:

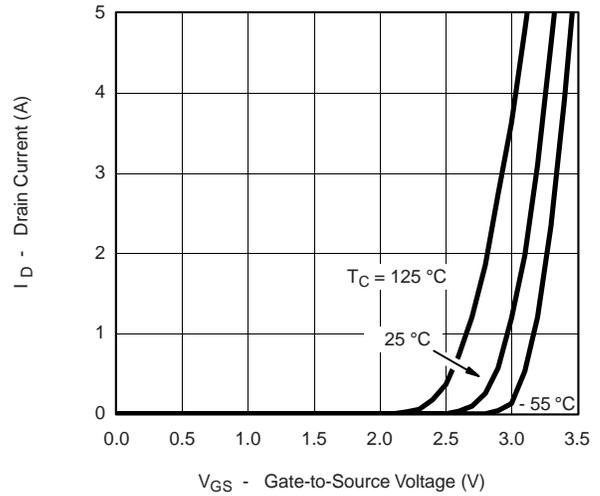
- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

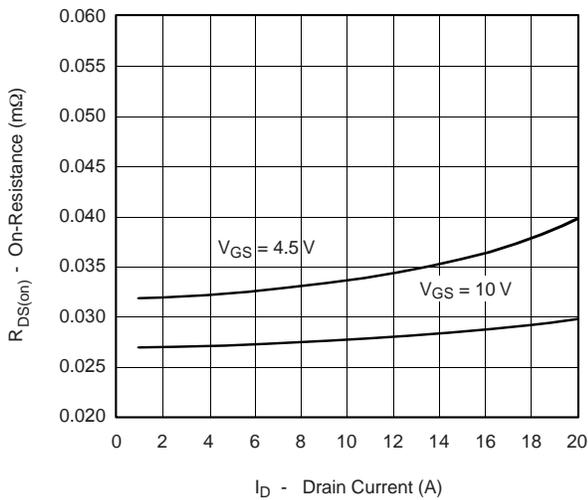
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



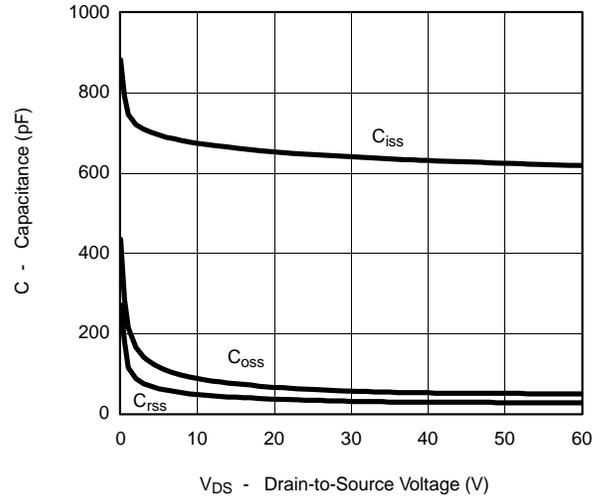
Output Characteristics



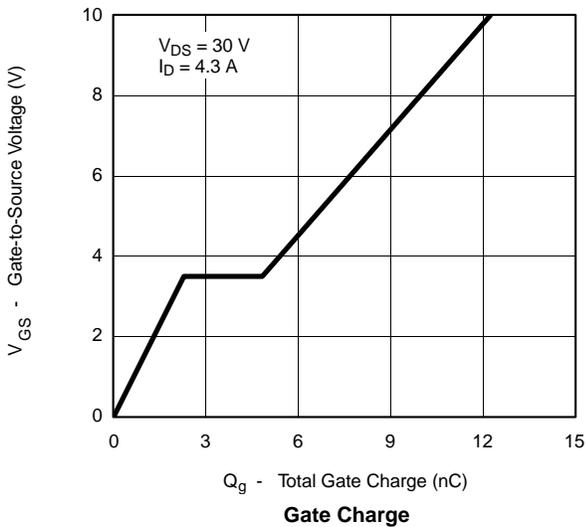
Transfer Characteristics



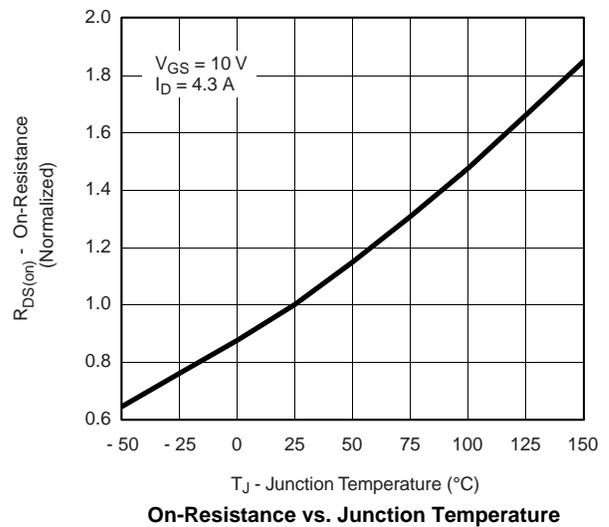
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

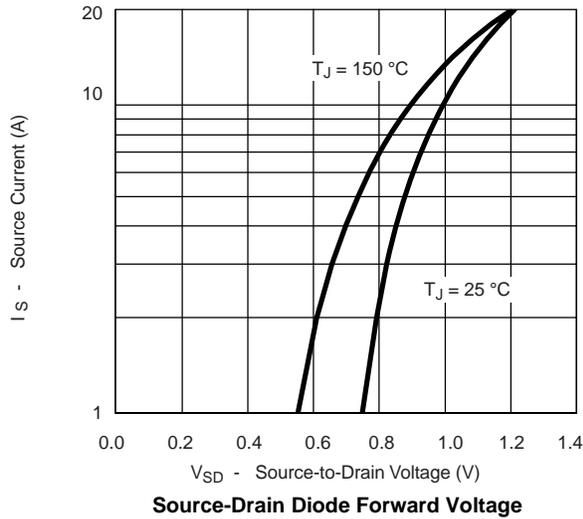


Gate Charge

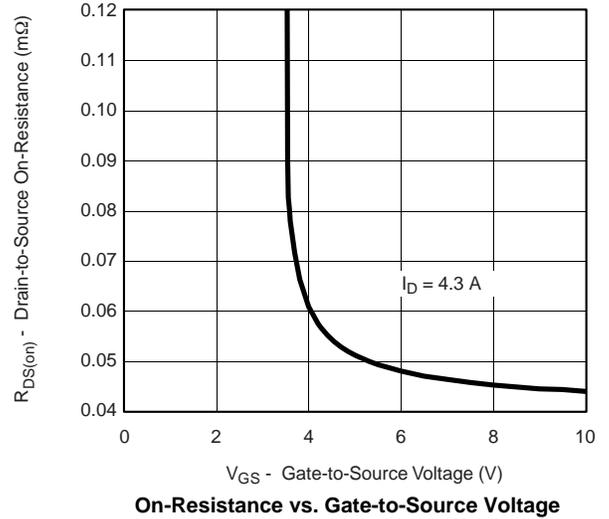


On-Resistance vs. Junction Temperature

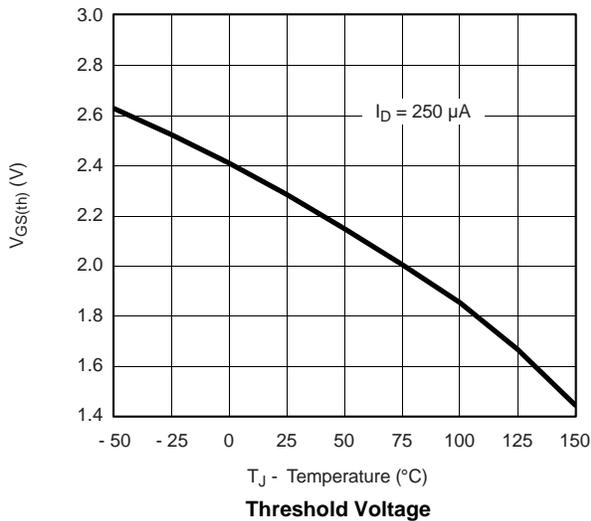
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



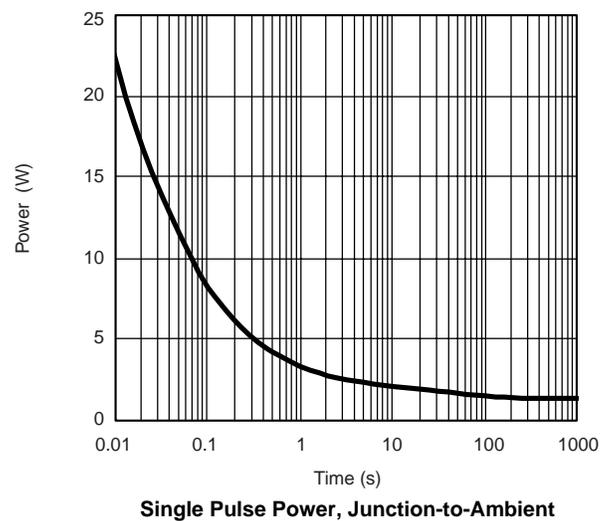
Source-Drain Diode Forward Voltage



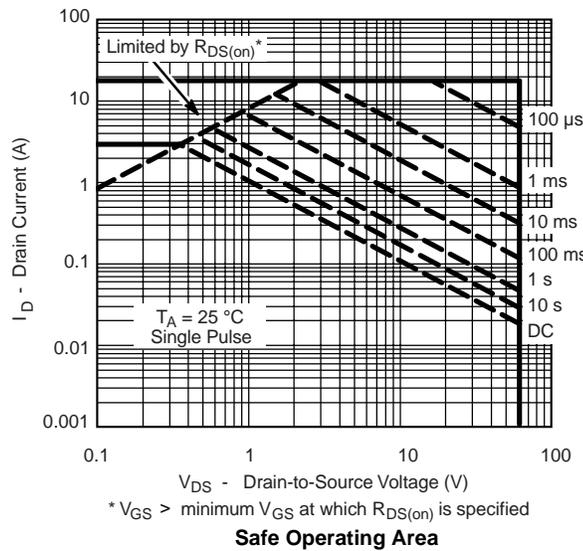
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

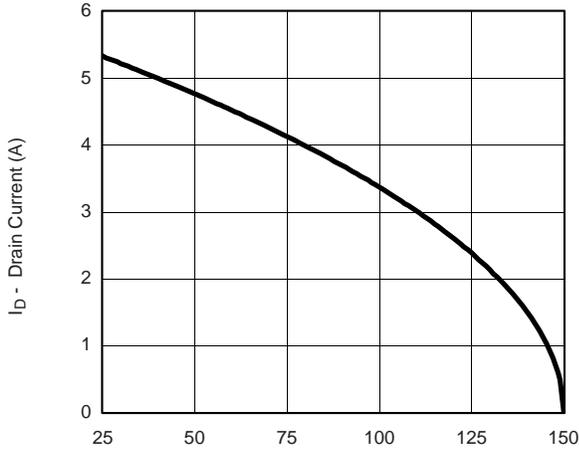


Single Pulse Power, Junction-to-Ambient

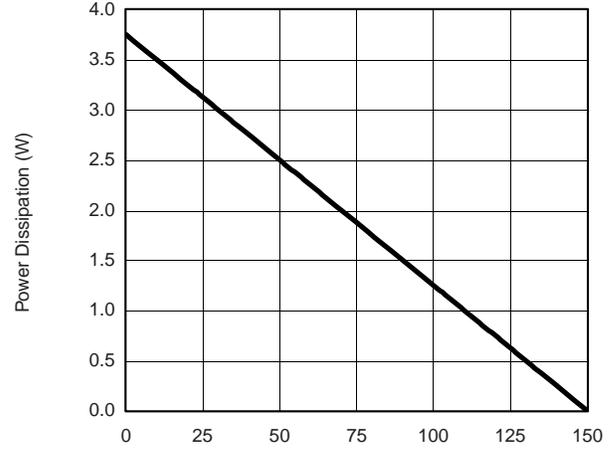


Safe Operating Area

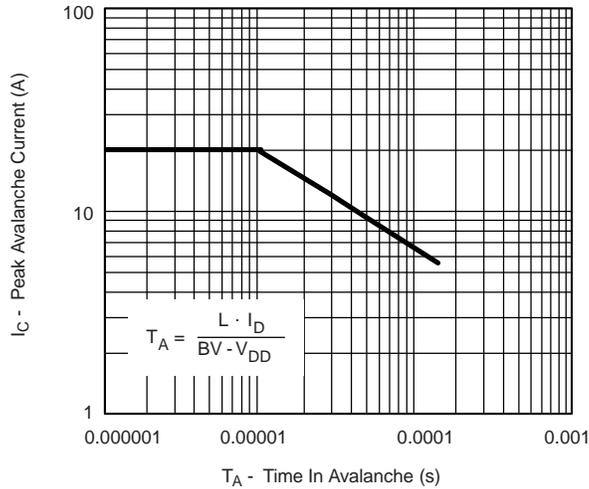
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



T_C - Case Temperature (°C)
Current Derating*



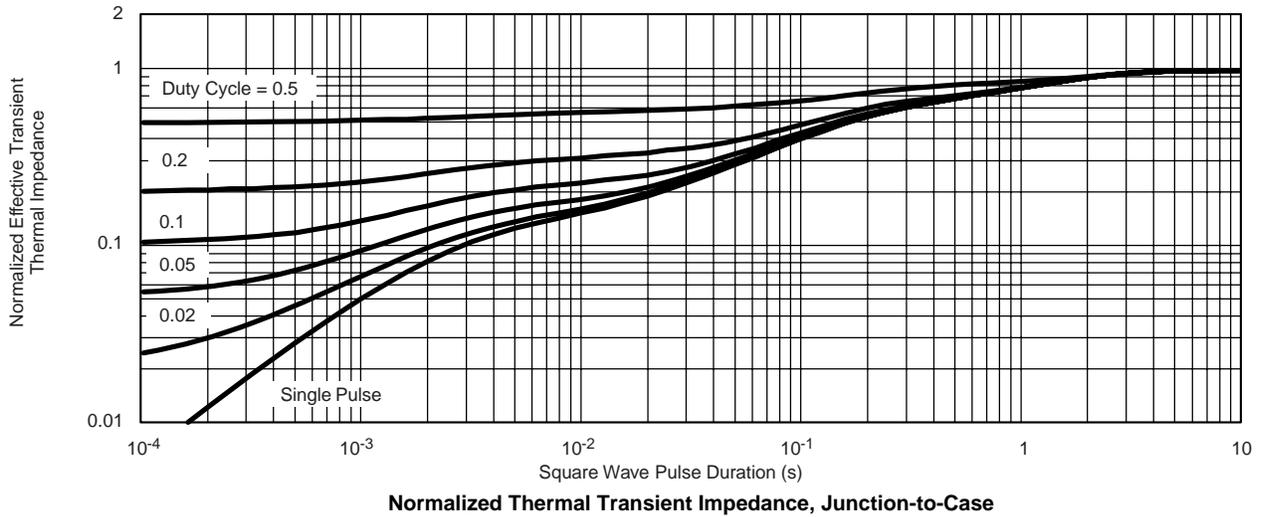
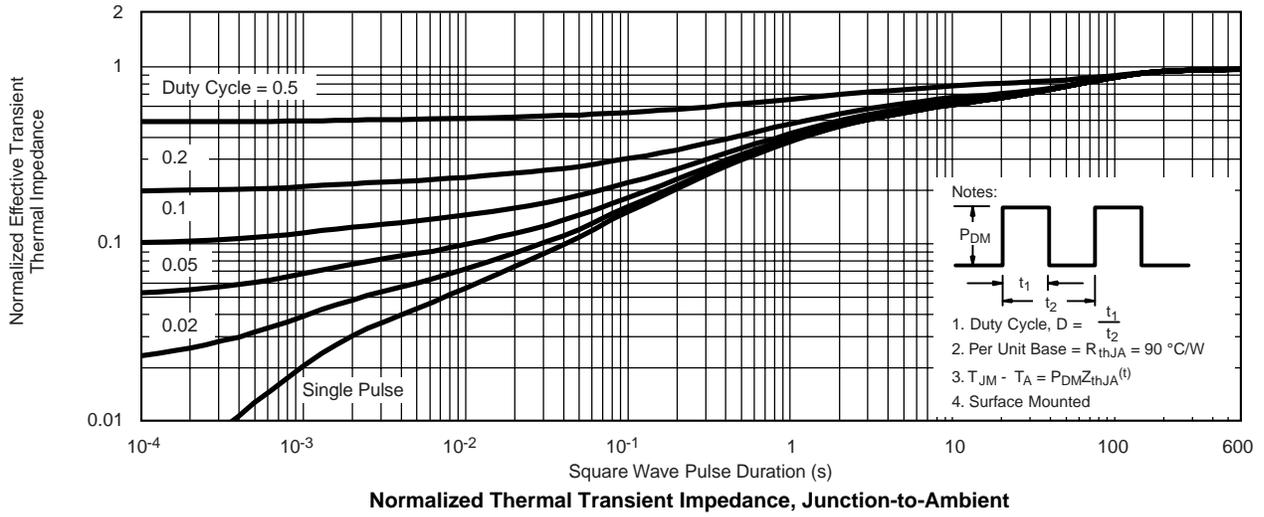
T_C - Case Temperature (°C)
Power Derating



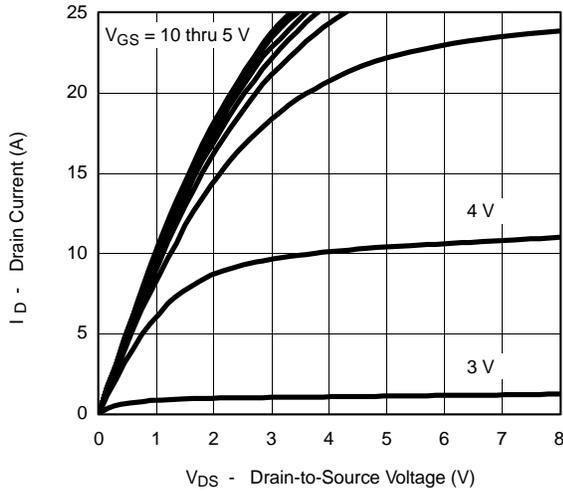
Single Pulse Avalanche Capability

* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

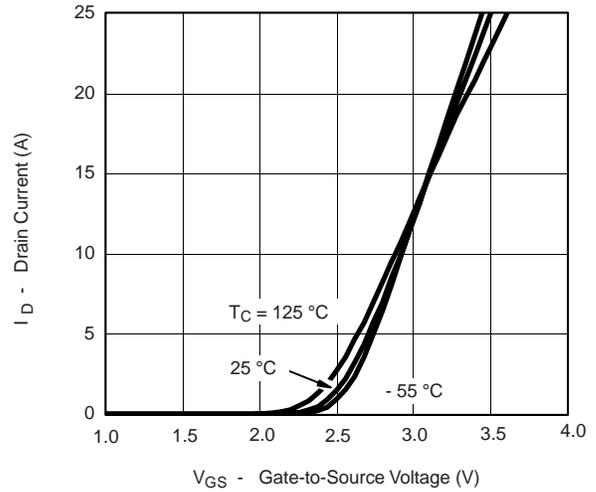
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



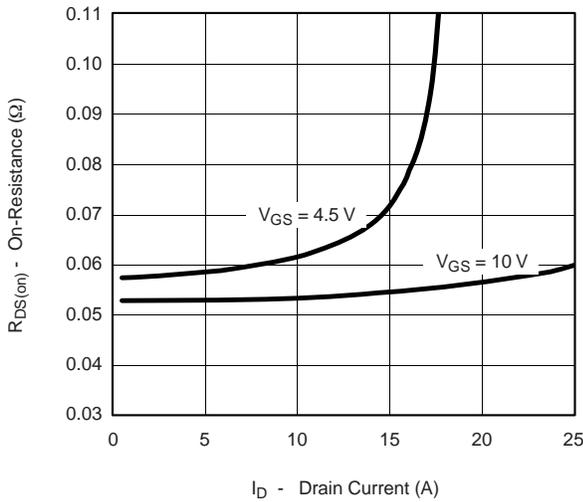
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



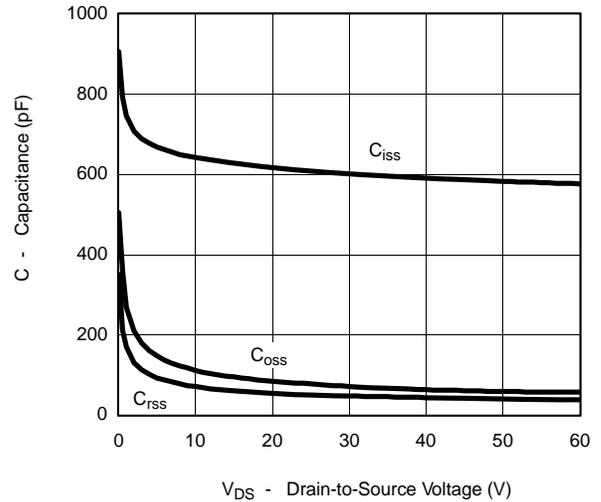
Output Characteristics



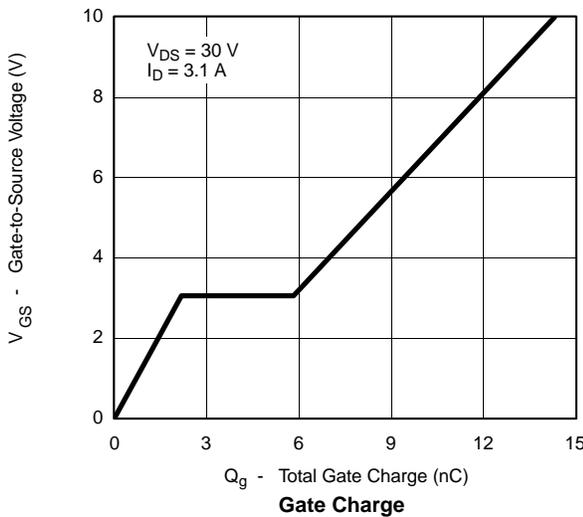
Transfer Characteristics



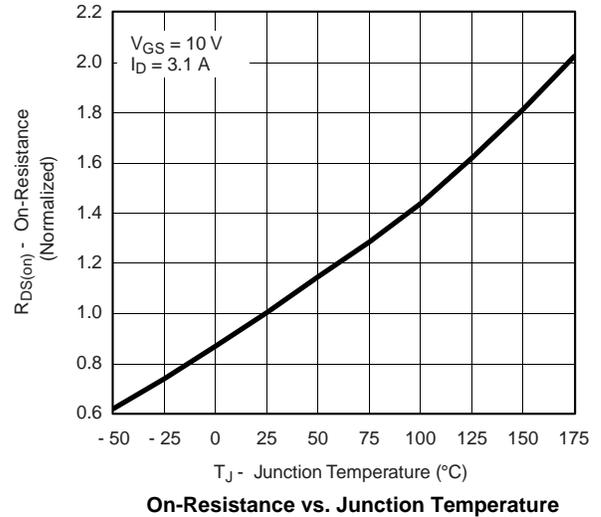
On-Resistance vs. Drain Current



Capacitance

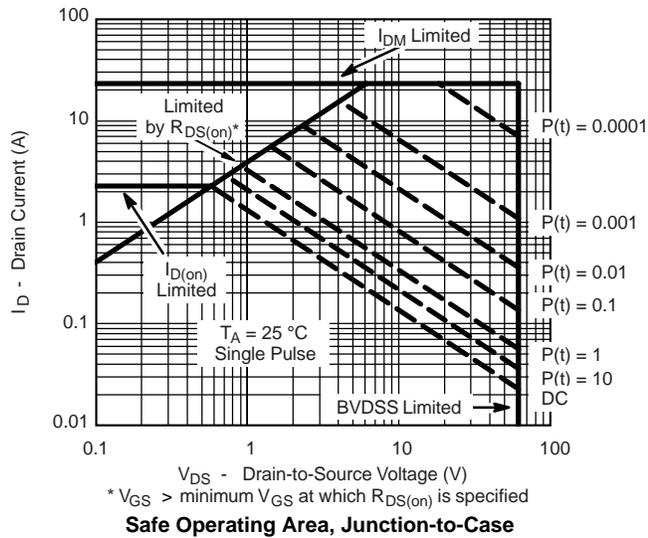
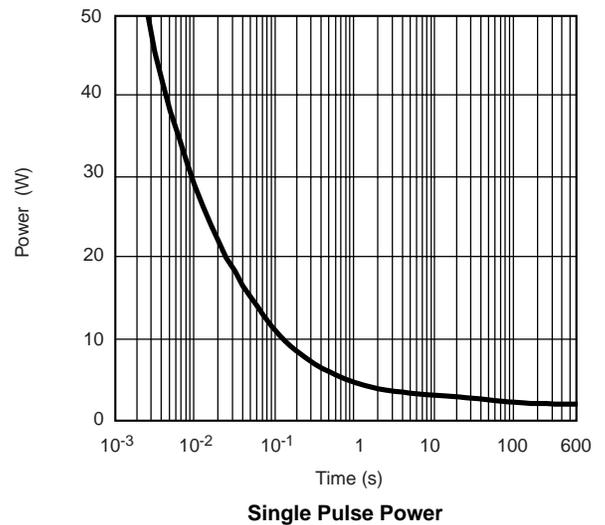
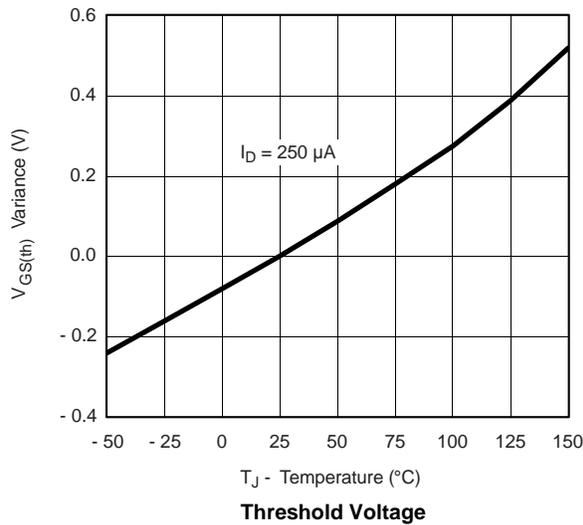
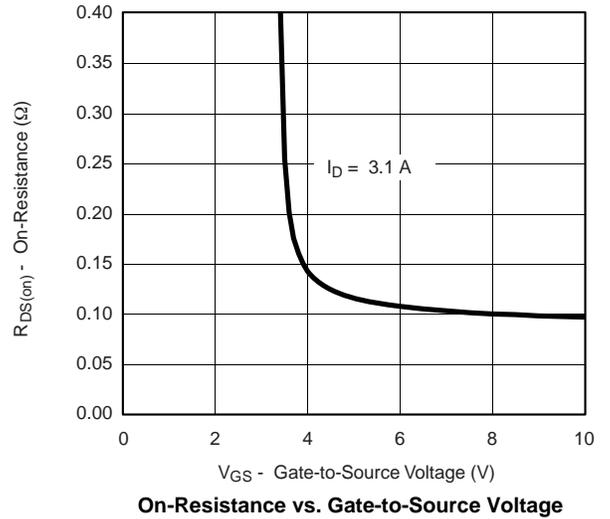
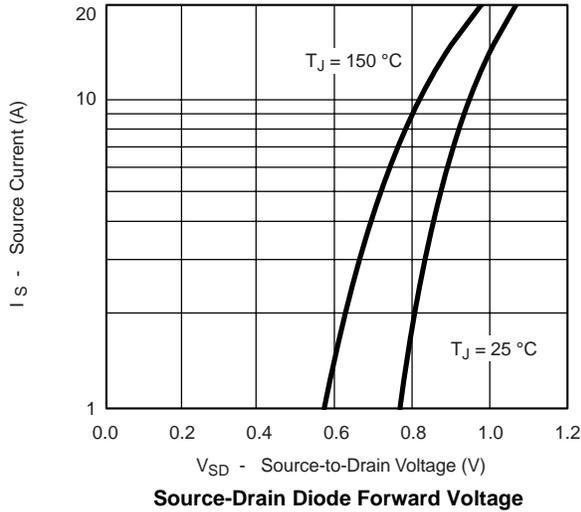


Gate Charge

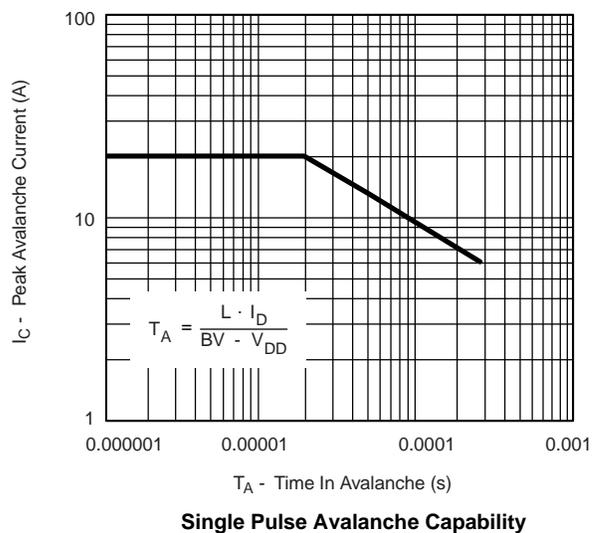
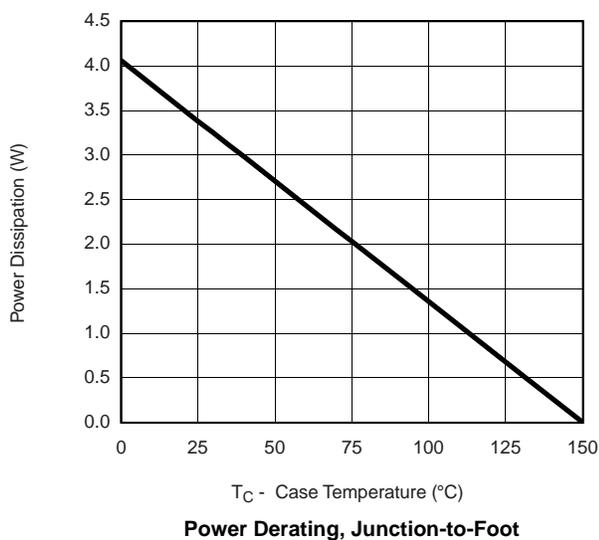
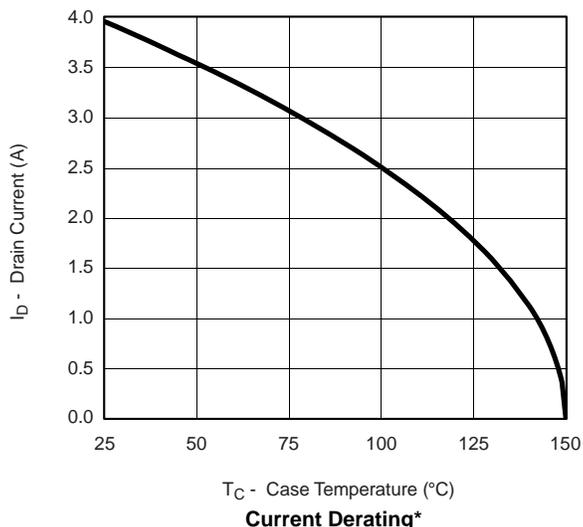


On-Resistance vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

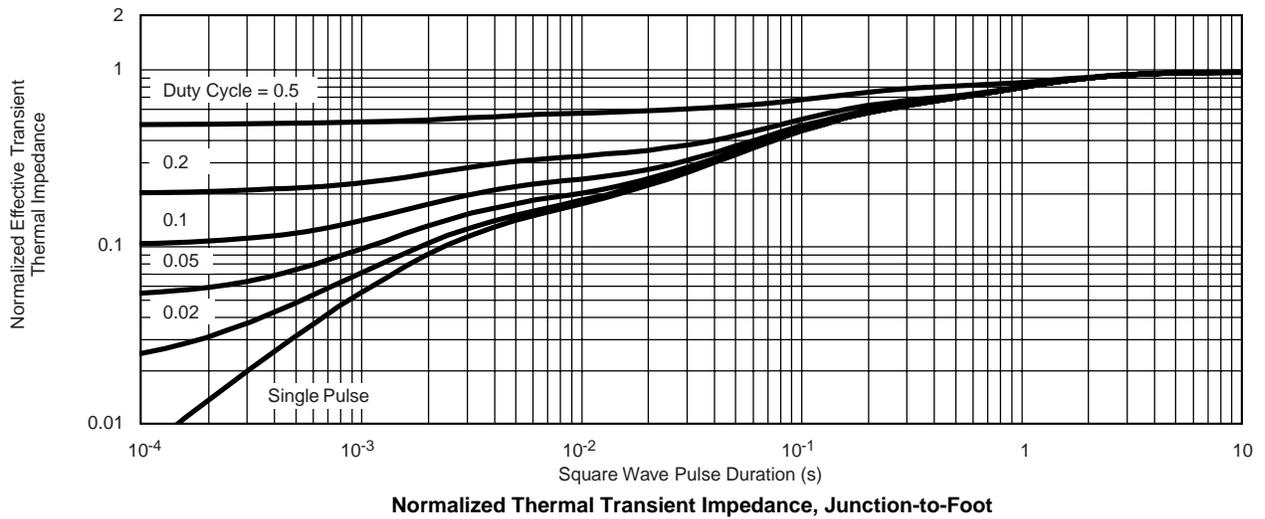
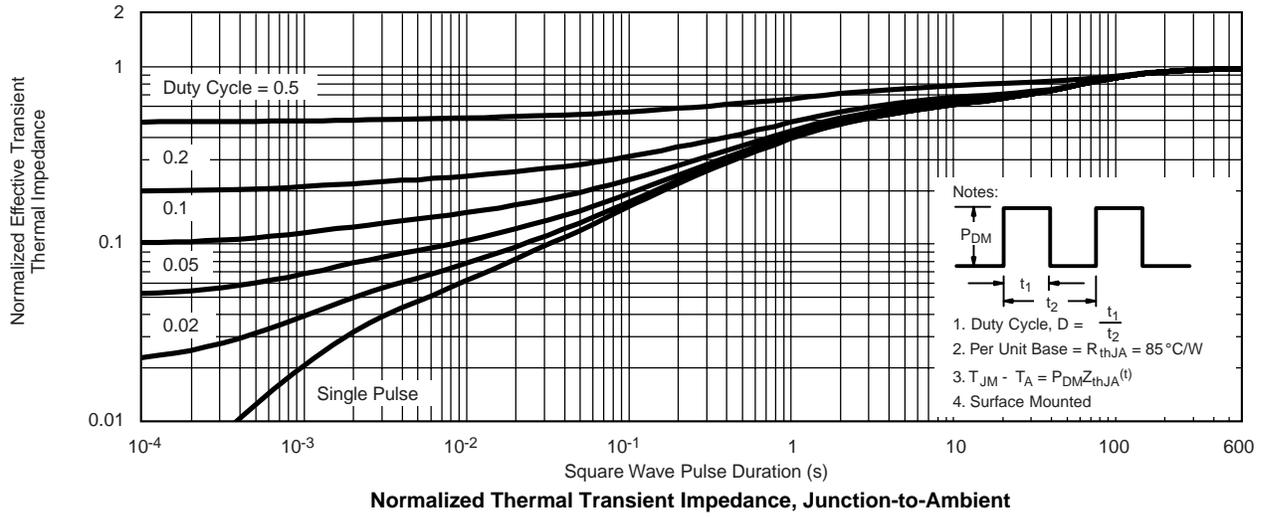


P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

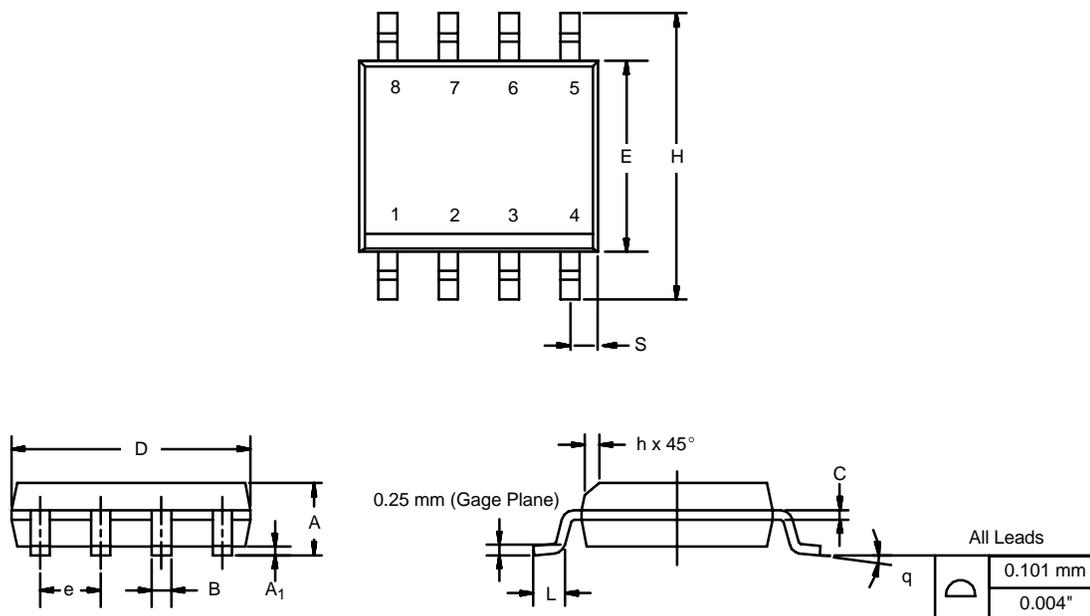


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P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

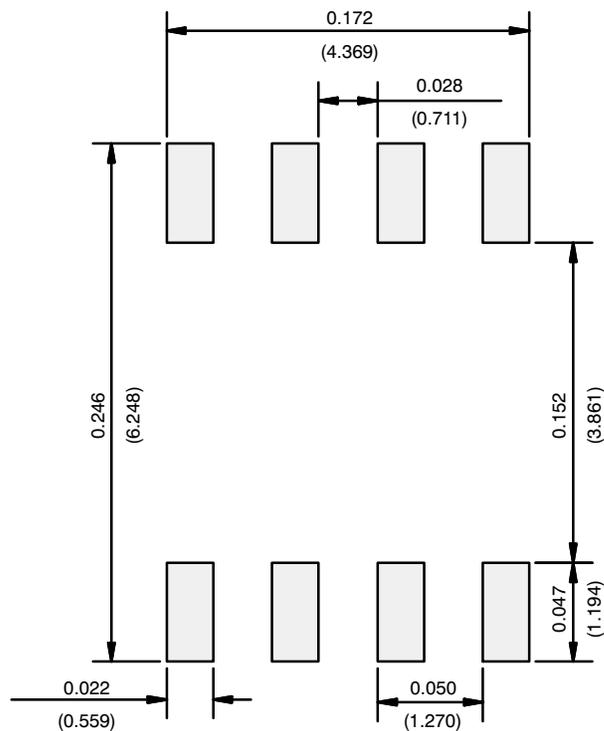


SOIC (NARROW): 8-LEAD
JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Taiwan VBsemi Electronics Co., Ltd., hereby certify that all of the products are determined to be RoHS compliant and meets the definition of restrictions under Directive of the European Parliament 2011/65 / EU, 2011 Nian. 6. 8 Ri Yue restrict the use of certain hazardous substances in electrical and electronic equipment (EEE) - modification, unless otherwise specified as inconsistent.(www.VBsemi.tw)

Please note that some documents may still refer to Taiwan VBsemi RoHS Directive 2002/95 / EC. We confirm that all products identified as consistent with the Directive 2002/95 / EC European Directive 2011/65 /.

Taiwan VBsemi Electronics Co., Ltd. hereby certify that all of its products comply identified as halogen-free halogen-free standards required by the JEDEC JS709A. Please note that some Taiwanese VBsemi documents still refer to the definition of IEC 61249-2-21, and we are sure that all products conform to confirm compliance with IEC 61249-2-21 standard level JS709A.