60 A VRPower® Integrated Power Stage

DESCRIPTION

The SiC620 and SiC620A are an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 5 mm x 5 mm MLP package, SiC620 and SiC620A enables voltage regulator design to deliver up to 60 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art TrenchFET Gen IV technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC620 and SiC620A incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and a thermal warning (THWn) that alerts the system of excessive junction temperature. This driver is also compatible with wide range of PWM controllers and supports Tri-state PWM, 3.3 V (SiC620A) / 5 V (SiC620) PWM logic, and zero current detect to improve light load efficiency.

FEATURES

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's Gen IV MOSFET technology and a low-side MOSFET with integrated Schottky diode
- Delivers up to 60 A continuous current
- 95 % peak efficiency
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 12 V input stage
- 3.3 V (SiC620A) / 5 V (SiC620) PWN logic with tri-state and hold-off
- Zero current detect control for light load efficiency improvement
- Low PWM propagation delay (< 20 ns)
- Thermal monitor flag
- Faster enable / disable
- Under voltage lockout for V_{CIN}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Multi-phase VRDs for CPU, GPU, and memory

TYPICAL APPLICATION DIAGRAM

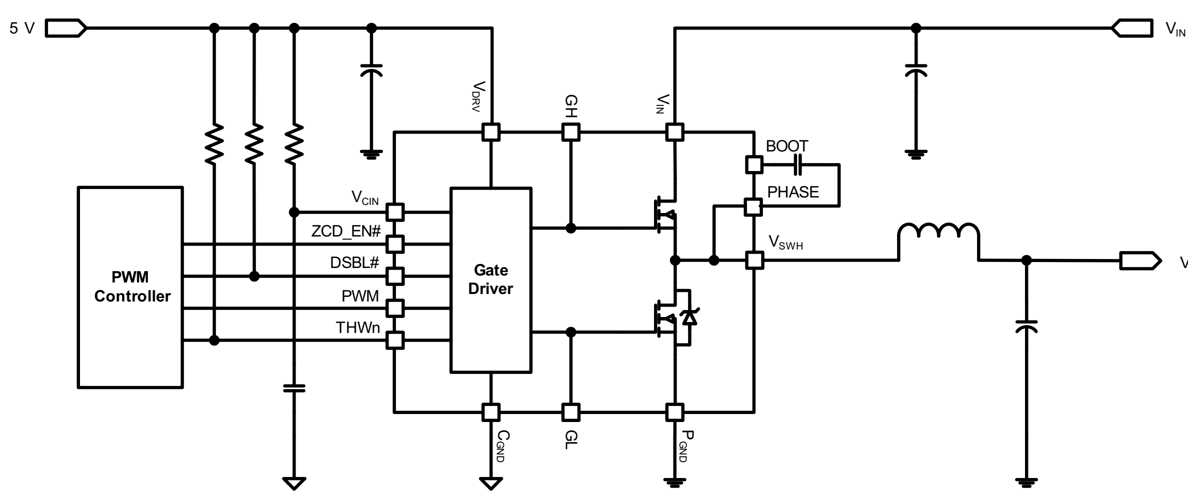

Fig. 1 - SiC620 and SiC620A Typical Application Diagram

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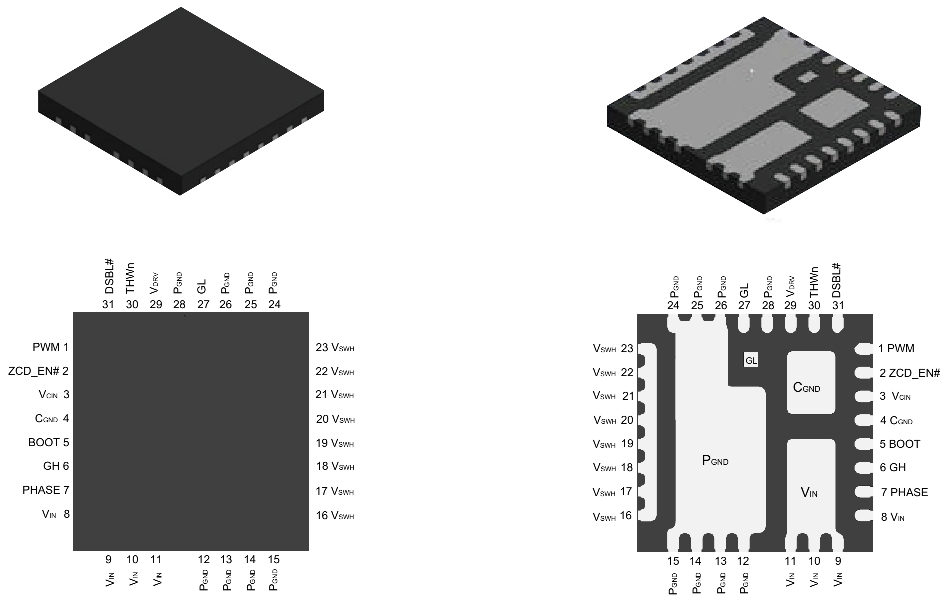
PINOUT CONFIGURATION



Top View

Bottom View

Fig. 2 - SiC620 and SiC620A Pin Configuration

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	PWM	PWM control input
2	ZCD_EN#	ZCD control. Active low
3	V_{CIN}	Supply voltage for internal logic circuitry
4	C_{GND}	Analog ground for the driver IC
5	BOOT	High-side driver bootstrap voltage
6	GH	High-side gate signal
7	Phase	Return path of high-side gate driver
8 to 11	V_{IN}	Power stage input voltage. Drain of high-side MOSFET
12 to 15, 24 to 26	P_{GND}	Power ground
16 to 23	V_{SWH}	Switch node of the power stage
27	GL	Low-side gate signal
29	V_{DRV}	Supply voltage for internal gate driver
30	THWn	Thermal warning open drain output
31	DSBL#	Disable pin. Active low

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING CODE**
SiC620ACD-T1-GE3	PowerPAK® MLP55-31L	SiC620A
SiC620CD-T1-GE3		SiC620
SiC620ADB and SiC620DB	Reference board	

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ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**CONDITIONS**	**LIMIT**	**UNIT**
Input Voltage	V_{IN}	-0.3 to 25	V
Control Logic Supply Voltage	V_{CIN}	-0.3 to 7	
Drive Supply Voltage	V_{DRV}	-0.3 to 7	
Switch Node (DC Voltage)	V_{SWH}	-0.3 to 25	
Switch Node (AC Voltage) (1)		-8 to 30	
Boot Voltage (DC Voltage)	V_{BOOT}	-0.3 to 32	
Boot to Switch Node (DC Voltage)	$V_{BOOT-VSWH}$	-0.3 to 7	
All Logic Inputs and Outputs (PWM, DSBL#, and THWn)		-0.3 to V_{CIN} + 0.3	
Output Current, $I_{OUT(AV)}$ (2)	f_S = 300 kHz, V_{IN} = 12 V, V_{OUT} = 1.8 V	60	A
	f_S = 1 MHz, V_{IN} = 12 V, V_{OUT} = 1.8 V	50	
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_{amb}	-40 to 125	
Storage Temperature	T_{stg}	-65 to 150	
Electrostatic Discharge Protection	Human Body Model, JESD-A114	3000	V

Note

(1) The specification values indicated "AC" is V_{SWH} to P_{GND} -8 V (< 20 ns, 10 µJ), min. and 30 V (< 50 ns), max.

(2) Output current rated with testing evaluation board at T_A = 25 °C with natural convection cooling. The rating is limited by the peak evaluation board temperature, T_J = 150 °C, and varies depending on the operating conditions and PCB layout. This rating may be changed with different application settings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	**MINIMUM**	**TYPICAL**	**MAXIMUM**	**UNIT**
Input Voltage (V_{IN})	4.5	-	18	V
Drive Supply Voltage (V_{DRV})	4.5	5	5.5	
Control Logic Supply Voltage (V_{CIN})	4.5	5	5.5	
Switch Node (V_{SWH}, DC Voltage)	-	-	18	
BOOT to V_{SWH}	4	4.5	5.5	
Thermal Resistance from Junction to Ambient	-	10.6	-	°C/W
Thermal Resistance from Junction to Case	-	1.6	-	

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ELECTRICAL SPECIFICATIONS (DSBL# = ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C)						
PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Control Logic Supply Current	I_{VCIN}	$V_{DSBL\#}$ = 0 V, no switching	-	12	-	µA
		$V_{DSBL\#}$ = 5 V, no switching, V_{PWM} = FLOAT	-	300	-	
		$V_{DSBL\#}$ = 5 V, f_S = 300 kHz, D = 0.1	-	380	-	
Drive Supply Current	I_{VDRV}	f_S = 300 kHz, D = 0.1	-	15	25	mA
		f_S = 1 MHz, D = 0.1	-	50	-	
		$V_{DSBL\#}$ = 0 V, no switching	-	25	-	µA
		$V_{DSBL\#}$ = 5 V, no switching	-	60	-	
BOOTSTRAP SUPPLY						
Bootstrap Diode Forward Voltage	V_F	I_F = 2 mA			0.4	V
PWM CONTROL INPUT (SiC620)						
Rising Threshold	$V_{TH\_PWM\_R}$	V_{PWM} = FLOAT	3.4	3.7	4.2	V
Falling Threshold	$V_{TH\_PWM\_F}$		0.7	0.9	1.2	
Tri-state Voltage	V_{TRI}		-	2.3	-	
Tri-state Rising Threshold	$V_{TRI\_TH\_R}$		0.9	-	1.5	
Tri-state Falling Threshold	$V_{TRI\_TH\_F}$		3	3.4	3.7	
Tri-state Rising Threshold Hysteresis	$V_{HYS\_TRI\_R}$		-	225	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS\_TRI\_F}$		-	325	-	
PWM Input Current	I_{PWM}	V_{PWM} = 5 V	-	-	350	µA
		V_{PWM} = 0 V	-	-	-350	
PWM CONTROL INPUT (SiC620A)						
Rising Threshold	$V_{TH\_PWM\_R}$	V_{PWM} = FLOAT	2.1	2.4	2.8	V
Falling Threshold	$V_{TH\_PWM\_F}$		0.7	0.9	1.2	
Tri-state Voltage	V_{TRI}		-	1.8	-	
Tri-state Rising Threshold	$V_{TRI\_TH\_R}$		0.9	1.2	1.5	
Tri-state Falling Threshold	$V_{TRI\_TH\_F}$		1.9	2.2	2.6	
Tri-state Rising Threshold Hysteresis	$V_{HYS\_TRI\_R}$		-	250	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS\_TRI\_F}$		-	300	-	
PWM Input Current	I_{PWM}	V_{PWM} = 3.3 V	-	-	225	µA
		V_{PWM} = 0 V	-	-	-225	
TIMING SPECIFICATIONS						
Tri-State to GH/GL Rising Propagation Delay	$t_{PD\_TRI\_R}$	No load, see fig. 4	-	30	-	ns
Tri-state Hold-Off Time	t_{TSHO}		-	130	-	
GH - Turn Off Propagation Delay	$t_{PD\_OFF\_GH}$		-	15	-	
GH - Turn ON Propagation Delay (Dead Time Rising)	$t_{PD\_ON\_GH}$		-	10	-	
GL - Turn Off Propagation Delay	$t_{PD\_OFF\_GL}$		-	12	-	
GL - Turn ON Propagation Delay (Dead Time Falling)	$t_{PD\_ON\_GL}$		-	10	-	
DSBL# Lo to GH/GL Falling Propagation Delay	$t_{PD\_DSBL\#\_F}$	Fig. 5	-	15	-	
PWM Minimum On-Time	$t_{PWM\_ON\_MIN}$		30	-	-	

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ELECTRICAL SPECIFICATIONS (DSBL# = ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C)						
PARAMETER	**SYMBOL**	**TEST CONDITION, UNLESS SPECIFIED**	**LIMITS**			**UNIT**
			MIN.	**TYP.** (1)	**MAX.**	
DSBL# ZCD_EN# INPUT						
DSBL# Logic Input Voltage	$V_{IH\_DSBL\#}$	Input logic high	2	-	-	V
	$V_{IL\_DSBL\#}$	Input logic low	-	-	0.8	
ZCD_EN# Logic Input Voltage	$V_{IH\_ZCD\_EN\#}$	Input logic high	2	-	-	
	$V_{IL\_ZCD\_EN\#}$	Input logic low	-	-	0.8	
PROTECTION						
Under Voltage Lockout	V_{UVLO}	V_{CIN} rising, ON threshold	-	3.7	4.3	V
		V_{CIN} falling, OFF threshold	2.7	3	-	
Under Voltage Lockout Hysteresis	V_{UVLO_HYST}		-	575	-	mV
THWn Flag Set (2)	T_{THWn_SET}		-	160	-	°C
THWn Flag Clear (2)	T_{THWn_CLEAR}		-	135	-	
THWn Flag Hysteresis (2)	T_{THWn_HYST}		-	25	-	
THWn Output Low	V_{OL_THWn}	I_{THWn} = 2 mA	-	0.02	-	V

Notes

(1) Typical limits are established by characterization and are not production tested.
(2) Guaranteed by design.

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above PWM_{TH_R} the low-side is turned OFF and the high-side is turned ON. When PWM input is driven below PWM_{TH_F} the high-side turns off and the low-side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC620 and SiC620A to pull the PWM input into the tri-state region (see the tri-state Voltage Threshold Diagram below). If the PWM input stays in this region for the tri-state Hold-Off Period, t_{TSHO}, both high-side and low-side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC620A incorporates PWM voltage thresholds that are compatible with 3.3 V logic and SiC620 is 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to C_{GND} and shut down the IC.

Diode Emulation Mode (ZCD_EN#)

When ZCD_EN# pin is Low and PWM signal switches Low, GL is forced on (after normal BBM time). During this time, it is under control of the ZCD (Zero Crossing Detect) comparator. If, after the internal blanking delay, the inductor current becomes zero, GL is turned off. This improves light load efficiency by avoiding discharge of output capacitors. If PWM enters tri-state, then device will go into normal tri-state mode after tri-state Delay. The GL output will be turned off regardless of Inductor current, this is an alternative method of improving light load efficiency by reducing switching losses.

Thermal Shutdown Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 kΩ to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC620 and SiC620A do not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

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Switch Node (V_{SWH} and PHASE)

The switch node is connected to the output filter circuit to deliver the regulated output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating the C_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gated rive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin. Shoot-through protection and adaptive dead time.

Shoot-Through Protection and Adaptive Dead Time

The SiC620 and SiC620A have an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1 V), that and built in delays ensure the one power MOSFET is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC620, SiC620A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

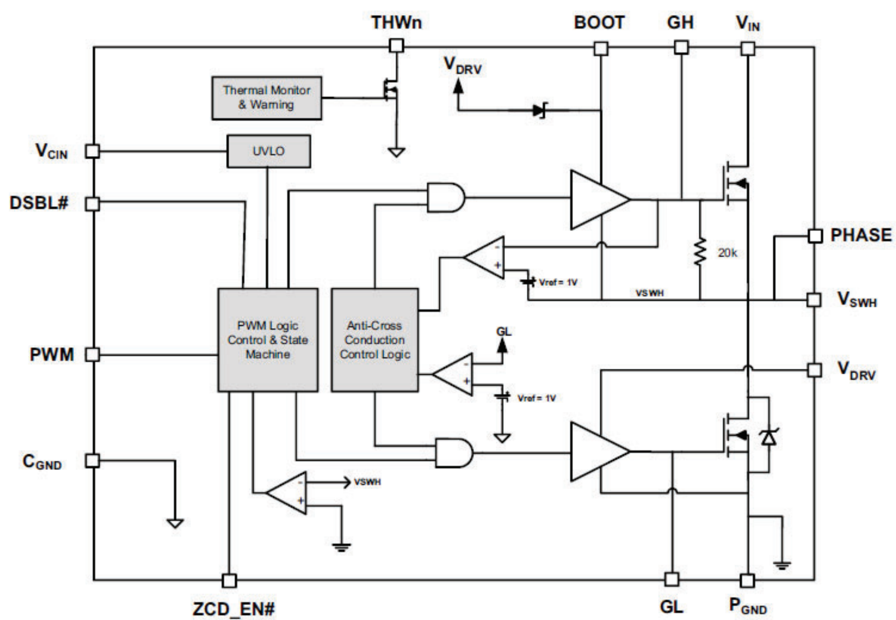

Fig. 3 - SiC620 and SiC620A Functional Block Diagram

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DEVICE TRUTH TABLE

DSBL#	ZCD_EN#	PWM	GH	GL
L	X	X	L	L
H	L	L	L	H, $I_L > 0$ A L, $I_L < 0$ A
H	L	H	H	L
H	L	Tri-state	L	L
H	H	L	L	H
H	H	H	H	L
H	H	Tri-state	L	L

PWM TIMING DIAGRAM

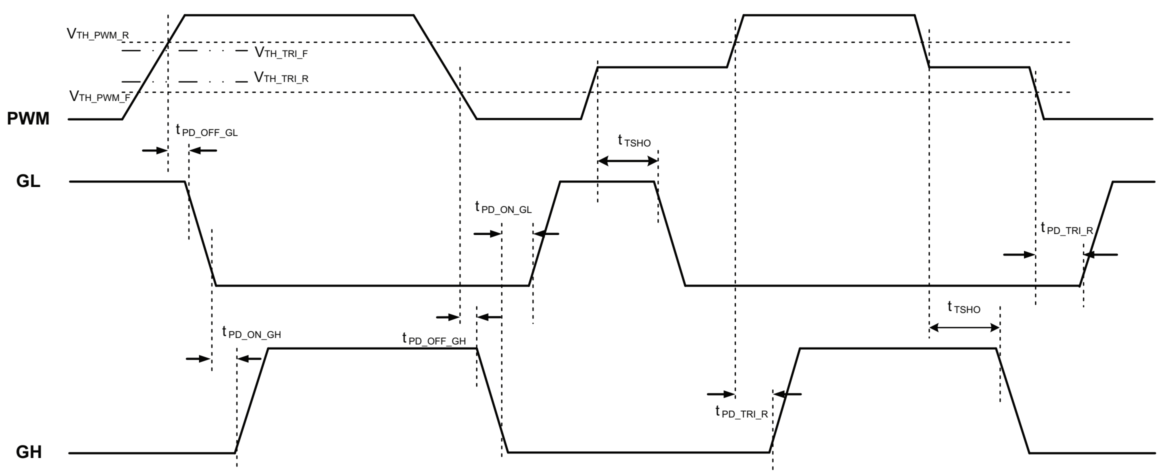

Fig. 4 - Definition of PWM Logic and Tri-State

DSBL# PROPAGATION DELAY

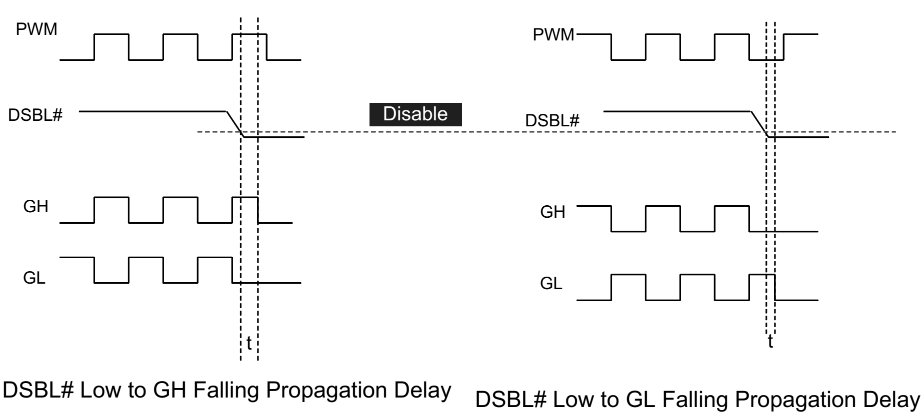

Fig. 5 - DSBL# Falling Propagation Delay

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ELECTRICAL CHARACTERISTICS

(Test condition: V_{IN} = 12 V, V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1.8 V, L_{OUT} = 250 nH (DCR = 0.32 mΩ), T_A = 25 °C, natural convection cooling)
(All power loss and normalized power loss curves show SiC620 and SiC620A losses only unless otherwise stated))

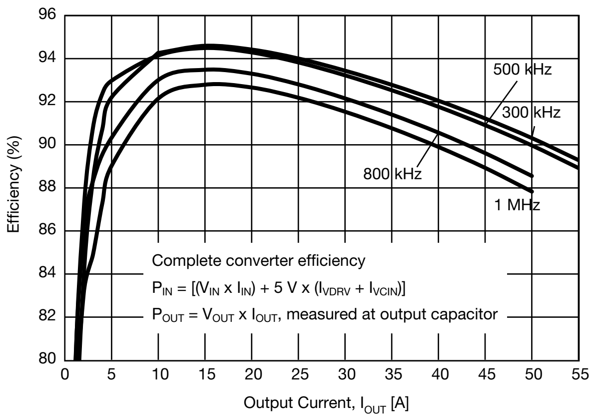

Fig. 6 - Efficiency vs. Output Current

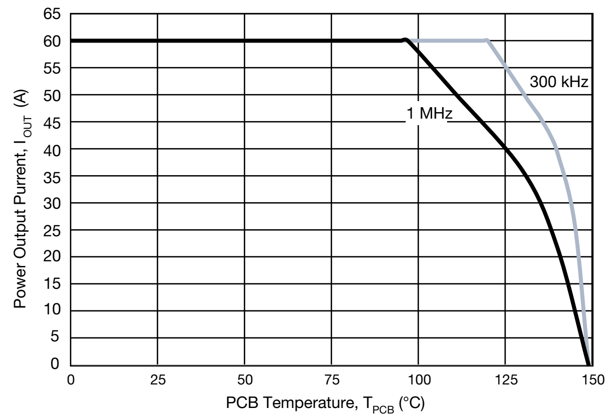

Fig. 9 - Safe Operating Area

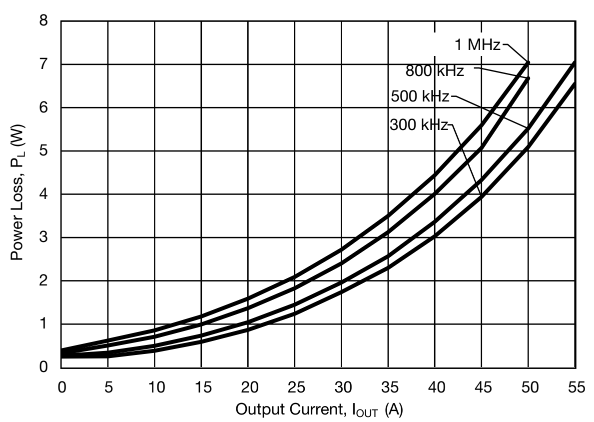

Fig. 7 - Power Loss vs. Output Current

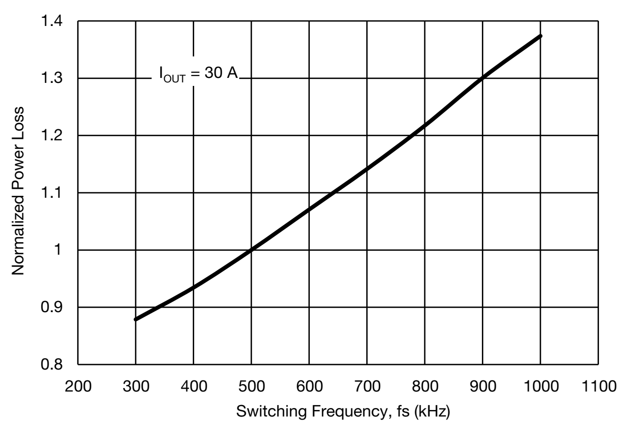

Fig. 10 - Power Loss vs. Switching Frequency

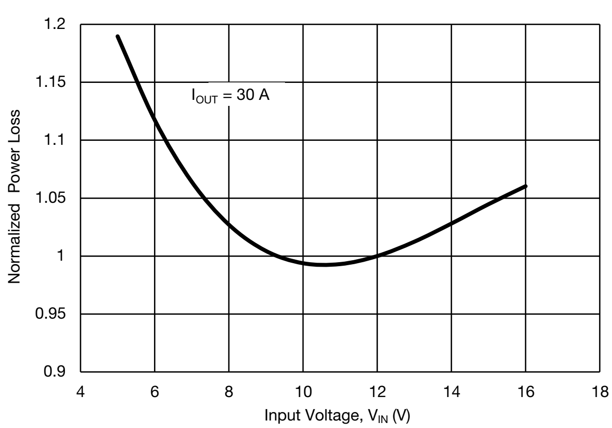

Fig. 8 - Power Loss vs. Input Voltage

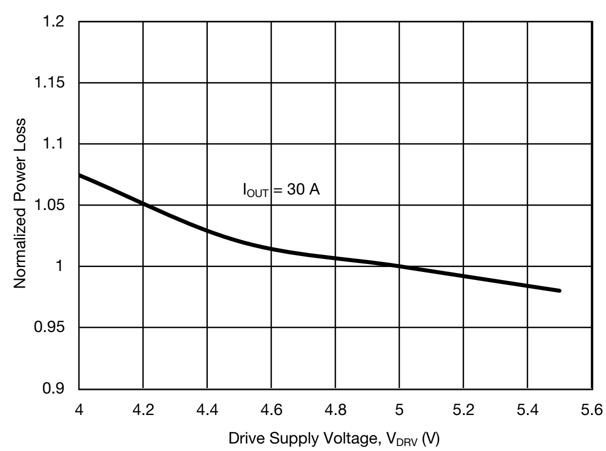

Fig. 11 - Power Loss vs. Drive Supply Voltage

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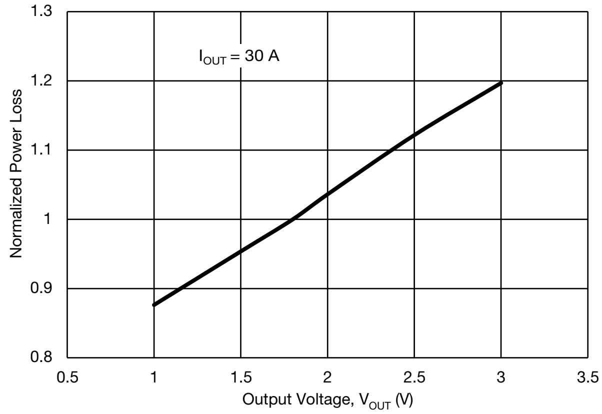

Fig. 12 - Power Loss vs. Output Voltage

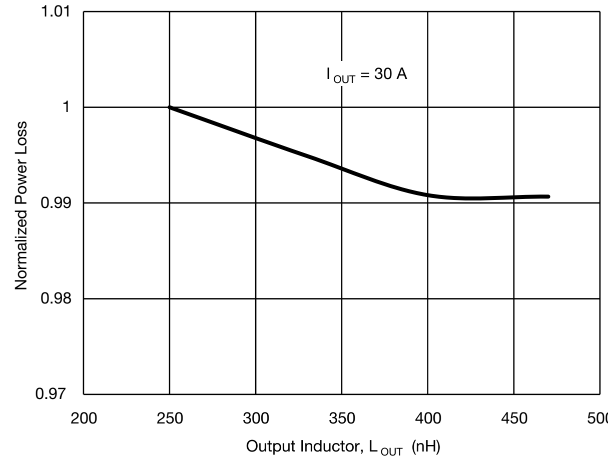

Fig. 15 - Power Loss vs. Output Inductor

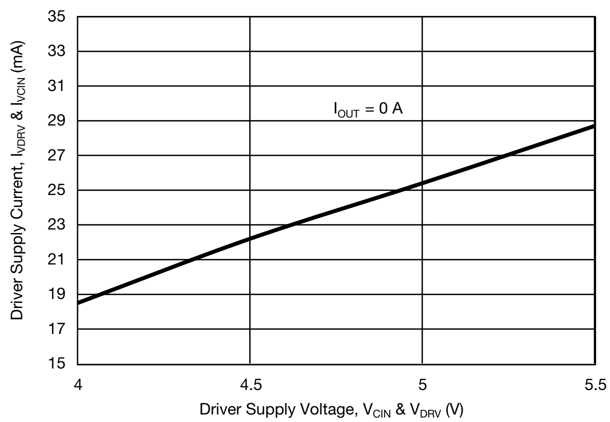

Fig. 13 - Driver Supply Current vs. Driver Supply Voltage

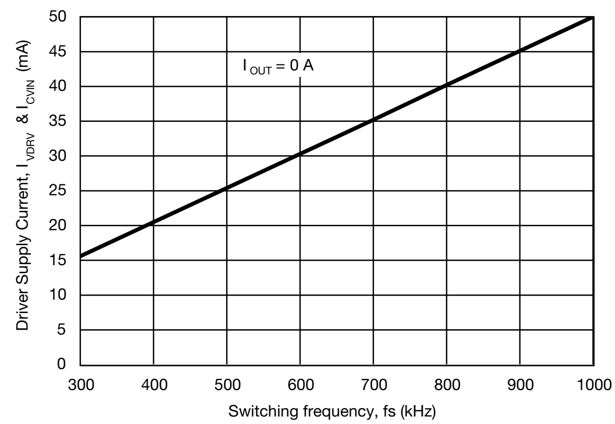

Fig. 16 - Driver Supply Current vs. Switching Frequency

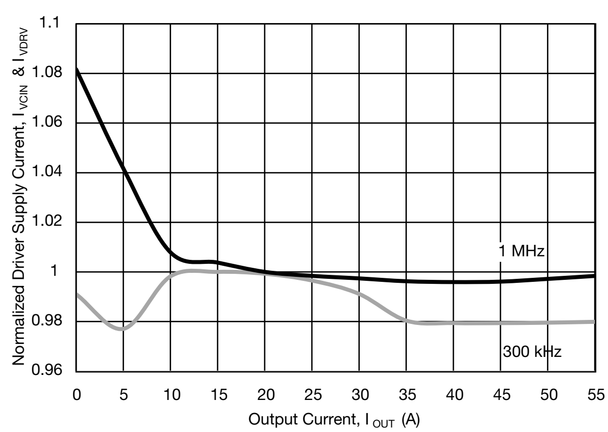

Fig. 14 - Driver Supply Current vs. Output Current

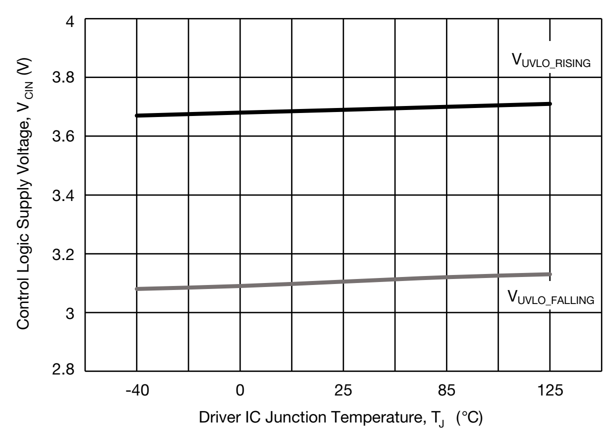

Fig. 17 - UVLO Threshold vs. Temperature

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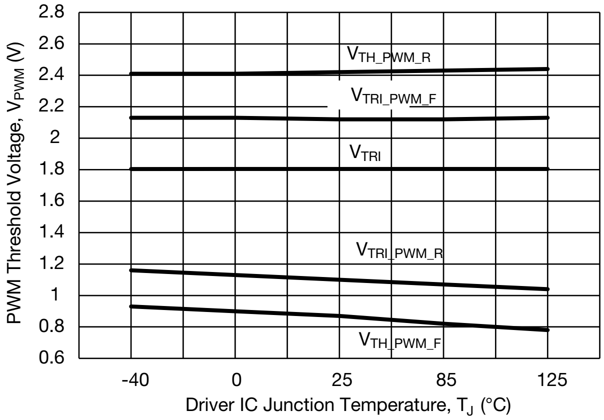

Fig. 18 - PWM Threshold vs. Temperature (SiC620A)

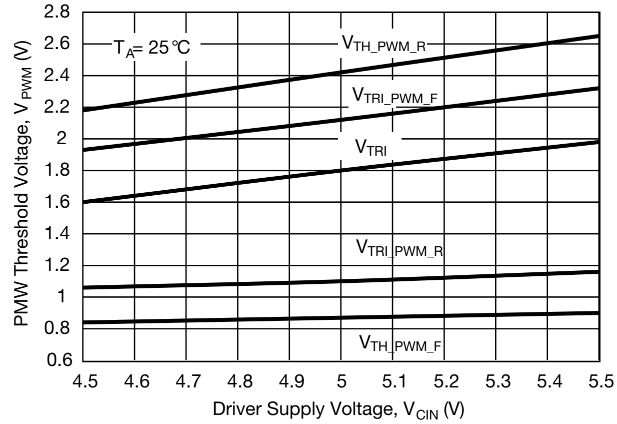

Fig. 21 - PWM Threshold vs. Driver Supply Voltage (SiC620A)

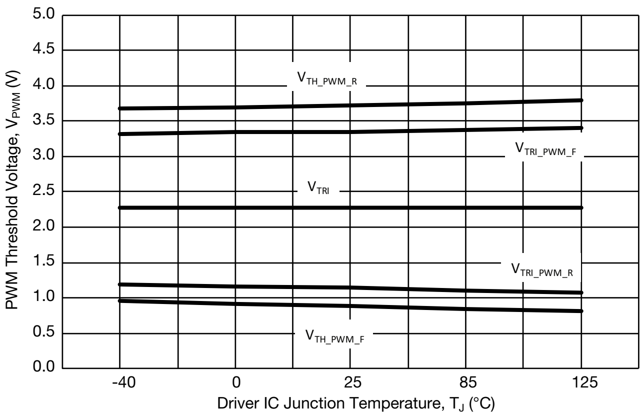

Fig. 19 - PWM Threshold vs. Temperature (SiC620)

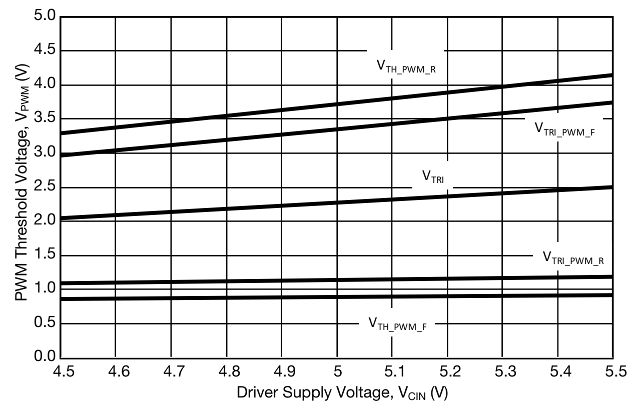

Fig. 22 - PWM Threshold vs. Driver Supply Voltage (SiC620)

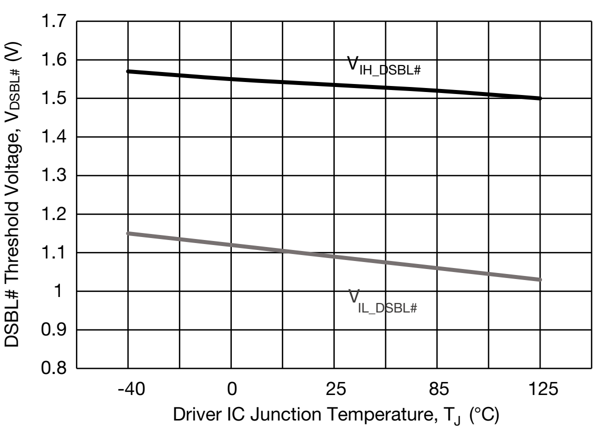

Fig. 20 - DSBL# Threshold vs. Temperature

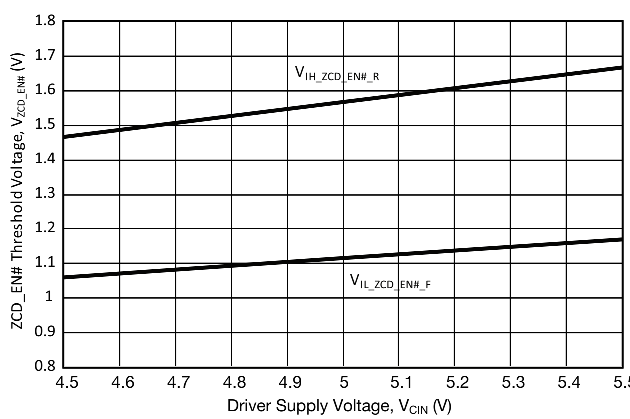

Fig. 23 - ZCD_EN# Threshold vs. Driver Supply Voltage

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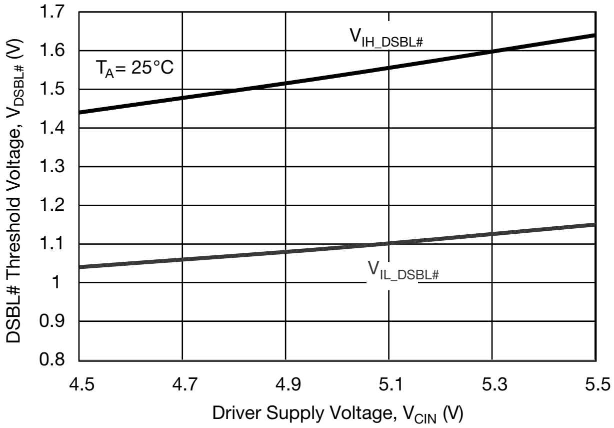

Fig. 24 - DSBL# vs. Driver Input Voltage

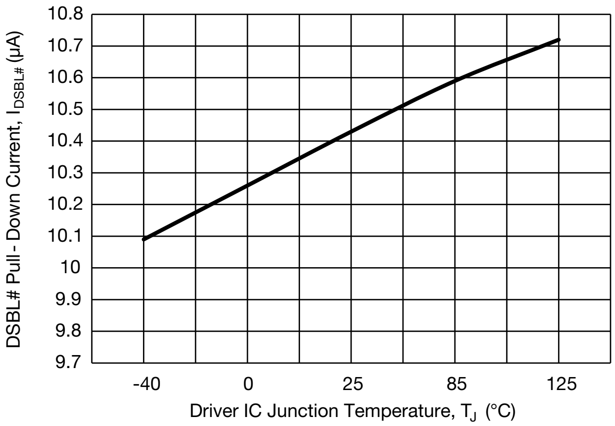

Fig. 25 - DSBL# Pull-Down Current vs. Temperature

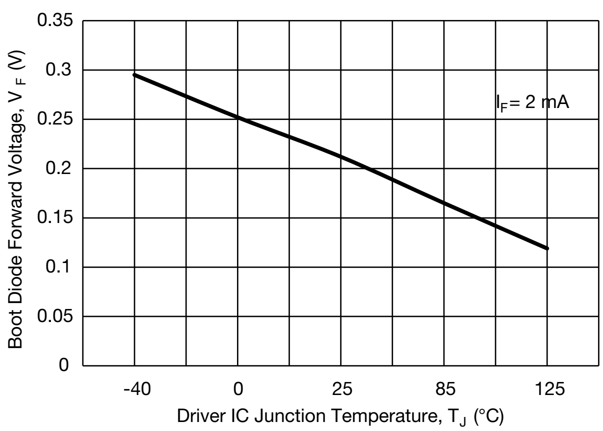

Fig. 26 - Boot Diode Forward Voltage vs. Temperature

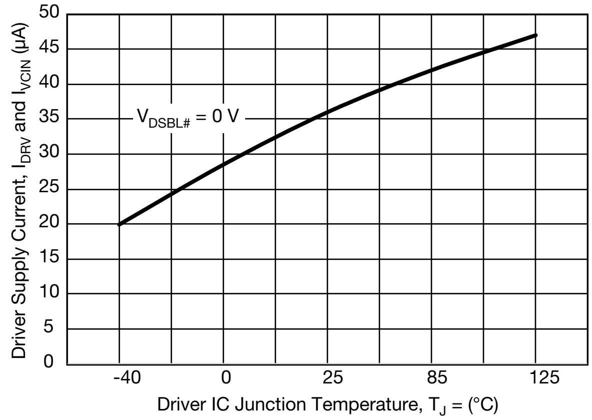

Fig. 27 - Driver Shutdown Current vs. Temperature

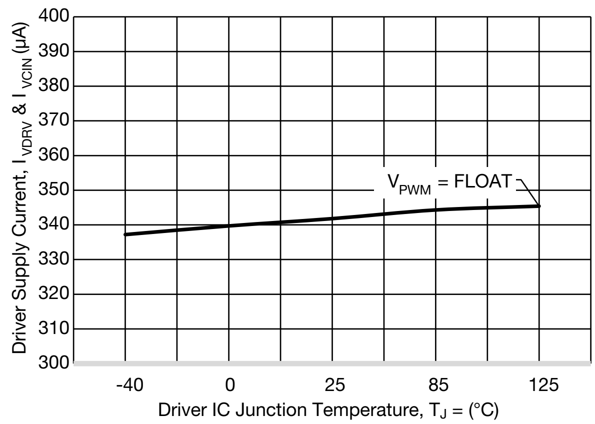

Fig. 28 - Driver Supply Current vs. Temperature

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PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling

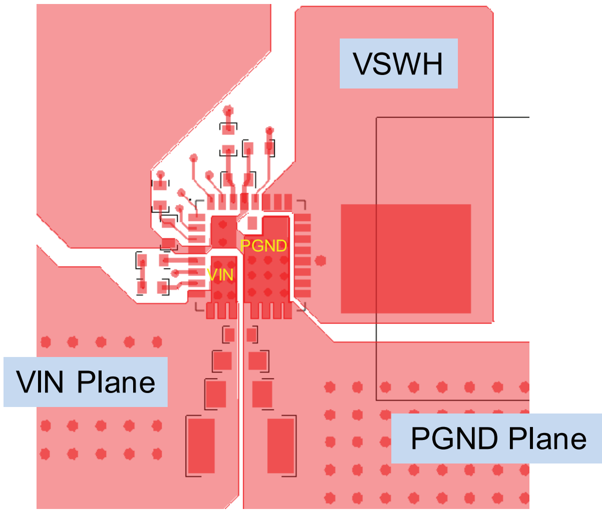

Fig. 29

1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210 + 0805 + 0603 + 0402
4. Smaller capacitance value, closer to device V_{IN} pin(s) - better high frequency noise absorbing

Step 2: V_{SWH} Plane

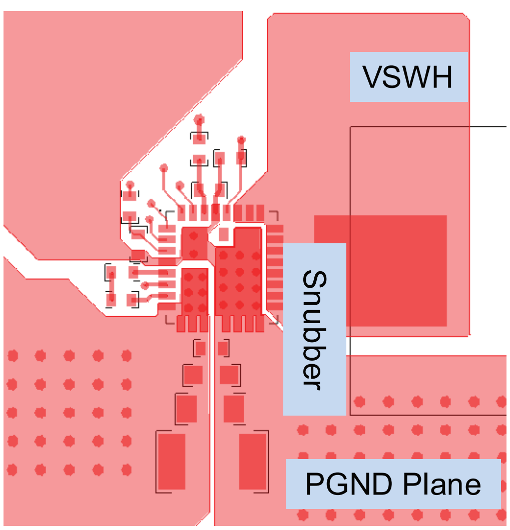

Fig. 30

1. Connect output inductor to DrMOS with large plane to lower the resistance
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

Step 3: V_{CIN}/V_{DRV} Input Filter

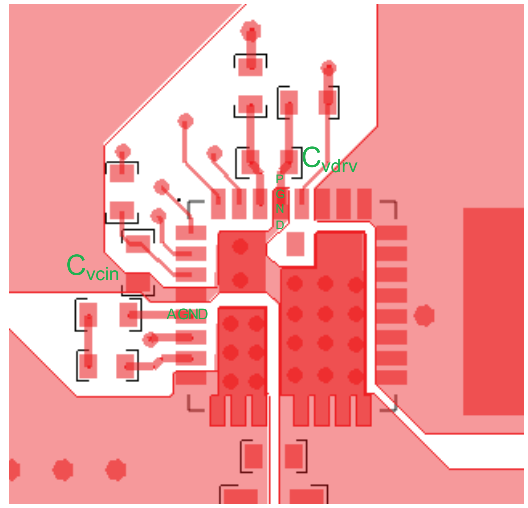

Fig. 31

1. The V_{CIN}/V_{DRV} input filter ceramic cap should be placed very close to DrMOS. It is recommended to connect two caps separately.
2. C_{VCIN} cap should be placed between pin 3 and pin 4 (A_{GND} of driver IC) to achieve best noise filtering.
3. C_{VDRV} cap should be placed between pin 28 (P_{GND} of driver IC) and pin 29 to provide maximum instantaneous driver current for low-side MOSFET during switching cycle
4. For connecting C_{VCIN} analog ground, it is recommended to use large plane to reduce parasitic inductance.

Step 4: BOOT Resistor and Capacitor Placement

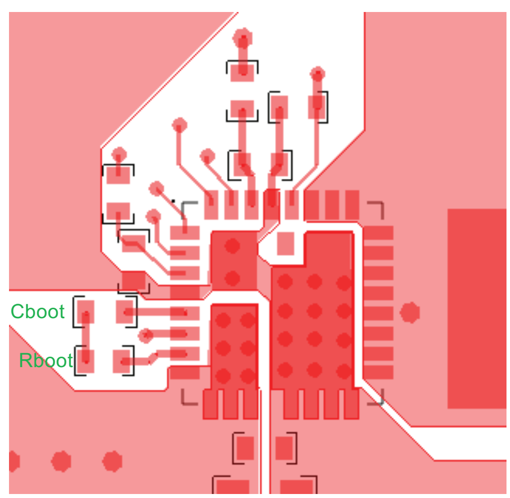

Fig. 32

1. These components need to be placed very close to DrMOS, right between PHASE (pin 7) and BOOT (pin 5).
2. To reduce parasitic inductance, chip size 0402 can be used.

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Step 5: Signal Routing

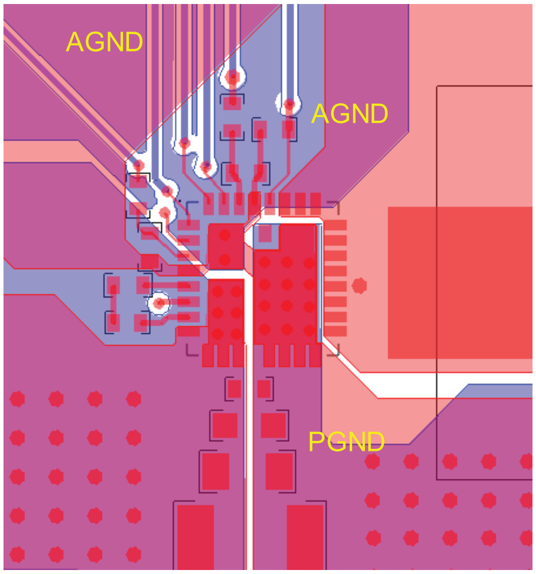

Fig. 33

1. Route the PWM / ZCD_EN# / DSBL# / THWn signal traces out of the top left corner next DrMOS pin 1.
2. PWM signal is very important signal, both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer.
3. It is best to "shield" them with GND island form power switching nodes, e.g. V_{SWH}, to improve signal integrity.
4. GL (pin 27) has been connected with GL pad internally and does not need to connect externally.

Step 6: Adding Thermal Relief Vias

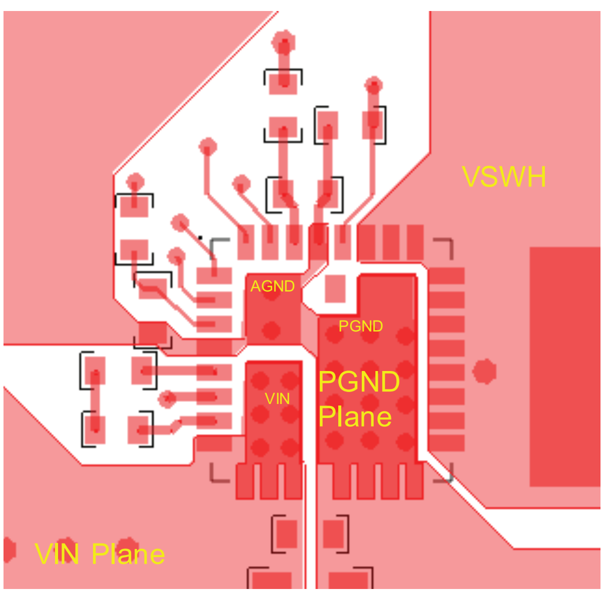

Fig. 34

1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high-current and thermal dissipation.
2. To achieve better thermal performance, additional vias can be put on V_{IN} plane and P_{GND} plane.
3. V_{SWH} pad is a noise source and not recommended to put vias on this plane.
4. 8 mil drill for pads and 10 mils drill for plane can be the optional via size. The vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline.

Step 7: Ground Connection

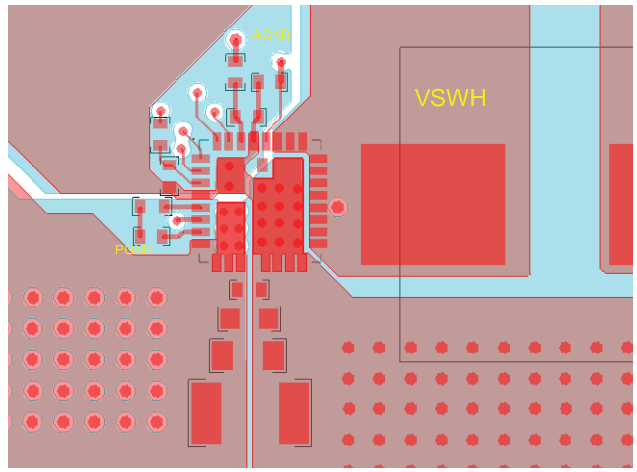

Fig. 35

1. It is recommended to make single connection between A_{GND} and P_{GND} and this connection can be done on top layer.
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into A_{GND} and P_{GND} plane.
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer.

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Multi-Phases VRPower PCB Layout

Following is an example for 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling caps next to them. The inductors are placed as close as possible to the SiC620 and SiC620A to minimize the PCB copper loss. Vias are applied on all PADs (V_{IN} P_{GND}, A_{GND}) of the SiC620 and SiC620A to ensure that both electrical and thermal performance are excellent. Large copper planes are used for all the high current loops, such as V_{IN}, V_{SWH}, V_{OUT} and P_{GND}. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC620 and SiC620A to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

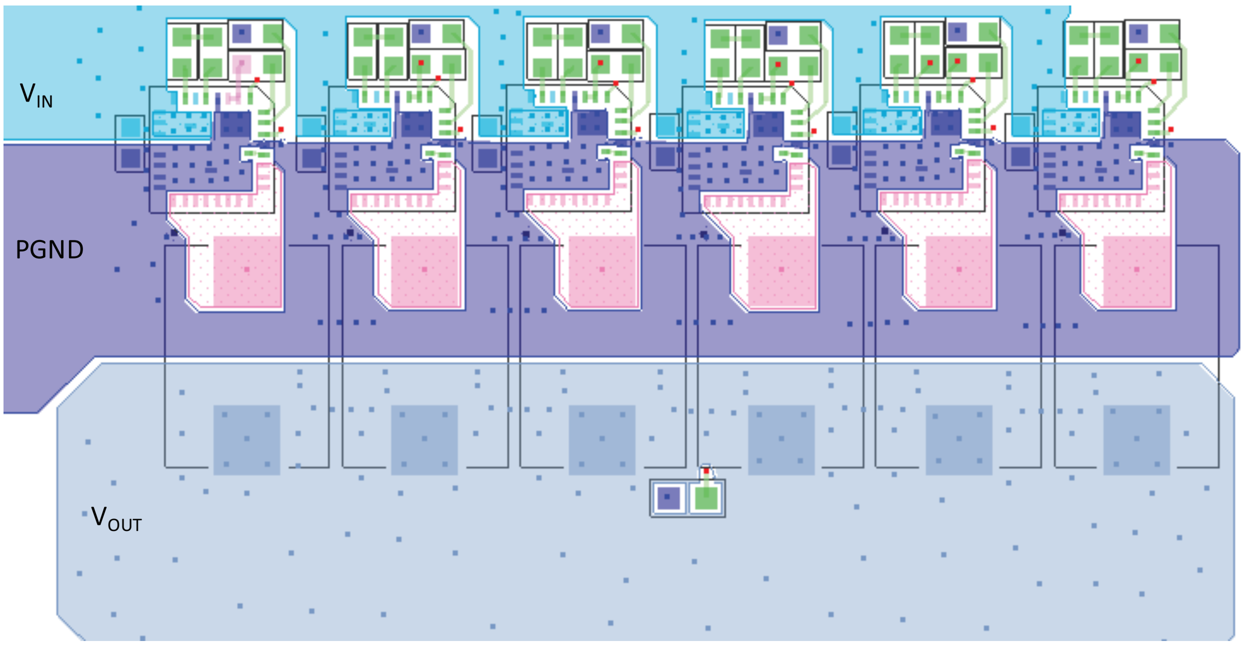

Fig. 36 - Multi - Phase VRPower (R) Layout Top View

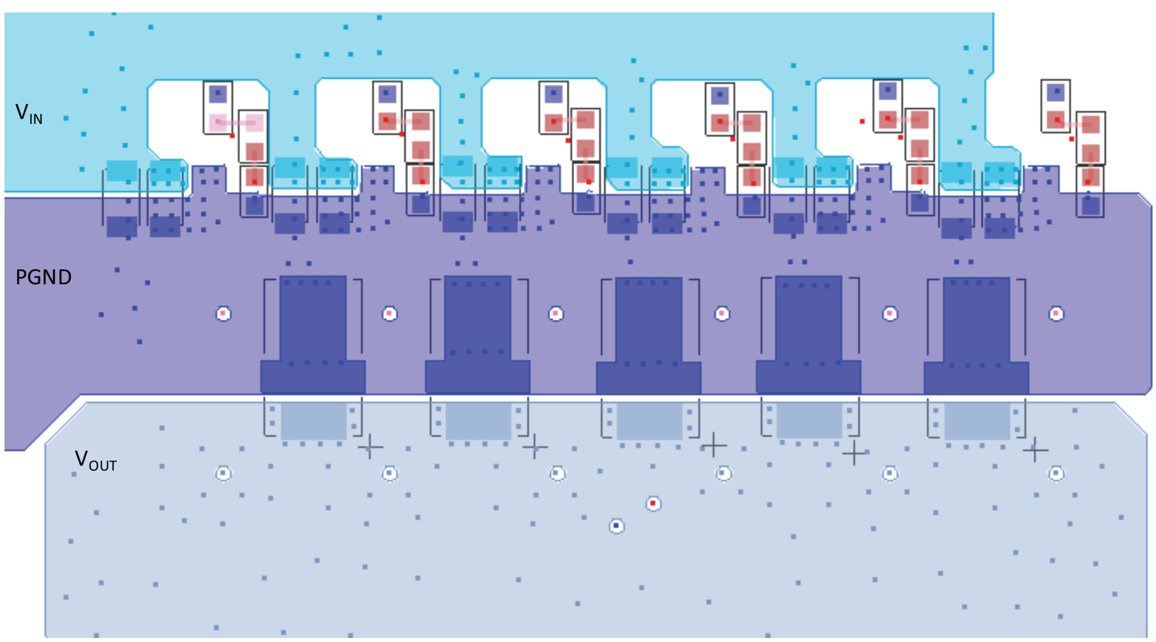

Fig. 37 - Multi - Phase VRPower Layout Bottom View

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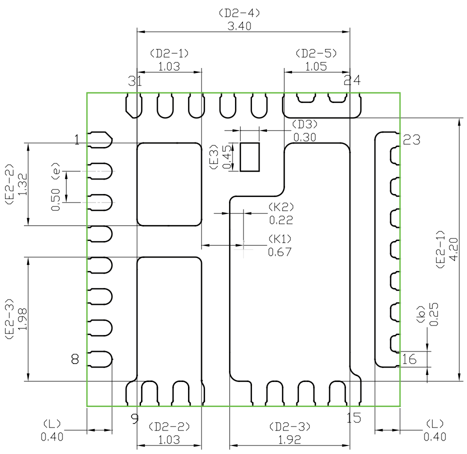
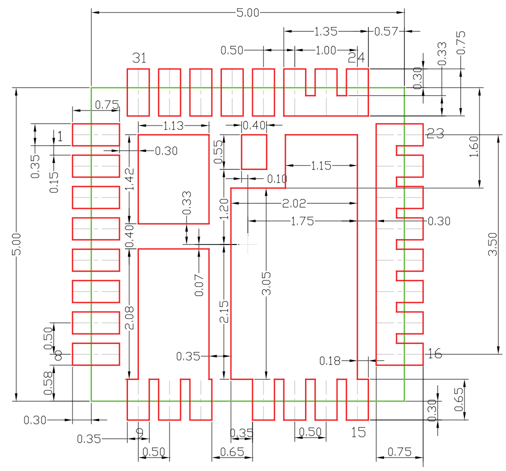
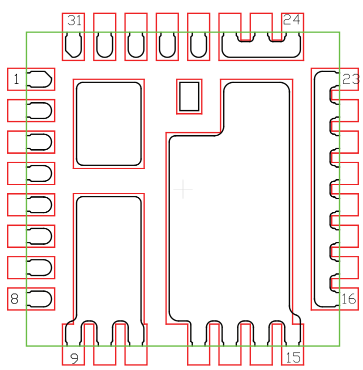
RECOMMENDED LAND PATTERN POWERPAK® MLP55-31L

Package Outline Bottom View



Land Pattern for MLP55-31L





All dimensions in mm

Fig. 38 - MLP55-31L Land Pattern

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PACKAGE OUTLINE DRAWING

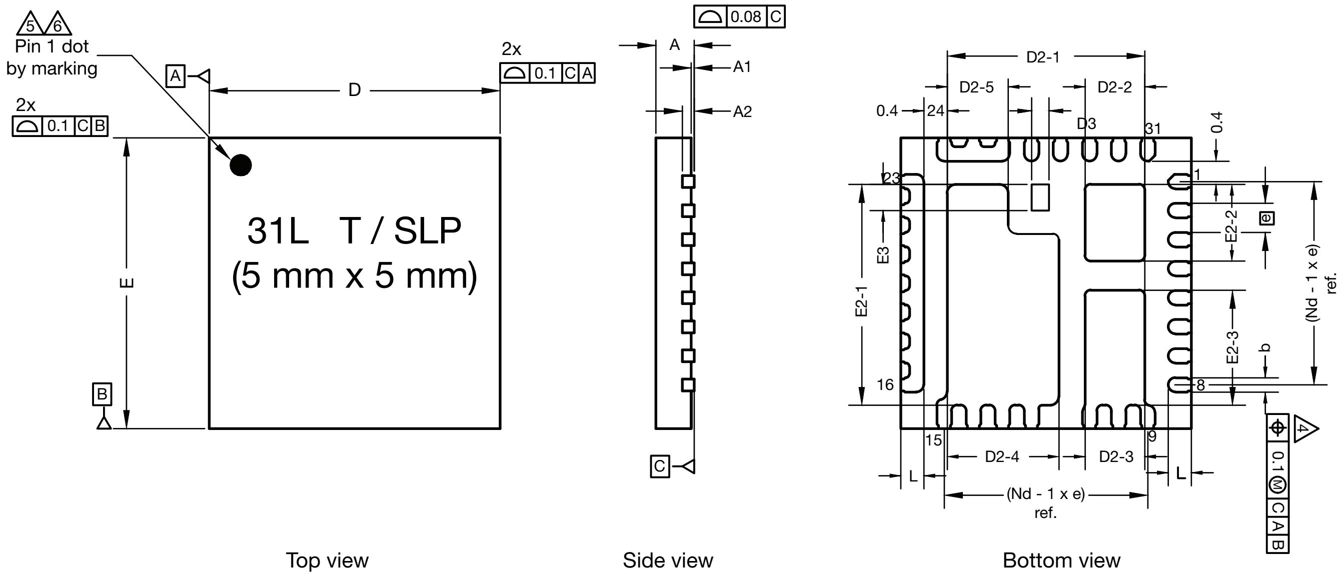

Fig. 39 - MLP55-31L Package Outline Drawing

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b	0.20	0.25	0.30	0.078	0.098	0.110
D		5.00 BSC			0.196 BSC	
e		0.50 BSC			0.019 BSC	
E		5.00 BSC			0.196 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N		32			32	
Nd		8			8	
Ne		8			8	
D2-1	3.35	3.40	3.45	0.132	0.134	0.136
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	0.98	1.03	1.08	0.039	0.041	0.043
D2-4	1.87	1.92	1.97	0.074	0.076	0.078
D2-5	1.00	1.05	1.10	0.039	0.041	0.043
D3		0.30 BSC			0.012 BSC	
E2-1	3.75	3.80	3.85	0.148	0.150	0.152
E2-2	1.27	1.32	1.37	0.050	0.052	0.054
E2-3	1.93	1.98	2.03	0.076	0.078	0.080
E3		0.45 BSC			0.018 BSC	

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