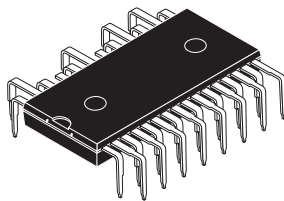
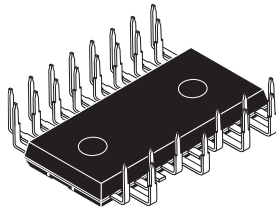


SLLIMM-nano IPM, 3 A, 600 V, 3-phase inverter bridge IGBT



NDIP-26L



Product status link

[STGIPN3H60A](#)

Product summary

Order code	STGIPN3H60A
Marking	GIPN3H60A
Package	NDIP-26L
Packing	Tube

Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interferences
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL input comparators with hysteresis and pull-down/pull-up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Optimized pinout for easy board layout

Applications

- 3-phase induction motor (ACIM)
- Dishwasher
- Fans
- PMSM / BLDC motor control
- Refrigerators and freezers

Description

This intelligent power module implements a compact, high performance AC motor drive in a simple, rugged design. It is composed of six IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit.

1 Internal schematic diagram and pin configuration

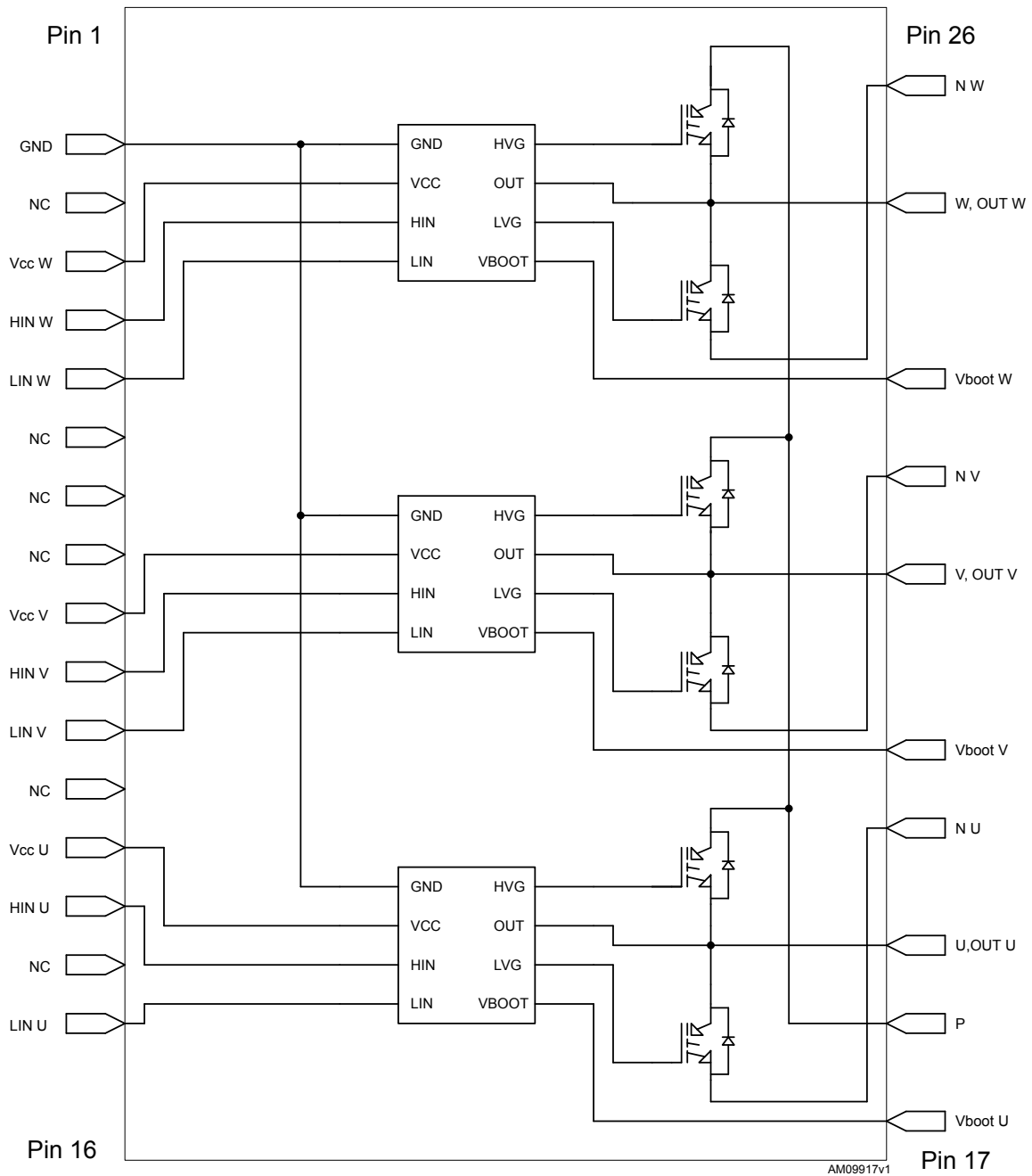
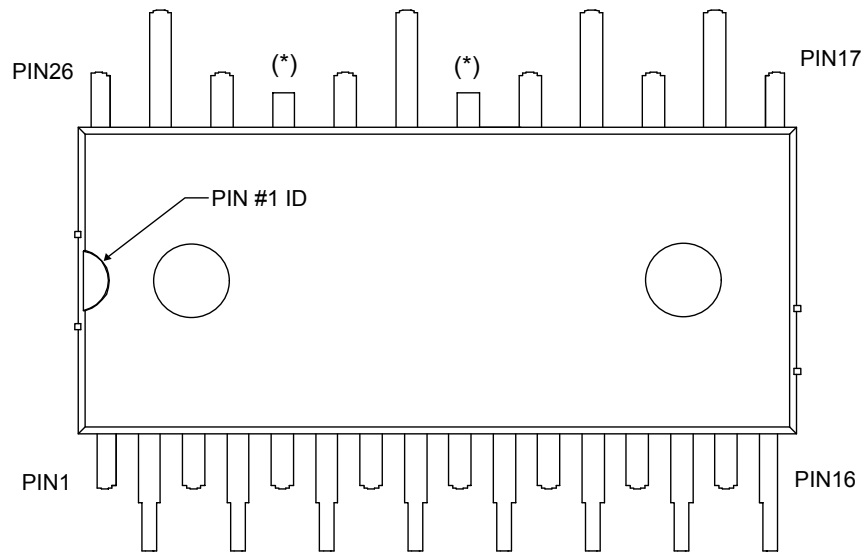
Figure 1. Internal schematic diagram


Table 1. Pin description

Pin	Symbol	Description
1	GND	Ground
2	NC	Not connected
3	V _{CC} W	Low voltage power supply W phase
4	HIN W	High side logic input for W phase
5	LIN W	Low side logic input for W phase
6	NC	Not connected
7	NC	Not connected
8	NC	Not connected
9	V _{CC} V	Low voltage power supply V phase
10	HIN V	High side logic input for V phase
11	LIN V	Low side logic input for V phase
12	NC	Not connected
13	V _{CC} U	Low voltage power supply for U phase
14	HIN U	High side logic input for U phase
15	NC	Not connected
16	LIN U	Low side logic input for U phase
17	V _{BOOT} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U	U phase output
20	N _U	Negative DC input for U phase
21	V _{BOOT} V	Bootstrap voltage for V phase
22	V	V phase output
23	N _V	Negative DC input for V phase
24	V _{BOOT} W	Bootstrap voltage for W phase
25	W	W phase output
26	N _W	Negative DC input for W phase

Figure 2. Pin layout (top view)



(*) Dummy pin internally connected to P (positive DC input).

AM09368V1

2 Electrical ratings

2.1 Absolute maximum ratings

Table 2. Inverter part

Symbol	Parameter	Value	Unit
V_{CES}	Each IGBT collector emitter voltage ($V_{IN}^{(1)} = 0$)	600	V
$\pm I_C$	Continuous collector current each IGBT ($T_C = 25\text{ °C}$)	3	A
$\pm I_{CP}^{(2)}$	Pulsed collector current each IGBT (less than 1 ms)	18	A
P_{TOT}	Total power dissipation each IGBT ($T_C = 25\text{ °C}$)	8	W

1. Applied between HIN_i , \overline{LIN}_i and G_{ND} for $i = U, V, W$.
2. Pulse width limited by max. junction temperature.

Table 3. Control part

Symbol	Parameter	Min.	Max.	Unit
V_{OUT}	Output voltage applied between OUT_U , OUT_V , OUT_W - GND	$V_{boot} - 18$	$V_{boot} + 0.3$	V
V_{CC}	Low voltage power supply	- 0.3	18	V
V_{boot}	Bootstrap voltage	- 0.3	618	V
V_{IN}	Logic input voltage applied among HIN , \overline{LIN} and GND	- 0.3	15	V
$\Delta V_{OUT/dT}$	Allowed output slew rate		50	V/ns

Table 4. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, $t = 60\text{ s}$)	1000	Vrms
T_J	Power chip operating junction temperature range	-40 to 150	°C
T_C	Operating case temperature range	-40 to 125	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case single IGBT	12.8	°C/W
	Thermal resistance, junction-to-case single diode	15.5	
R_{thJA}	Thermal resistance, junction-to-ambient per module	22	°C/W

3 Electrical characteristics

3.1 Inverter part

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 6. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$, $I_C = 1\text{ A}$	-	2.15	2.6	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$, $I_C = 1\text{ A}$, $T_J = 125\text{ °C}$	-	1.65		
I_{CES}	Collector cut-off current ($V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 550\text{ V}$, $V_{CC} = 15\text{ V}$, $V_{BS} = 15\text{ V}$	-		250	μA
V_F	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 1\text{ A}$	-		1.7	V

1. Applied between HIN_i , LIN_i and GND for $i = U, V, W$ (LIN inputs are active low).

Table 7. Inductive load switching time and energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{on}^{(1)}$	Turn-on time	$V_{DD} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(2)} = 0\text{ to }5\text{ V}$, $I_C = 1\text{ A}$ (see Figure 4. Switching time definition)	-	275	-	ns
$t_{c(on)}^{(1)}$	Crossover time (on)		-	90	-	
$t_{off}^{(1)}$	Turn-off time		-	890	-	
$t_{c(off)}^{(1)}$	Crossover time (off)		-	125	-	
t_{rr}	Reverse recovery time		-	50	-	
E_{on}	Turn-on switching energy		-	18	-	μJ
E_{off}	Turn-off switching energy		-	13	-	

1. t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving conditions.

2. Applied between HIN_i , \overline{LIN}_i and GND for $i = U, V, W$ (LIN inputs are active low).

Figure 3. Switching time test circuit

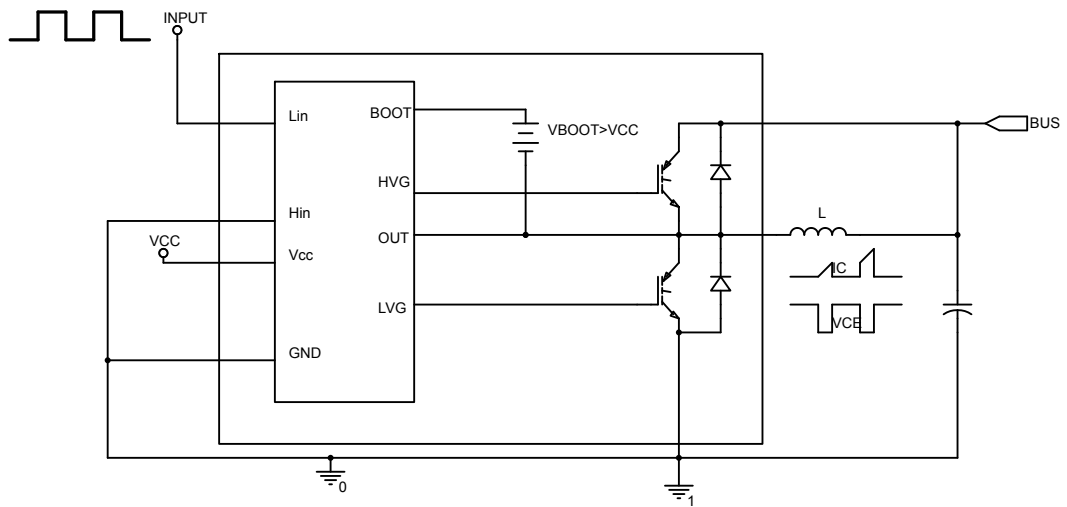
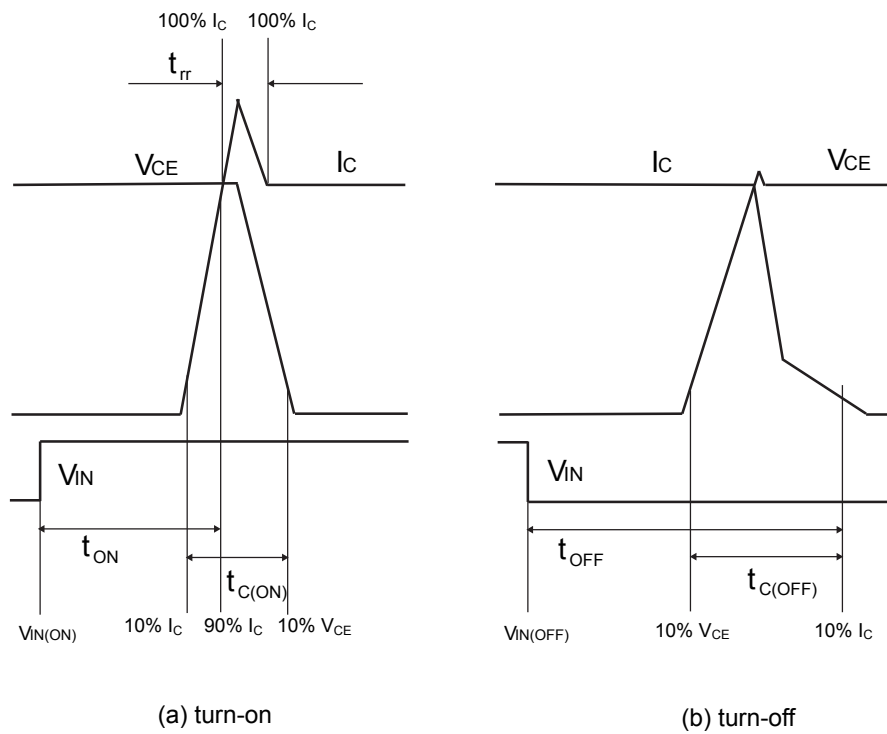


Figure 4. Switching time definition



AM09223V1

Figure 4. Switching time definition refers to HIN inputs (active high). For $\overline{\text{LIN}}$ inputs (active low), VIN polarity must be inverted for turn-on and turn-off.

3.2 Control part

($V_{CC} = 15\text{ V}$ unless otherwise specified).

Table 8. Low voltage power supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC_hys}	V_{CC} UV hysteresis		0.9			V
V_{CC_thON}	V_{CC} UV turn-ON threshold		9.1	9.6	10.1	V
V_{CC_thOFF}	V_{CC} UV turn-OFF threshold		7.9	8.3	8.8	V
I_{qccu}	Undervoltage quiescent supply current	$V_{CC} = 15\text{ V}$, $\overline{SD}/OD = 5\text{ V}$, $\overline{LIN} = 5\text{ V}$, $HIN = 0\text{ V}$, $CIN = 0\text{ V}$		250	330	μA
I_{qcc}	Quiescent current	$V_{CC} = 15\text{ V}$, $\overline{SD}/OD = 5\text{ V}$, $\overline{LIN} = 5\text{ V}$, $HIN = 0\text{ V}$, $CIN = 0\text{ V}$		350	450	mA

Table 9. Bootstrapped voltage

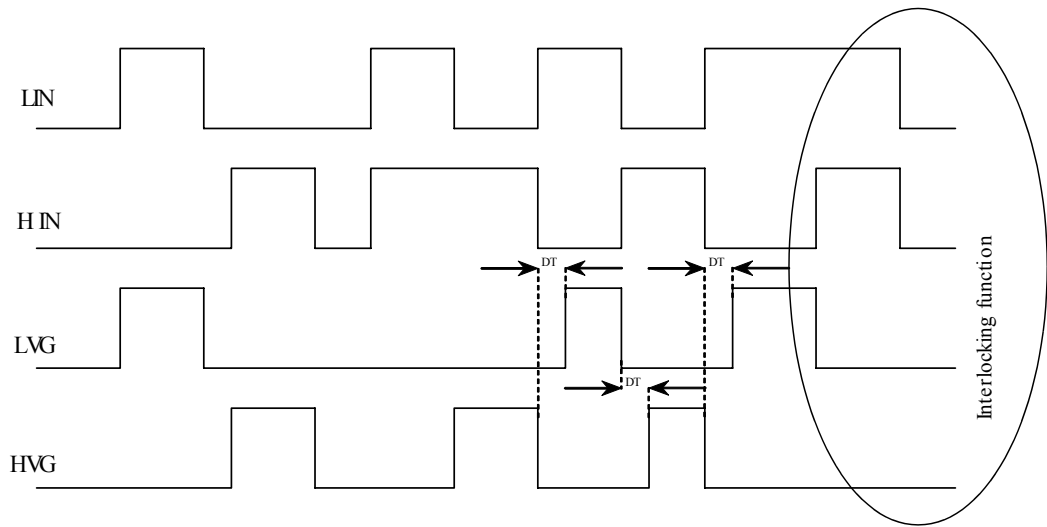
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{boot_thON}	Undervoltage turn-on threshold		8.5	9.5	10.5	V
V_{boot_thOFF}	Undervoltage turn-off threshold		7.2	8.3	9.2	V
V_{boot_hys}	Undervoltage hystereses		0.9			V
I_{qboot}	Quiescent current				250	μA
$R_{DS(on)}$	Bootstrap driver on-resistance	$V_{CC} > 12.5\text{ V}$		125		Ω

Table 10. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				1.1	V
V_{ih}	High logic level voltage		1.8			V
I_{il}	HIN logic "1" input bias current ⁽¹⁾	$HIN = 0\text{ V}$ ⁽¹⁾	-1			μA
I_{ih}	HIN logic "0" input bias current ⁽¹⁾	$HIN = 15\text{ V}$ ⁽¹⁾		20	70	μA
Dt	Dead time	see Figure 5. Dead time and interlocking definition		320		ns

1. Applied between HIN_i , LIN_i and GND for $i = U, V, W$

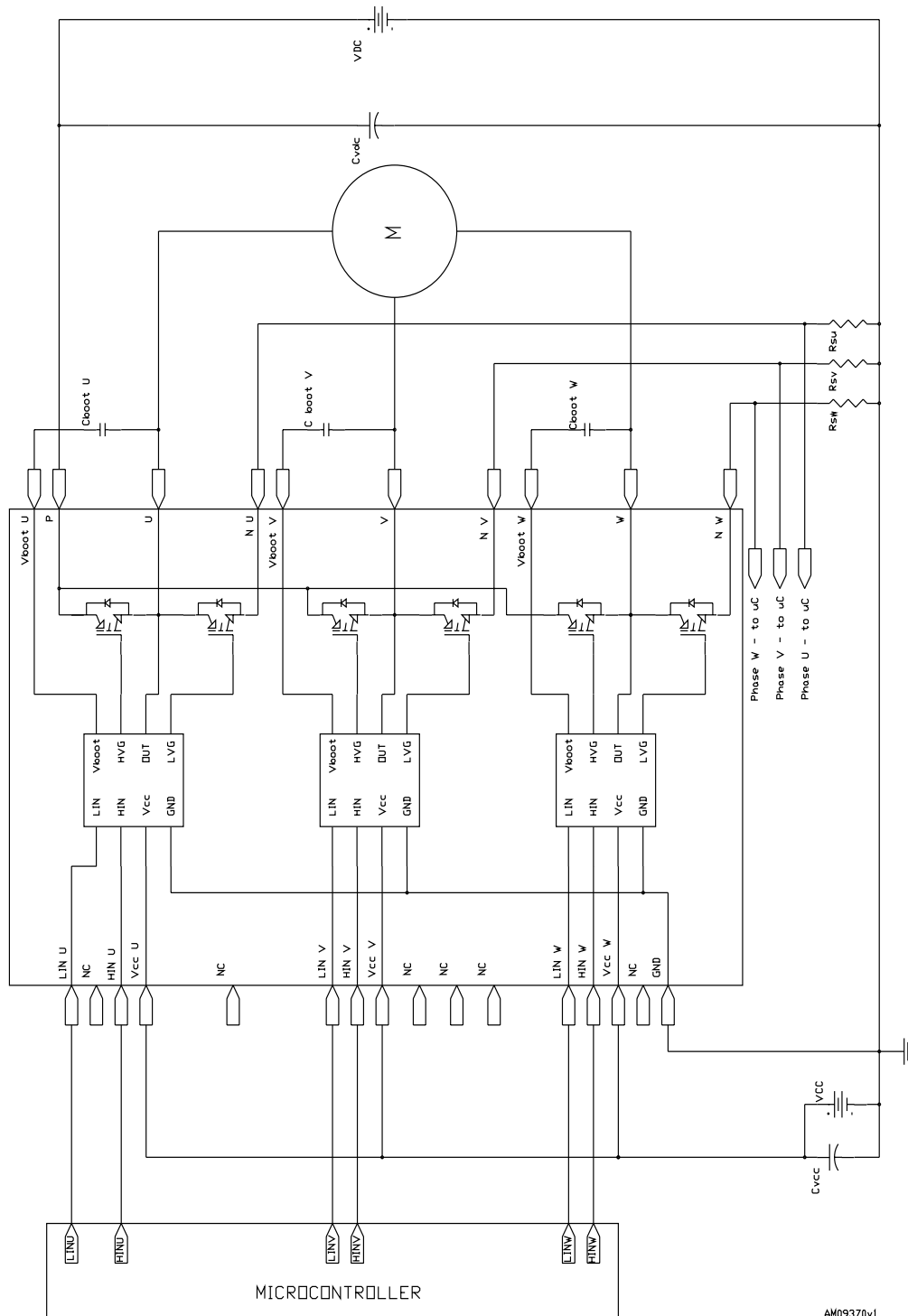
Figure 5. Dead time and interlocking definition



AM03794v1

4 Application circuit example

Figure 6. Application circuit example



AM09370v1

Application designers are free to use a different scheme according to the specifications of the device.

4.1 Guidelines

- Input signals HIN, LIN are active-high logic. A 500 k Ω (typ.) pull-down resistor is built-in for each input. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is suggested. The filters should be done with a time constant of about 100ns and must be placed as close as possible to the IPM input pins.
- The bypass capacitor C_{vcc} (aluminum or tantalum) is recommended to reduce the transient circuit demand on the power supply. In addition, a decoupling capacitor C2 (from 100 to 220 nF, ceramic with low ESR) is suggested, to reduce high frequency switching noise distributed on the power supply lines. It must be placed as close as possible to each V_{cc} pin and in parallel to the bypass capacitor.
- The use of RC filter (RSF, CSF) for current monitoring is recommended to improve noise immunity. The filter must be placed as close as possible to the microcontroller or to the Op-amp.
- The decoupling capacitor C3 (from 100 to 220 nF, ceramic with low ESR), in parallel to each C_{boot}, is recommended in order to filter high frequency disturbances.
- The Zener diodes DZ1 between the V_{cc} pins and GND and in parallel to each C_{boot} is suggested in order to prevent overvoltage.
- The decoupling capacitor C4 (from 100 to 220 nF, ceramic with low ESR) in parallel to the electrolytic capacitor C_{vdc} is recommended, in order to prevent surge destruction. Both capacitors C4 and C_{vdc} should be placed as close as possible to the IPM (C4 has priority over C_{vdc}).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- In order to avoid malfunctions, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
- It is recommended to connect SGN_GND to PWR_GND at only one point (near the terminal of shunt resistor), in order to avoid any malfunction due to power ground fluctuation.

These guidelines ensure the specifications of the device for application designs. For further details, please refer to the relevant application note AN4043.

Table 11. Recommended operating conditions

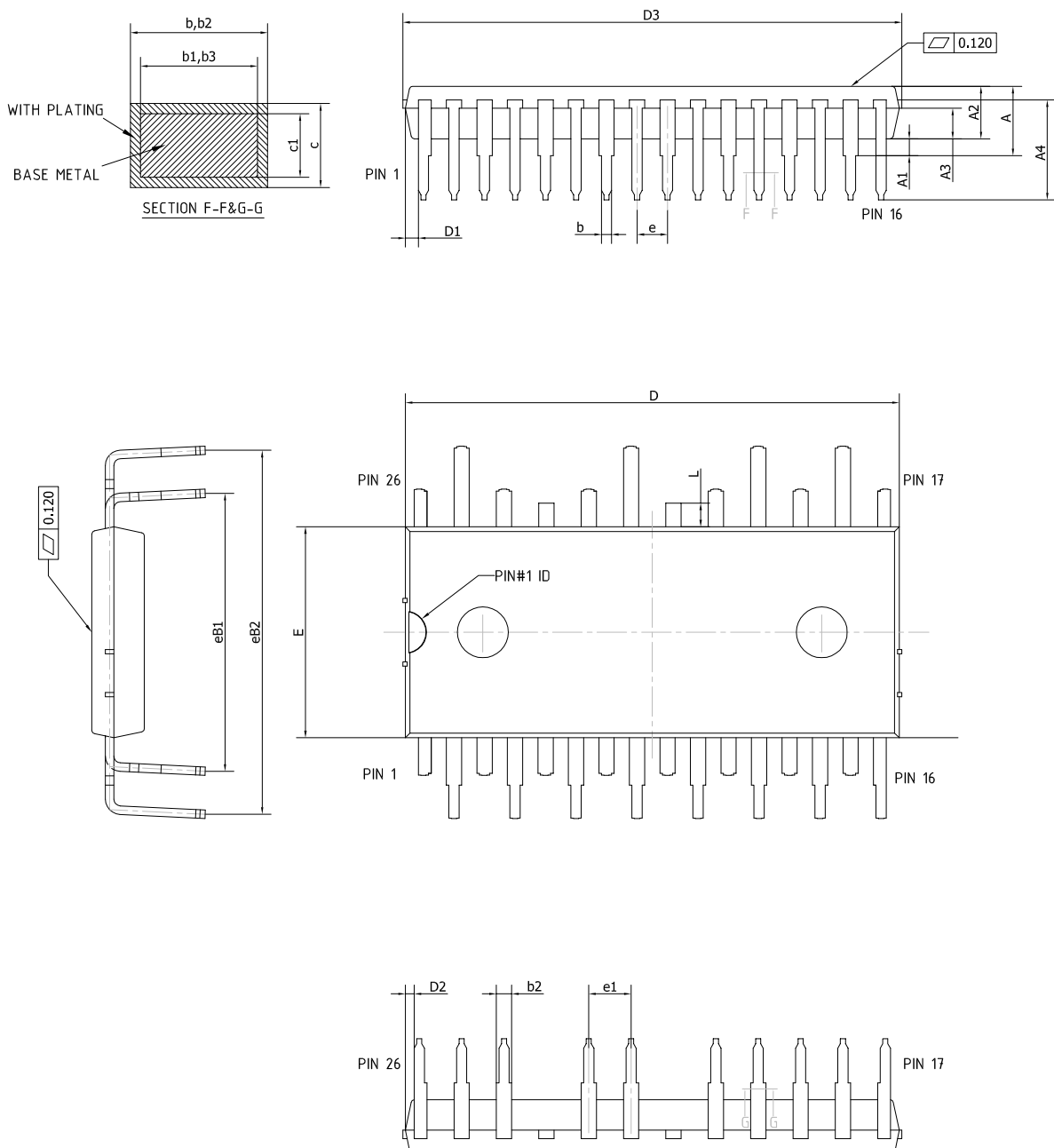
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{PN}	Supply voltage	Applied between P-Nu, Nv, Nw		300	500	V
V _{CC}	Control supply voltage	Applied between V _{CC} -GND	12	15	17	V
V _{BS}	High-side bias voltage	Applied between V _{BOOTi} -OUT _i for i = U, V, W	11.5		17	V
t _{dead}	Blanking time to avoid arm-short	For each input signal	1.5			μ s
f _{PWM}	PWM input signal	-40 °C < T _C < 100 °C -40 °C < T _J < 125 °C			25	kHz
T _C	Operating case temperature				100	°C

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 NDIP-26L type C package information

Figure 7. NDIP-26L type C package outline



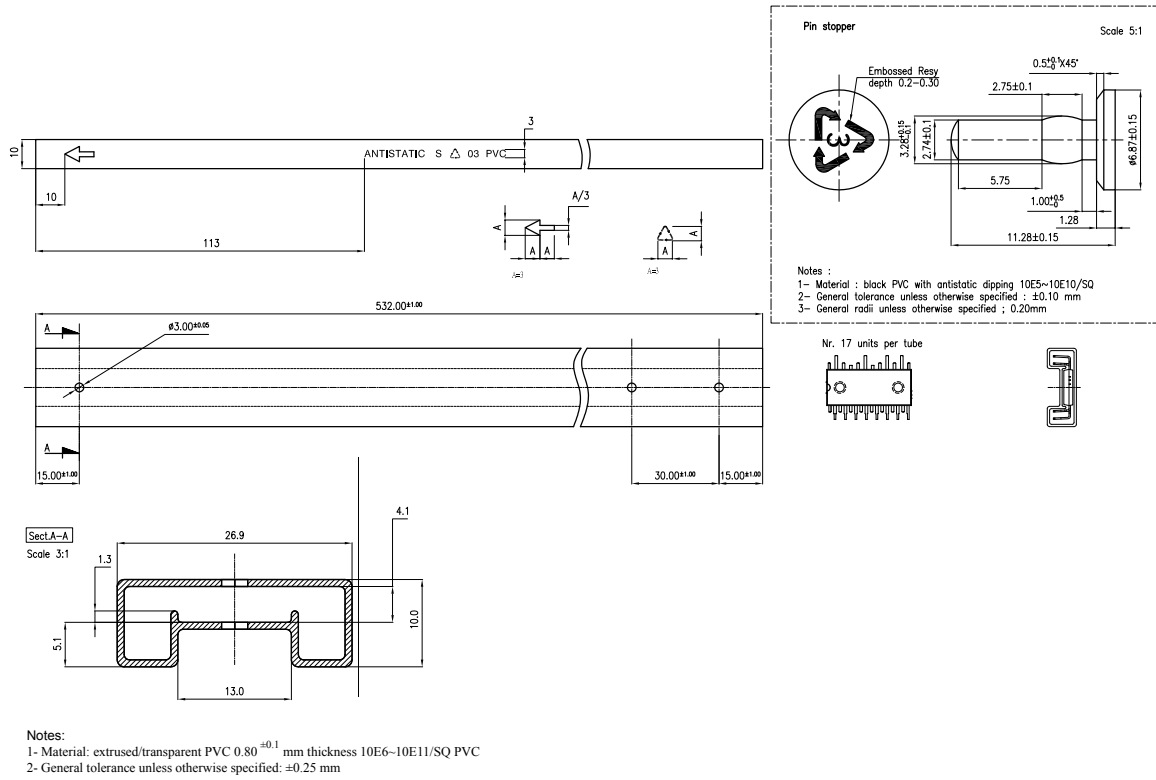
8278949_7

Table 12. NDIP-26L type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			4.40
A1	0.80	1.00	1.20
A2	3.00	3.10	3.20
A3	1.70	1.80	1.90
A4	5.70	5.90	6.10
b	0.53		0.72
b1	0.52	0.60	0.68
b2	0.83		1.02
b3	0.82	0.90	0.98
c	0.46		0.59
c1	0.45	0.50	0.55
D	29.05	29.15	29.25
D1	0.50	0.77	1.00
D2	0.35	0.53	0.70
D3			29.55
E	12.35	12.45	12.55
e	1.70	1.80	1.90
e1	2.40	2.50	2.60
eB1	16.10	16.40	16.70
eB2	21.18	21.48	21.78
L	1.24	1.39	1.54

5.2 NDIP-26L packing information

Figure 8. NDIP-26L tube (dimensions are in mm)



8313150_3

Table 13. Shipping details

Parameter	Value
Base quantity	17 pieces
Bulk quantity	476 pieces

Revision history

Table 14. Document revision history

Date	Revision	Changes
30-Sep-2014	1	Initial release.
13-Sep-2016	2	Updated <i>Section 5.1: "NDIP-26L type C package information"</i> and <i>Section 5.2: "NDIP-26L packing information"</i> Minor text changes
24-Aug-2022	3	Modified Applications on cover page Modified Table 5. Thermal data Minor text changes.

Contents

1	Internal schematic diagram and pin configuration	2
2	Electrical ratings	5
2.1	Absolute maximum ratings	5
2.2	Thermal data	5
3	Electrical characteristics	6
3.1	Inverter part	6
3.2	Control part	8
4	Application circuit example	10
4.1	Guidelines	11
5	Package information	12
5.1	NDIP-26L type C package information	12
5.2	NDIP-26L packing information	14
	Revision history	15

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved