TC4420/TC4429

6A High-Speed MOSFET Drivers

Features

- Latch-Up Protected: Will Withstand >1.5A Reverse Output Current
- Logic Input Will Withstand Negative Swing Up To 5V
- ESD Protected: 4 kV
- Matched Rise and Fall Times:
  - 25 ns (2500 pF load)
- High Peak Output Current: 6A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability: 10,000 pF
- Short Delay Time: 55 ns (typ.)
- CMOS/TTL Compatible Input
- Low Supply Current With Logic '1' Input:
  - 450 µA (typ.)
- Low Output Impedance: 2.5Ω
- Output Voltage Swing to Within 25 mV of Ground or V_{DD}
- Space-Saving 8-Pin SOIC and 8-Pin 6x5 DFN Packages

Applications

- Switch-Mode Power Supplies
- Motor Controls
- Pulse Transformer Driver
- Class D Switching Amplifiers

General Description

The TC4420/TC4429 are 6A (peak), single-output MOSFET drivers. The TC4429 is an inverting driver (pin-compatible with the TC429), while the TC4420 is a non-inverting driver. These drivers are fabricated in CMOS for lower power and more efficient operation versus bipolar drivers.
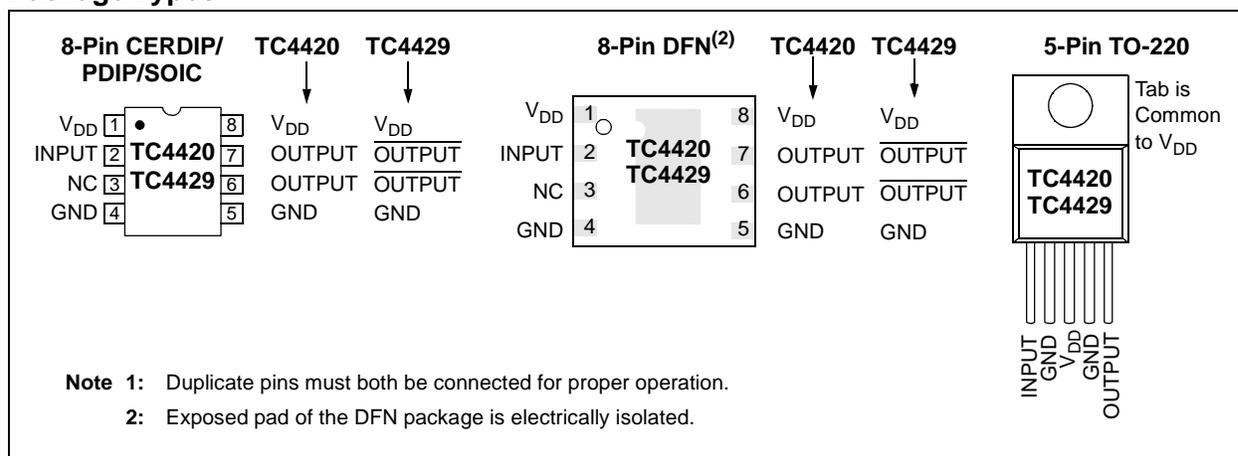
Both devices have TTL/CMOS compatible inputs that can be driven as high as V_{DD} + 0.3V or as low as –5V without upset or damage to the device. This eliminates the need for external level-shifting circuitry and its associated cost and size. The output swing is rail-to-rail, ensuring better drive voltage margin, especially during power-up/power-down sequencing. Propagational delay time is only 55 ns (typ.) and the output rise and fall times are only 25 ns (typ.) into 2500 pF across the usable power supply range.

Unlike other drivers, the TC4420/TC4429 are virtually latch-up proof. They replace three or more discrete components, saving PCB area, parts and improving overall system reliability.
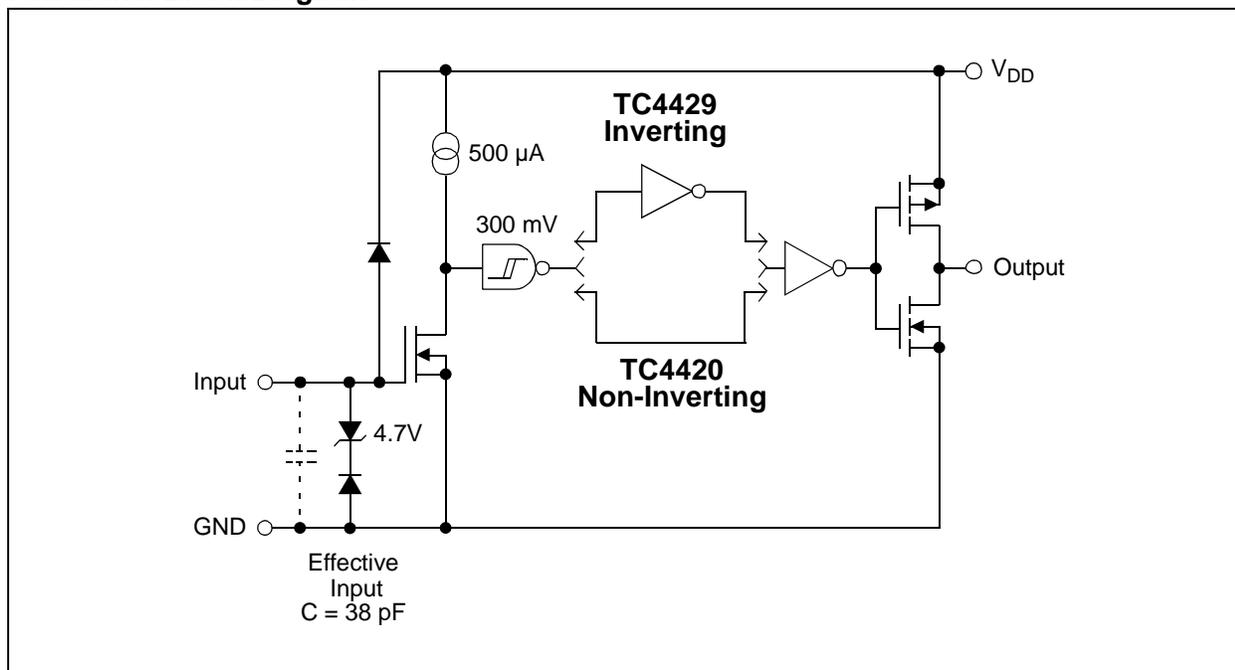
Package Types[1]

Note 1: Duplicate pins must both be connected for proper operation.

2: Exposed pad of the DFN package is electrically isolated.

TC4420/TC4429

Functional Block Diagram

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage ....+20V

Input Voltage .... – 5V to V_{DD} + 0.3V

Input Current ($V_{IN} > V_{DD}$)...................................50 mA

Power Dissipation ($T_A \leq 70°C$)
   5-Pin TO-220 .... 1.6W
   CERDIP... 800 mW
   DFN ....**Note 2**
   PDIP .... 730 mW
   SOIC.. 470 mW

Package Power Dissipation ($T_A \leq 25°C$)
   5-Pin TO-220 (With Heatsink) 12.5W

Thermal Impedances (To Case)
   5-Pin TO-220 $R_{\theta J-C}$ .... 10°C/W

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 4.5V $\leq V_{DD} \leq$ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	1.8	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	1.3	0.8	V	
Input Voltage Range	V_{IN}	–5	—	V_{DD}+0.3	V	
Input Current	I_{IN}	–10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	2.1	2.8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	1.5	2.5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	6.0	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	> 1.5	—	A	Duty cycle $\leq$ 2%, t $\leq$ 300 µsec
Switching Time (Note 1)						
Rise Time	t_R	—	25	35	ns	**Figure 4-1**, C_L = 2,500 pF
Fall Time	t_F	—	25	35	ns	**Figure 4-1**, C_L = 2,500 pF
Delay Time	t_{D1}	—	55	75	ns	**Figure 4-1**
Delay Time	t_{D2}	—	55	75	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	0.45	1.5	mA	V_{IN} = 3V
		—	55	150	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

2: Package power dissipation is dependent on the copper pad area on the PCB.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise noted, over operating temperature range with $4.5V \leq V_{DD} \leq 18V$.

| Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Voltage Range	V_{IN}	−5	—	V_{DD} + 0.3	V	
Input Current	I_{IN}	−10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC TEST
Low Output Voltage	V_{OL}	—	—	0.025	V	DC TEST
Output Resistance, High	R_{OH}	—	3	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	2.3	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	32	60	ns	**Figure 4-1**, C_L = 2,500 pF
Fall Time	t_F	—	34	60	ns	**Figure 4-1**, C_L = 2,500 pF
Delay Time	t_{D1}	—	50	100	ns	**Figure 4-1**
Delay Time	t_{D2}	—	65	100	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	—	0.45	3	mA	V_{IN} = 3V
		—	60	400	µA	V_{IN} = 0V
Operating Input Voltage	V_{DD}	4.5	—	18	V	

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with $4.5V \leq V_{DD} \leq 18V$.

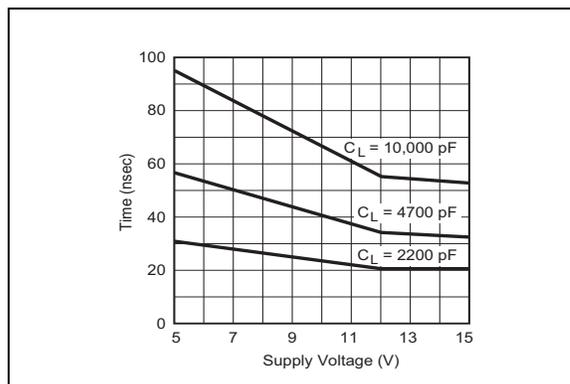| Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	°C	
Specified Temperature Range (I)	T_A	−25	—	+85	°C	
Specified Temperature Range (E)	T_A	−40	—	+85	°C	
Specified Temperature Range (V)	T_A	−40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	−65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 5L-TO-220	θ_{JA}	—	71	—	°C/W	
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	°C/W	
Thermal Resistance, 8L-6x5 DFN	θ_{JA}	—	33.2	—	°C/W	Typical four-layer board with vias to ground plane.
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.
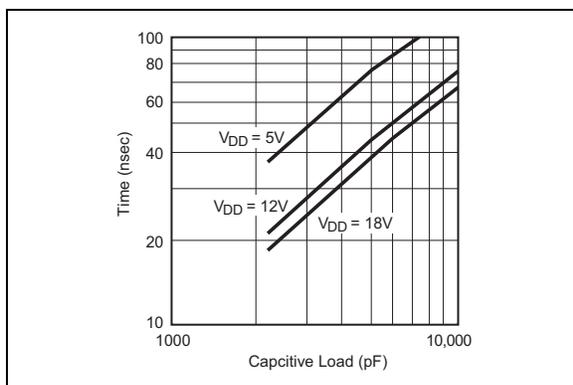
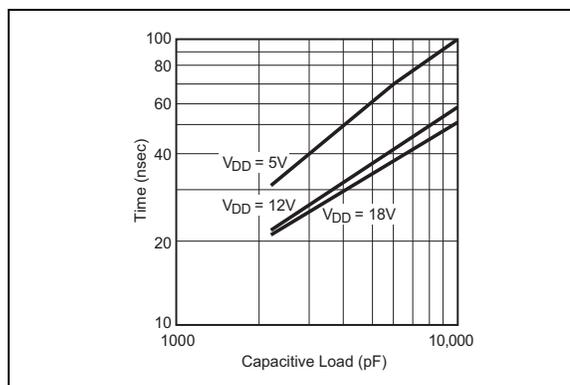**Note:** Unless otherwise indicated, T_A = +25°C with 4.5V $\leq V_{DD} \leq$ 18V.
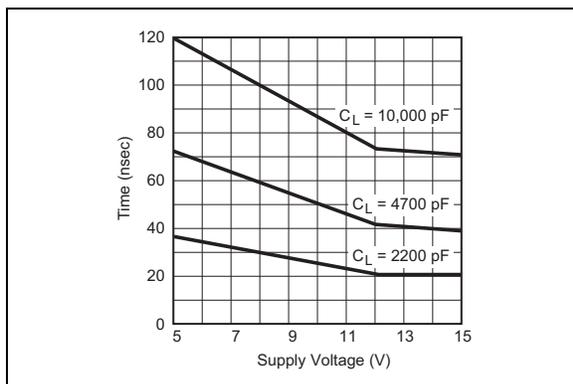
FIGURE 2-1: Rise Time vs. Supply Voltage.

FIGURE 2-2: Rise Time vs. Capacitive Load.
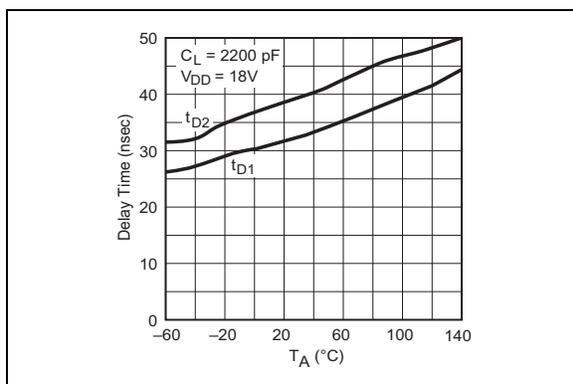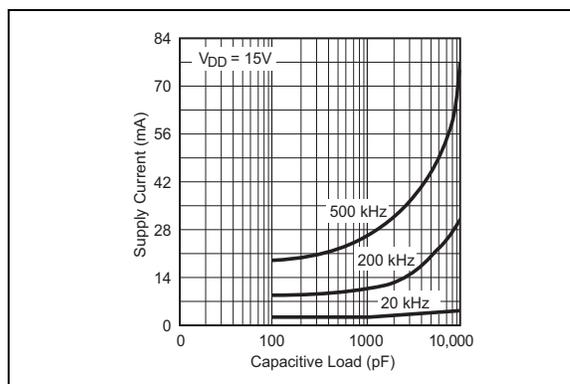
FIGURE 2-3: Propagation Delay Time vs. Temperature.

FIGURE 2-4: Fall Time vs. Supply Voltage.

FIGURE 2-5: Fall Time vs. Capacitive Load.
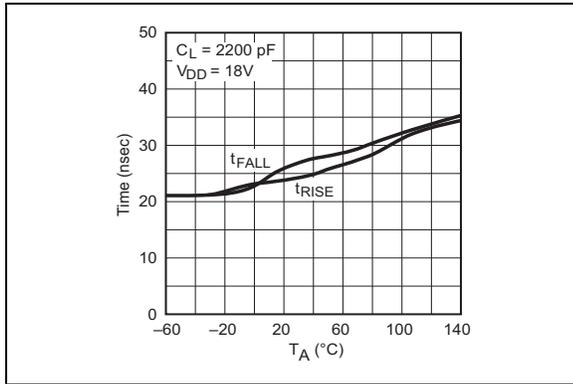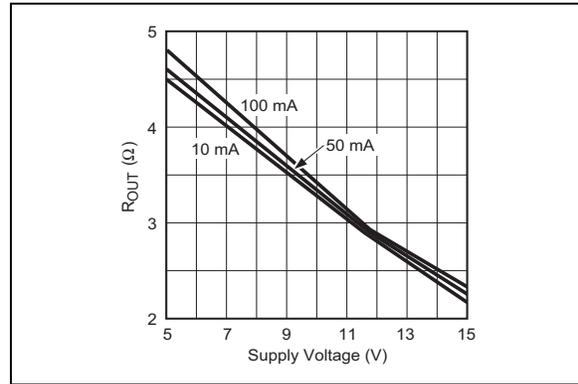
FIGURE 2-6: Supply Current vs. Capacitive Load.

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FIGURE 2-7: *Rise and Fall Times vs. Temperature.*

FIGURE 2-8: *Propagation Delay Time vs. Supply Voltage.*

FIGURE 2-9: *Supply Current vs. Frequency.*

FIGURE 2-10: *High-State Output Resistance vs Supply Voltage.*

FIGURE 2-11: *Effect of Input Amplitude on Propagation Delay.*
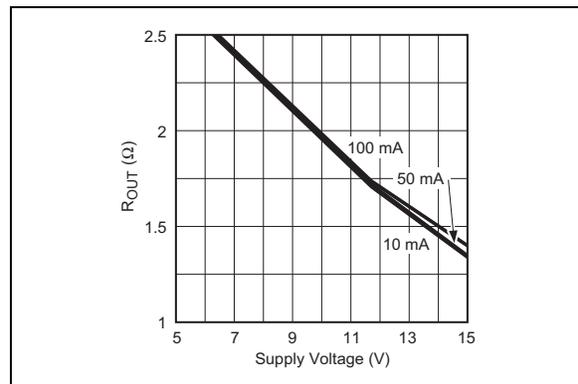
FIGURE 2-12: *Low-State Output Resistance vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25°C with 4.5V $\leq V_{DD} \leq$ 18V.

The values on this graph represent the loss seen by the driver during one complete cycle. For a single transition, divide the value by 2.
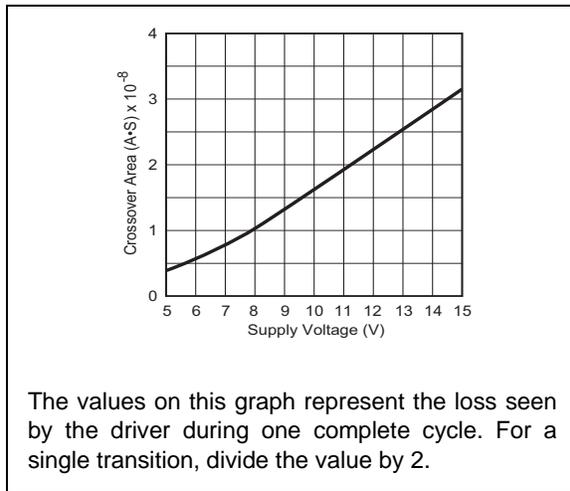
FIGURE 2-13: *Crossover Energy.*

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3.0   PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1:   PIN FUNCTION TABLE

Pin No. 8-Pin CERDIP/ PDIP/SOIC	Pin No. 8-Pin DFN	Pin No. 5-Pin TO-220	Symbol	Description
1	1	—	V_{DD}	Supply input, 4.5V to 18V
2	2	1	INPUT	Control input, TTL/CMOS compatible input
3	3	—	NC	No Connection
4	4	2	GND	Ground
5	5	4	GND	Ground
6	6	5	OUTPUT	CMOS push-pull output
7	7	—	OUTPUT	CMOS push-pull output
8	8	3	V_{DD}	Supply input, 4.5V to 18V
—	PAD	—	NC	Exposed Metal Pad
—	—	TAB	V_{DD}	Metal Tab is at the V_{DD} Potential

3.1   Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pins. The V_{DD} input should be bypassed to ground with a local ceramic capacitor. The value of the capacitor should be chosen based on the capacitive load that is being driven. A minimum value of 1.0 μF is suggested.

3.2   Control Input

The MOSFET driver input is a high-impedance, TTL/CMOS compatible input. The input circuitry of the TC4420/TC4429 MOSFET driver also has a "speed-up" capacitor. This helps to decrease the propagation delay times of the driver. Because of this, input signals with slow rising or falling edges should not be used, as this can result in double-pulsing of the MOSFET driver output.

3.3   CMOS Push-Pull Output

The MOSFET driver output is a low-impedance, CMOS, push-pull style output capable of driving a capacitive load with 6.0A peak currents. The MOSFET driver output is capable of withstanding 1.5A peak reverse currents of either polarity.

3.4   Ground

The ground pins are the return path for the bias current and the high peak currents that discharge the load capacitor. The ground pins should be tied into a ground plane or have very short traces to the bias supply source return.

3.5   Exposed Metal Pad

The exposed metal pad of the 6x5 DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board (PCB) to aid in heat removal from the package.

4.0   APPLICATIONS INFORMATION
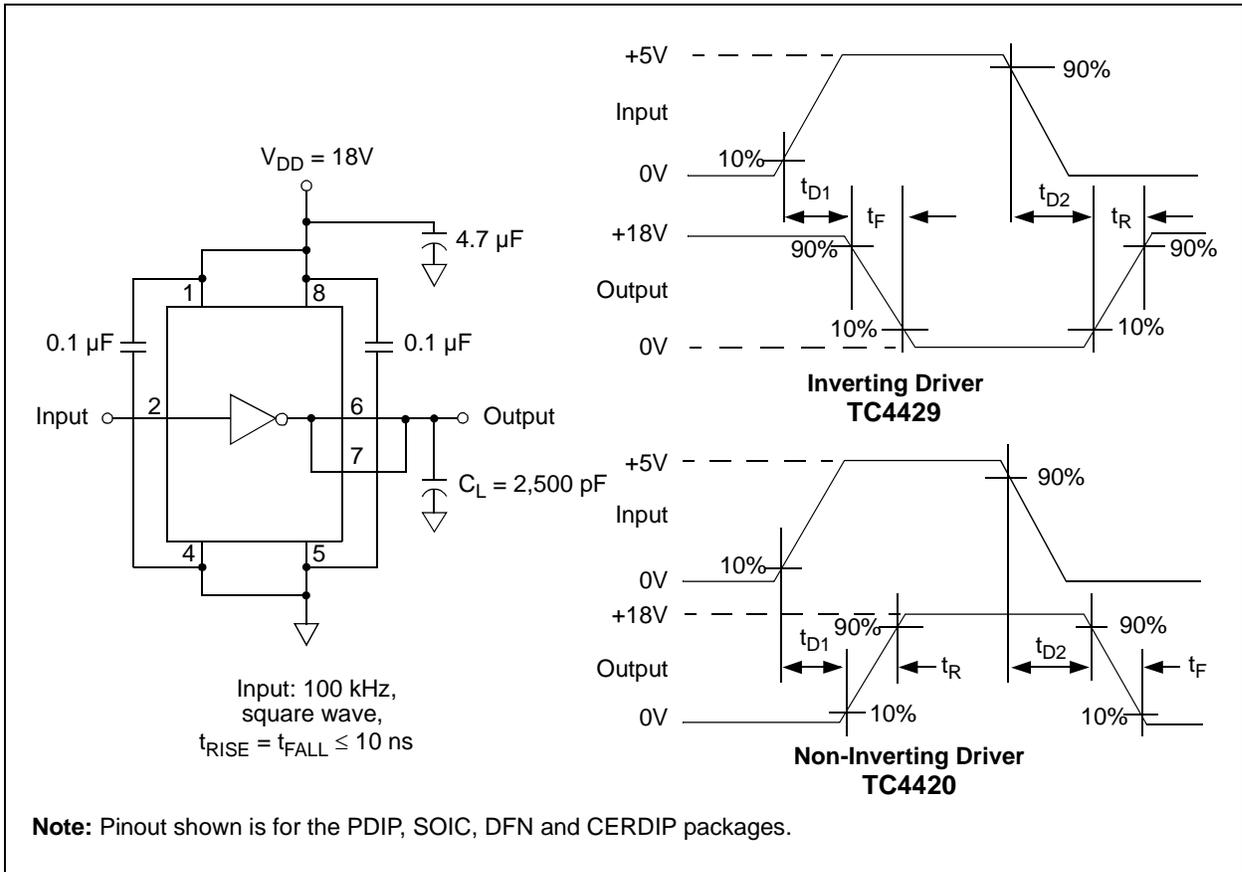
FIGURE 4-1:   *Switching Time Test Circuits.*

TC4420/TC4429

5.0   PACKAGING INFORMATION

5.1   Package Marking Information

5-Lead TO-220

Example:

```
XXXXXXXX
XXXXXXXX
 YYWWNNN
```

```
TC4420CAT
0419256
```

8-Lead CERDIP (300 mil)

Example:

```
XXXXXXXX
XXXXXNNN
     YYWW
```

```
TC4420
MJA256
   0419
```

8-Lead DFN

Example:

```
XXXXXXX
XXXXXXX
XXYYWW
  NNN
```
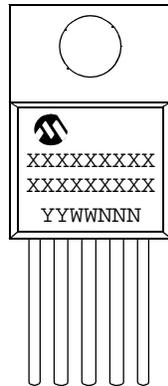
```
TC4420
 EMF
 0419
  256
```
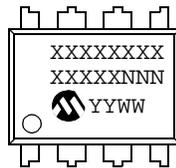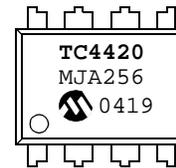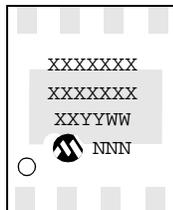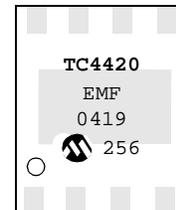
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

8-Lead PDIP (300 mil)

```
XXXXXXXX
XXXXXNNN
  YYWW
```

Example:

```
TC4420
CPA256
  0419
```

8-Lead SOIC (150 mil)

```
XXXXXXXX
XXXXXYYWW
  NNN
```

Example:

```
TC4420
EOA0419
  256
```
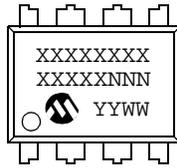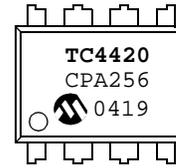
TC4420/TC4429

5-Lead Plastic Transistor Outline (AT) (TO-220)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

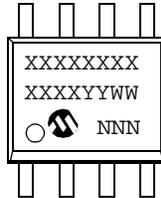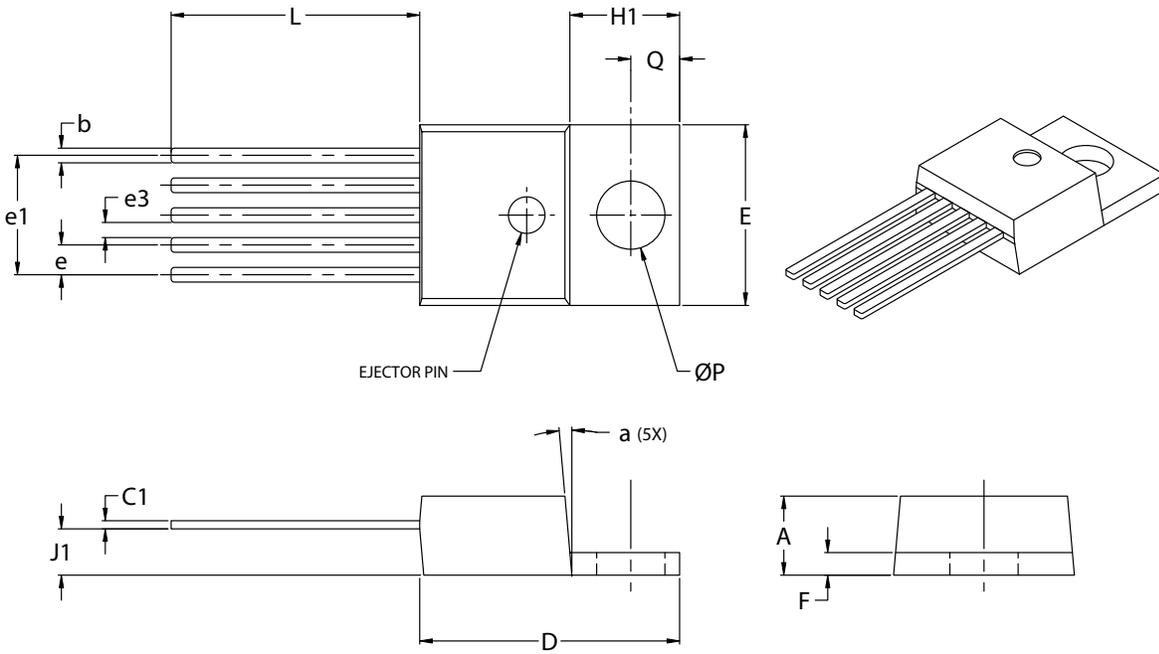|	Units	INCHES*		MILLIMETERS	
Dimension Limits		MIN	MAX	MIN	MAX
Lead Pitch	e	.060	.072	1.52	1.83
Overall Lead Centers	e1	.263	.273	6.68	6.93
Space Between Leads	e3	.030	.040	0.76	1.02
Overall Height	A	.160	.190	4.06	4.83
Overall Width	E	.385	.415	9.78	10.54
Overall Length	D	.560	.590	14.22	14.99
Flag Length	H1	.234	.258	5.94	6.55
Flag Thickness	F	.045	.055	1.14	1.40
Through Hole Center	Q	.103	.113	2.62	2.87
Through Hole Diameter	P	.146	.156	3.71	3.96
Lead Length	L	.540	.560	13.72	14.22
Base to Bottom of Lead	J1	.090	.115	2.29	2.92
Lead Thickness	C1	.014	.022	0.36	0.56
Lead Width	b	.025	.040	0.64	1.02
Mold Draft Angle	a	3°	7°	3°	7°

*Controlling Parameter

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC equivalent: TO-220

Drawing No. C04-036

8-Lead Ceramic Dual In-line – 300 mil (JA) (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
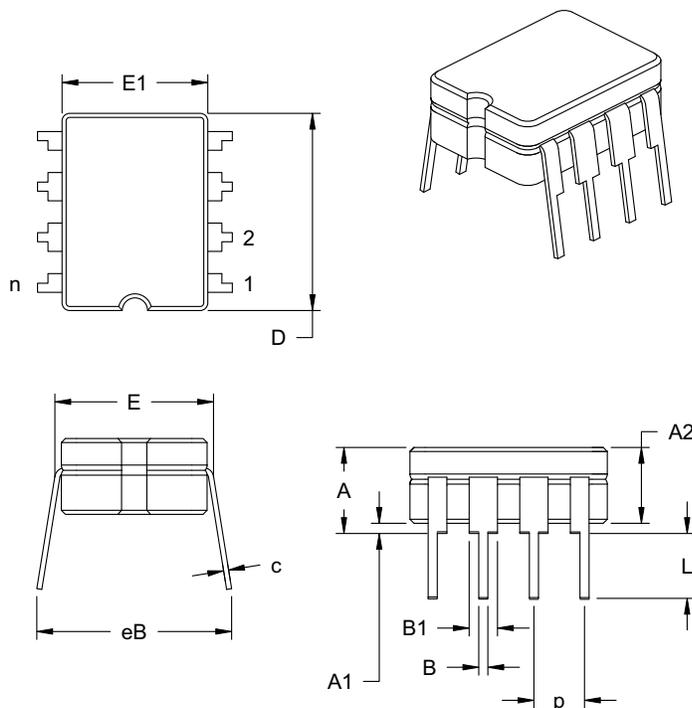
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

TC4420/TC4429

8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

BOTTOM VIEW
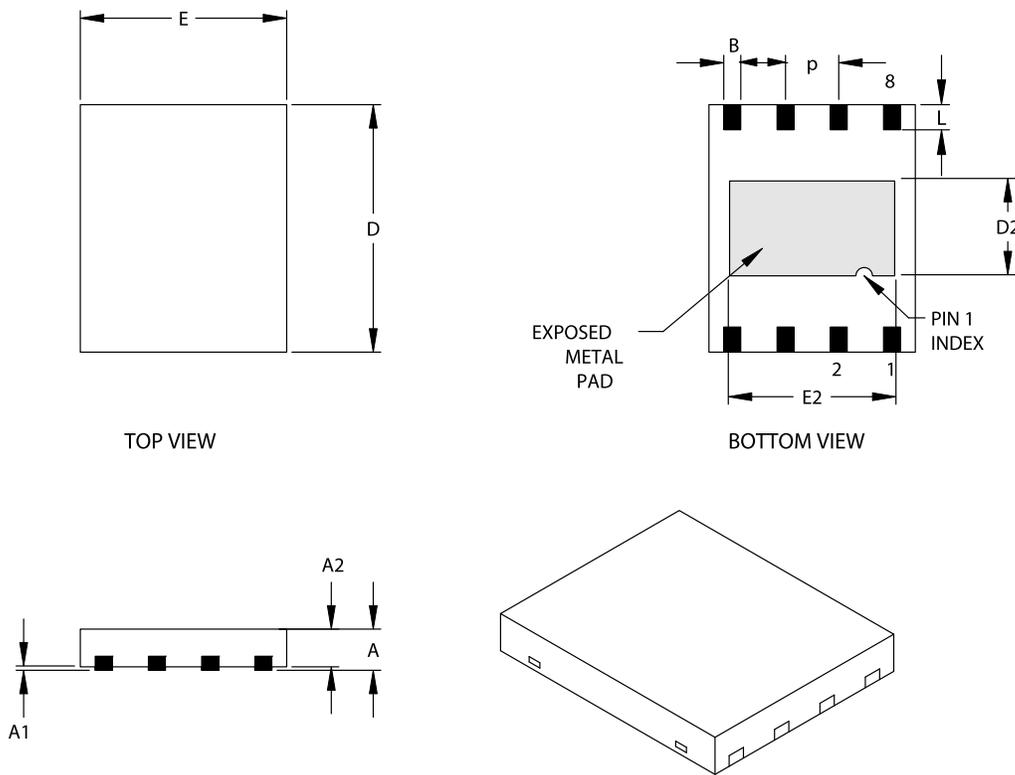
	Units	INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050 BSC			1.27 BSC	
Overall Height	A	.033	.035	.037	0.85	0.90	0.95
Package Thickness	A2	.031	.035	.037	0.80	0.89	0.95
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.007	.008	.009	0.17	0.20	0.23
Overall Length	E	.195	.197	.199	4.95	5.00	5.05
Exposed Pad Length	E2	.152	.157	.163	3.85	4.00	4.15
Overall Width	D	.234	.236	.238	5.95	6.00	6.05
Exposed Pad Width	D2	.089	.091	.093	2.25	2.30	2.35
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.024		.026	0.60		0.65

Notes:

JEDEC equivalent: MO-220

Drawing No. C04-122

Revised 11/3/03

8-Lead Plastic Dual In-line (PA) – 300 mil (PDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

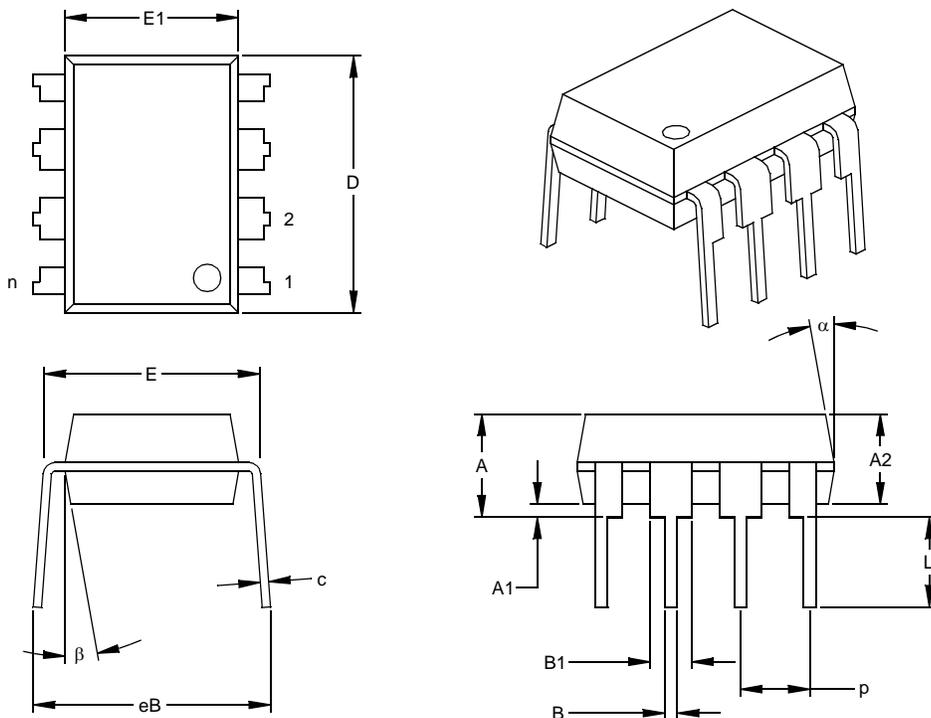|	Units		INCHES*			MILLIMETERS	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

TC4420/TC4429

8-Lead Plastic Small Outline (OA) – Narrow, 150 mil (SOIC)

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

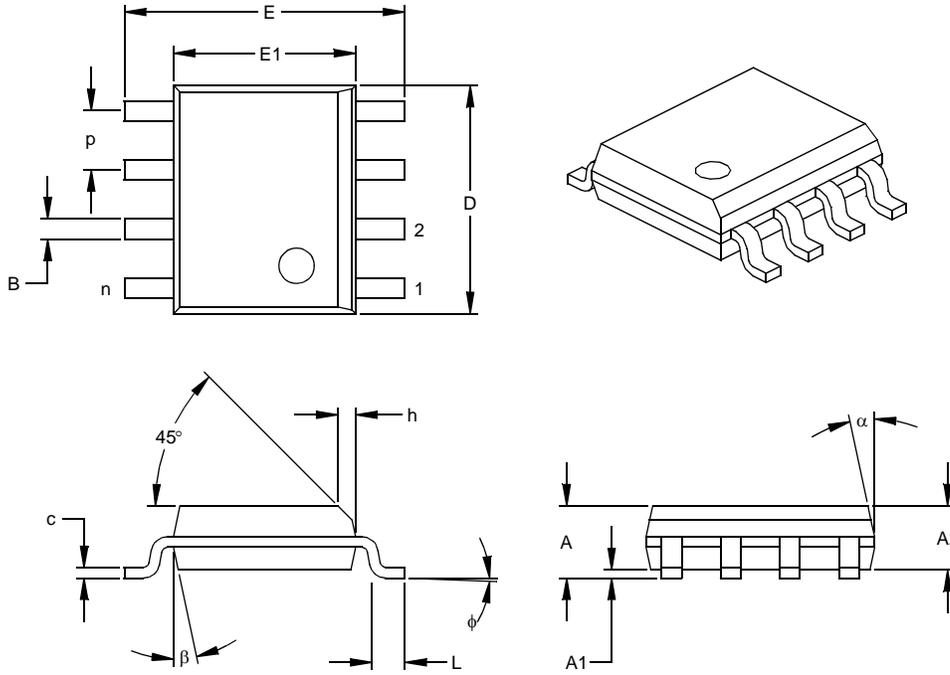|	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

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6.0   REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX	X
Device	**Temperature Range**	**Package**	**Tape and Reel**	**PB Free**

Device:
TC4420:   6A High-Speed MOSFET Driver, Non-Inverting
TC4429:   6A High-Speed MOSFET Driver, Inverting

Temperature Range:
C   =   0°C to +70°C (PDIP, SOIC, and TO-220 Only)
I   =   -25°C to +85°C (CERDIP Only)
E   =   -40°C to +85°C
V   =   -40°C to +125°C

Package:
AT   = TO-220, 5-lead (C-Temp Only)
JA   = Ceramic Dual In-line (300 mil Body), 8-lead (I-Temp Only)
MF   = Dual, Flat, No-Lead (6X5 mm Body), 8-lead
MF713 = Dual, Flat, No-Lead (6X5 mm Body), 8-lead (Tape and Reel)
PA   = Plastic DIP (300 mil Body), 8-lead
OA   = Plastic SOIC, (150 mil Body), 8-lead
OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel)

PB Free
G   = Lead-Free device*
    = Blank

* Available on selected packages. Contact your local sales representative for availability

Examples:

a)   TC4420CAT: 6A High-Speed MOSFET Driver, Non-inverting, TO-220 package, 0°C to +70°C.

b)   TC4420EOA: 6A High-Speed MOSFET Driver, Non-inverting, SOIC package, -40°C to +85°C.

c)   TC4420VMF: 6A High-Speed MOSFET Driver, Non-inverting, DFN package, -40°C to +125°C.

a)   TC4429CAT: 6A High-Speed MOSFET Driver, Inverting, TO-220 package, 0°C to +70°C

b)   TC4429EPA: 6A High-Speed MOSFET Driver, Inverting, PDIP package, -40°C to +85°C

c)   TC4429VMF: 6A High-Speed MOSFET Driver, Inverting, DFN package, -40°C to +125°C

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1.   Your local Microchip sales office
2.   The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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