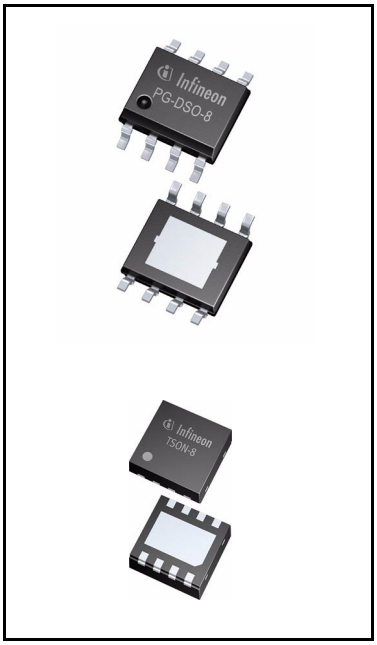
TLE7258

LIN transceiver

AEC Qualified

RoHS



Features

- Single-wire LIN transceiver for transmission rates up to 20 kbps
- Compliant to ISO 17987-4, LIN specification 2.2A and SAE J2602
- Very low current consumption in sleep mode with wake-up capability
- Very low leakage current on the BUS pin
- Digital I/O levels compatible with 3.3 V and 5 V microcontrollers
- TxD protected with dominant time-out function and state check after mode change to normal operation mode
- BUS short to VBAT protection and BUS short to GND handling
- Over temperature protection and supply undervoltage detection
- Very high ESD robustness, ± 10 kV according to IEC61000-4-2
- Optimized for high electromagnetic compatibility (EMC); Very low emission and high immunity to interference
- Available in standard PG-DSO-8 and leadless PG-TSON-8 packages
- PG-TSON-8 package supports automated optical inspection (AOI)
- Green Product (RoHS compliant)

Potential applications

- LIN slave satellite modules
- Rain and light sensors
- Window lifters
- Parking aid systems

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE7258 is a transceiver for the local interconnect network (LIN) with integrated wake-up and protection features. It is designed for in-vehicle networks using data transmission rates up to 20 kbps. The TLE7258 operate as a bus driver between the protocol controller and the physical bus of the LIN network. Compliant to all LIN standards and with a wide operational supply range the TLE7258 can be used in all automotive applications.

The usage of different operation modes and the INH output allows the TLE7258 to control external components like e.g. voltage regulators. In sleep mode the TLE7258 draws typically less than 10 µA of quiescent current while still being able to wake-up when detecting LIN bus traffic. The very low leakage current on the BUS pin makes the TLE7258 especially suitable for partially supplied networks.

Based on the Infineon BiCMOS technology the TLE7258 provides excellent ESD robustness together with a very high electromagnetic compatibility (EMC). The TLE7258 reaches a very low level of electromagnetic emission (EME) within a broad frequency range and independent from the battery voltage. The TLE7258 is AEC qualified and tailored to withstand the harsh conditions of the automotive environment.

Type	Package	Marking
TLE7258SJ	PG-DSO-8	7258
TLE7258LE	PG-TSON-8	7258

Table of Contents

1 Block diagram . . . 4

2 Pin configuration . . . 5
2.1 Pin assignment . . . 5
2.2 Pin definitions and functions . . . 5

3 Functional description . . . 6
3.1 Operating modes . . . 7
3.2 Normal operation mode . . . 8
3.3 Standby mode . . . 9
3.4 Sleep mode . . . 11
3.5 Bus wake-up event . . . 12
3.6 Mode transition via EN input . . . 13
3.7 Overtemperature protection . . . 14
3.8 Undervoltage detection . . . 15
3.9 TxD time-out . . . 16
3.10 3.3 V and 5 V logic capability . . . 16
3.11 Short circuit . . . 16

4 General product characteristics . . . 17
4.1 Absolute maximum ratings . . . 17
4.2 Functional range . . . 18
4.3 Thermal characteristics . . . 18

5 Electrical characteristics . . . 19
5.1 Functional device characteristics . . . 19
5.2 Diagrams . . . 23

6 Application information . . . 24
6.1 Application example . . . 24
6.2 ESD Susceptibility according to IEC61000-4-2 . . . 25
6.3 Transient robustness according to ISO 7637-2 . . . 25
6.4 LIN Physical layer compatibility . . . 25
6.5 TxD Fail-safe input . . . 25
6.6 RxD Pull-up resistor . . . 26
6.7 Compatibility with other Infineon LIN transceivers . . . 27

7 Package outlines . . . 29

8 Revision history . . . 30

1 Block diagram

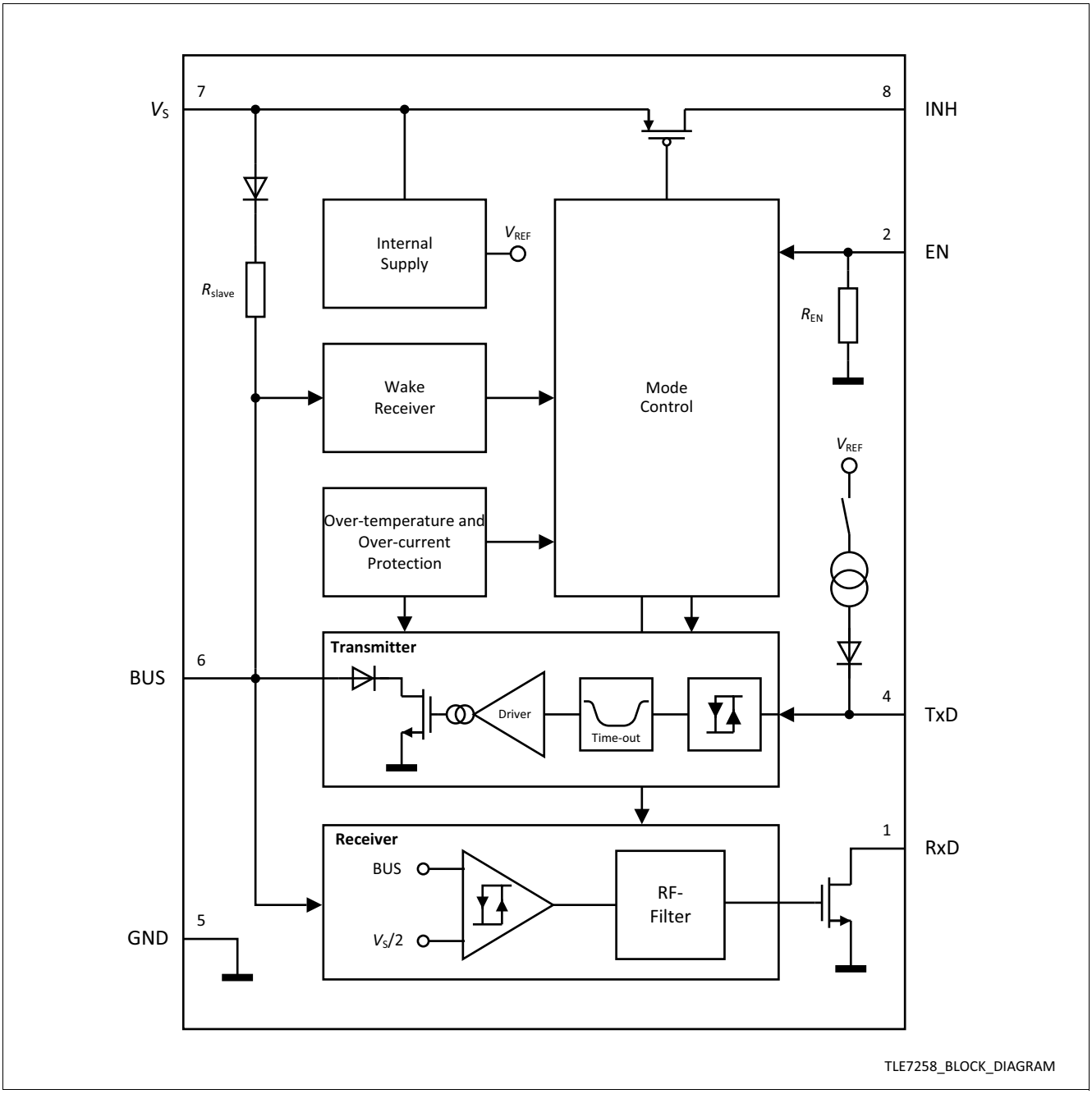


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

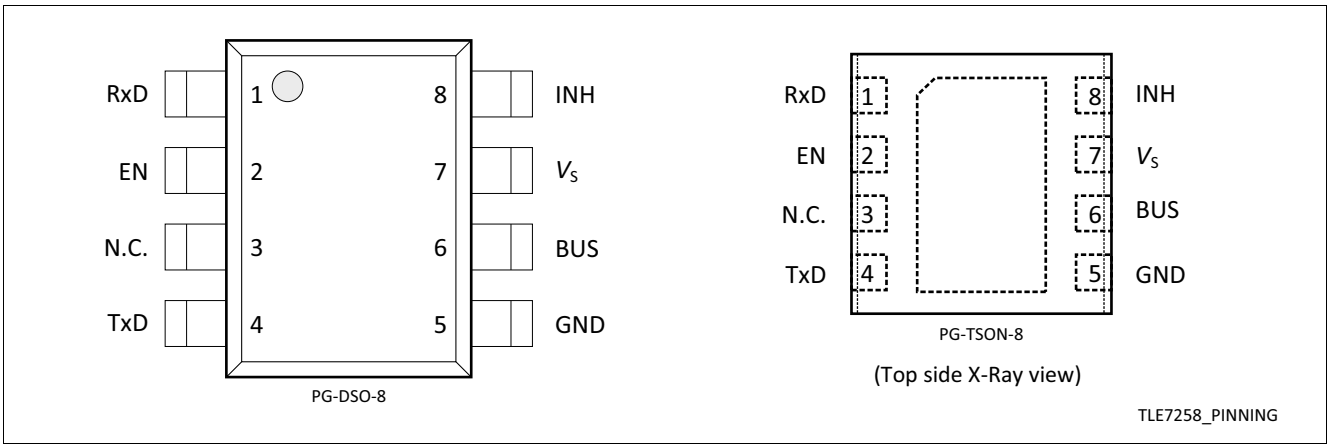


Figure 2 Pin configuration

2.2 Pin definitions and functions

Pin	Symbol	Function
1	RxD	**Receive data output;** External pull-up necessary Monitors the LIN bus signal in normal operation mode Indicates a wake-up event in standby mode
2	EN	**Enable input;** Integrated pull-down resistor Logical “high” to select normal operation mode
3	N.C.	**Not connected**
4	TxD	**Transmit data input;** Integrated pull-up current source Logical “low” to drive a “dominant” signal on the LIN bus
5	GND	**Ground**
6	BUS	**Bus input / output;** Integrated LIN slave termination
7	V_s	**Battery supply input;** 100 nF decoupling capacitor required
8	INH	**Inhibit output;** Battery supply related output Active in normal operation mode and standby mode
PAD[1)]	–	Connect to PCB heat sink area. Do not connect to other voltage potential than GND

1) Only for PG-TSON-8 package version (TLE7258LE)

3 Functional description

The LIN interface is a single wire, bi-directional bus, used for in-vehicle networks. The TLE7258 LIN transceiver is the interface between the microcontroller and the physical LIN Bus (see **Figure 16**). Data from the microcontroller is driven to the LIN bus via the TxD input of the TLE7258. The transmit data stream on the TxD input is converted to a LIN bus signal with optimized slew rates in order to minimize the electromagnetic emission level of the LIN network. The RxD output reads back the information from the LIN bus to the microcontroller. The receiver has an integrated filter network to suppress noise from the LIN bus and to increase the electromagnetic immunity level of the transceiver.

The LIN specification defines two valid bus states (see **Figure 3**):

- "Dominant" state with the LIN bus voltage level near GND.
- "Recessive" state with the LIN bus voltage pulled up to the supply voltage V_S through the bus termination.

By setting the TxD input of the TLE7258 to a logical "low" signal, the transceiver generates a "dominant" level on the BUS interface pin. The receiver reads back the signal on the LIN bus and indicates the "dominant" LIN bus signal with a logical "low" level on the RxD output to the microcontroller. By setting the TxD input to logical "high", the transceiver sets the LIN interface pin to the "recessive" level. At the same time the "recessive" level on the LIN bus is indicated by a logical "high" level on the RxD output.

Every LIN network consists of a master node and one or more slave nodes. To configure the TLE7258 for master node applications, a termination resistor of 1 kΩ and a diode must be connected between the LIN bus and the power supply V_S (see **Figure 16**).

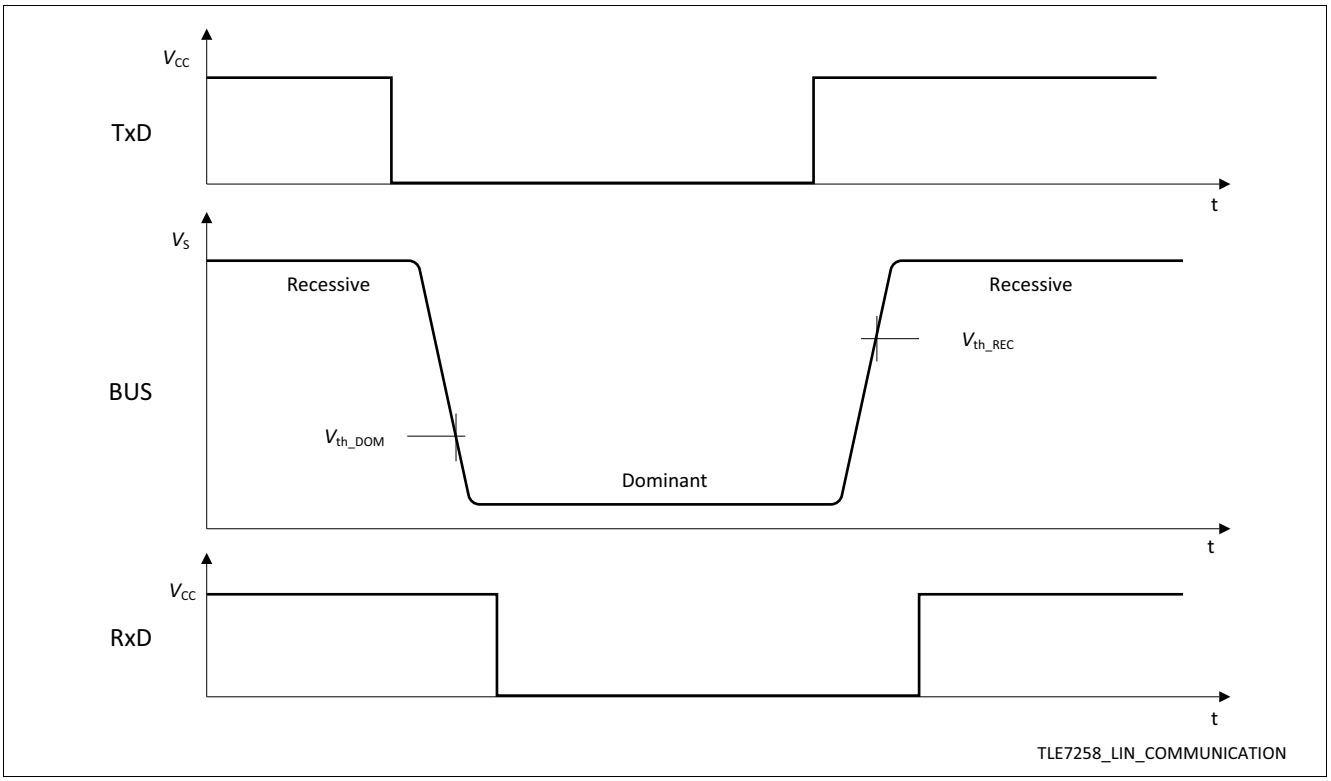


Figure 3 LIN bus signals

3.1 Operating modes

The TLE7258 has 3 major operation modes (see **Figure 4**):

- Normal operation mode
- Standby mode
- Sleep mode

Table 1 Operating modes

Mode	EN	INH	TxD	RxD	LIN Bus termination	Comments
Sleep	Low	Floating	Disabled[1)]	High[2)]	30 kΩ (typical)	No wake-up request detected
Standby	Low	High	High[3)]	Low High[2)]	30 kΩ (typical)	RxD “low” after a bus wake-up RxD “high“ after Power-up
Normal operation	High	High	Low High	Low High	30 kΩ (typical)	RxD reflects the signal on the bus TxD driven by the microcontroller

1) The TxD input is disabled in sleep mode and the internal pull-up current source is switched off (see **Figure 1**).
2) A pull-up resistor to the external microcontroller supply is required.
3) In case the TxD input is open the state is internally set to logical “high” through the internal pull-up current source.

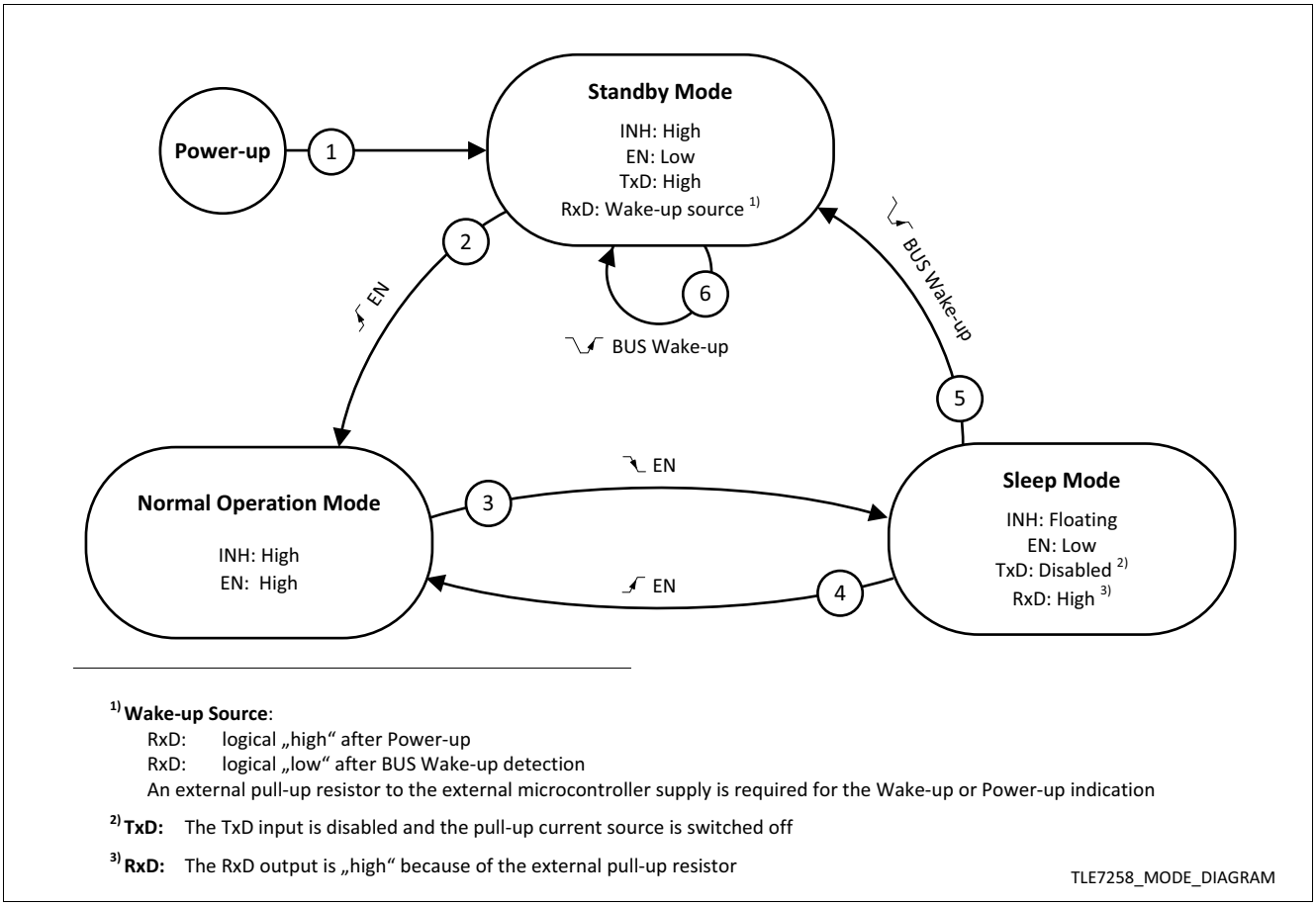


Figure 4 Operation mode state diagram

Table 2 Operation mode transitions

Number	Reason for transition	Comment
1	Power-on detection	The VS supply voltage rise above the VS,UV,PON power-on reset level
2	Mode change with EN input	Triggered by logical “high” level
3	Mode change with EN input	Triggered by logical “low” level
4	Mode change with EN input	Triggered by logical “high” level
5	Bus wake-up detection	RxD set “low” for signalling the bus wake-up event to the microcontroller
6	Bus wake-up detection	RxD set “low” for signalling the bus wake-up event to the microcontroller

3.2 Normal operation mode

While operating in normal operation mode the LIN bus receiver and transmitter are active and support data transmission rates up to 20 kbps. Data from the microcontroller is transmitted to the LIN bus via the TxD input. Simultaneously the receiver detects the data stream on the LIN bus and forwards it to the RxD output.

Normal operation mode can be entered from either sleep mode (see **Figure 9**) or from standby mode (see **Figure 5**), by setting the EN input to logical “high”. From normal operation mode the TLE7258 can only enter sleep mode, it is not possible to enter standby mode directly (see **Figure 4**).

The transition time for mode change to normal operation mode t_{MODE} specifies the delay between the threshold, where the EN pin detects a “high” input signal, and the actual mode change of TLE7258 to normal operation mode.

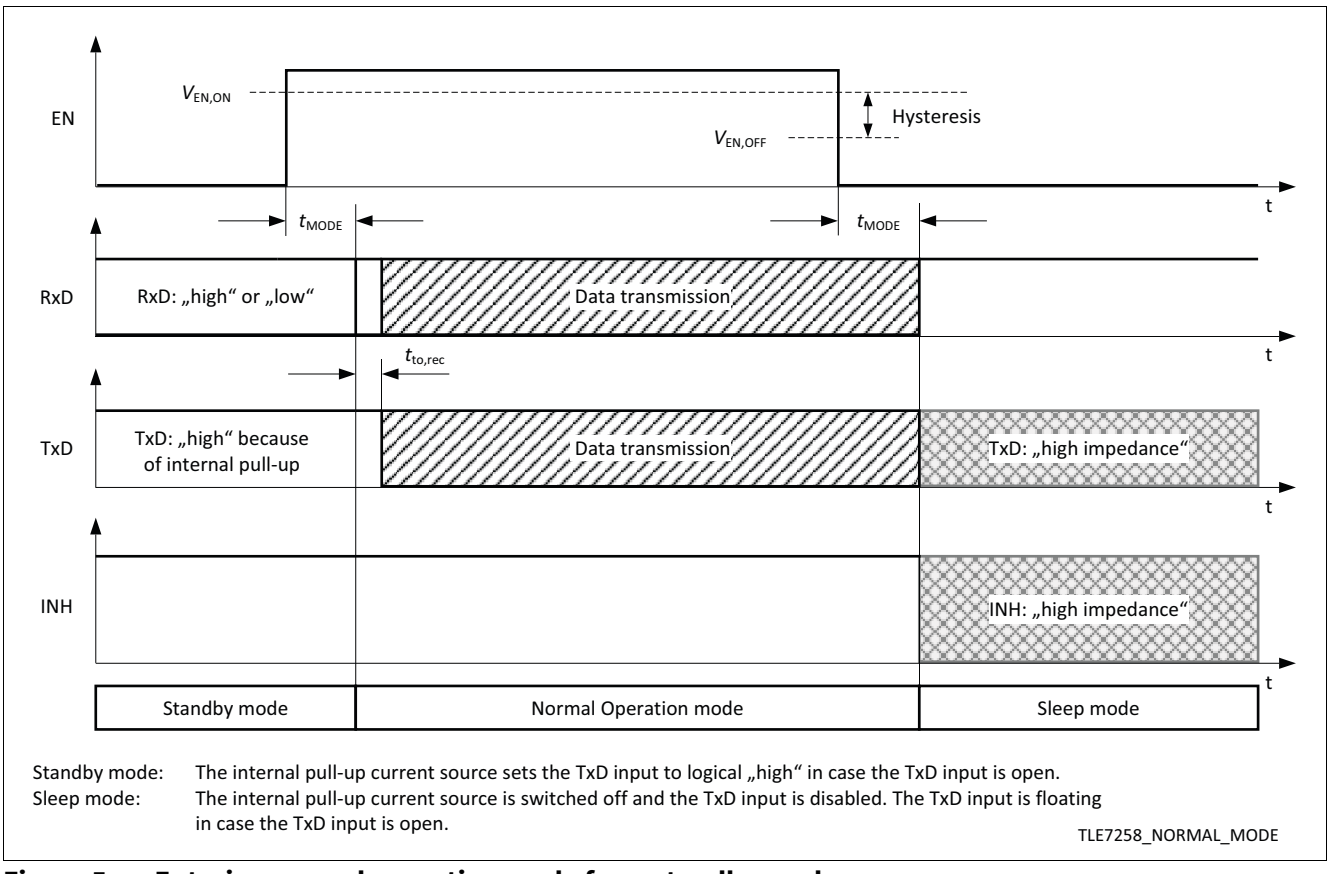


Figure 5 Entering normal operation mode from standby mode

While the TLE7258 is in normal operation mode the following functions are available:

- The transmitter is turned on; data on the TxD input are driven on the LIN bus.
- The receiver is turned on; data on the LIN bus are monitored and signaled on the RxD output.
- The BUS pin is terminated to V_S via the internal termination resistor R_{BUS} (see **Figure 1**).
- The TxD input is pulled up via a current source to the internal power supply of the TLE7258.
- The INH output is switched on.
- The bus wake-up comparator is turned off.
- The two-level undervoltage detection is active. In case V_S drops below the undervoltage detection level the TLE7258 blocks the transmitter and receiver. In case V_S drops below the power-on reset level $V_{S,UV,PON}$ the TLE7258 changes the operation mode to standby mode after recovery (see **"Undervoltage detection" on Page 15**).
- The EN input is active. A "low" signal on the EN input triggers a transition to Sleep.

After a mode change to normal operation the TLE7258 requires a logical "high" signal for the time $t_{to,rec}$ on the TxD input before releasing the data communication (see **Figure 5**). The transmitter remains deactivated as long as the signal on the TxD input remains logical "low", preventing possible bus communication disturbance.

3.3 Standby mode

The standby mode is entered automatically after:

- A power-up event on the supply V_S.
- A bus wake-up event.
- A power-on reset caused by the supply V_S.

In standby mode no communication to the LIN bus is possible. The transmitter and the receiver are disabled.

While the TLE7258 is in standby mode the following functions are available:

- The transmitter is turned off, the TxD input is inactive and the bus output is permanent "recessive".
- The receiver is turned off.
- The RxD output indicates either a wake-up event or a power-up event (see **Figure 4** and **Table 1**).
- The BUS pin is terminated to V_S via the internal termination resistor R_{BUS} (see **Figure 1**).
- The TxD input is pulled up with a current source to the internal power supply of the TLE7258.
- The INH output is switched on.
- The bus wake-up comparator is active and indicates wake-up events on the RxD pin.
- In standby mode only the power-on reset level of the undervoltage detection is active (see **"Undervoltage detection" on Page 15**).
- The EN input is active. A "high" signal on the EN input triggers a transition to normal operation mode (see **Figure 5**).

After a power-up event the TLE7258 enters standby mode by default. The EN pin has an internal pull-down resistor and the TLE7258 remains in standby until the external microcontroller applies a logical "high" signal at the EN input (see **Figure 6**).

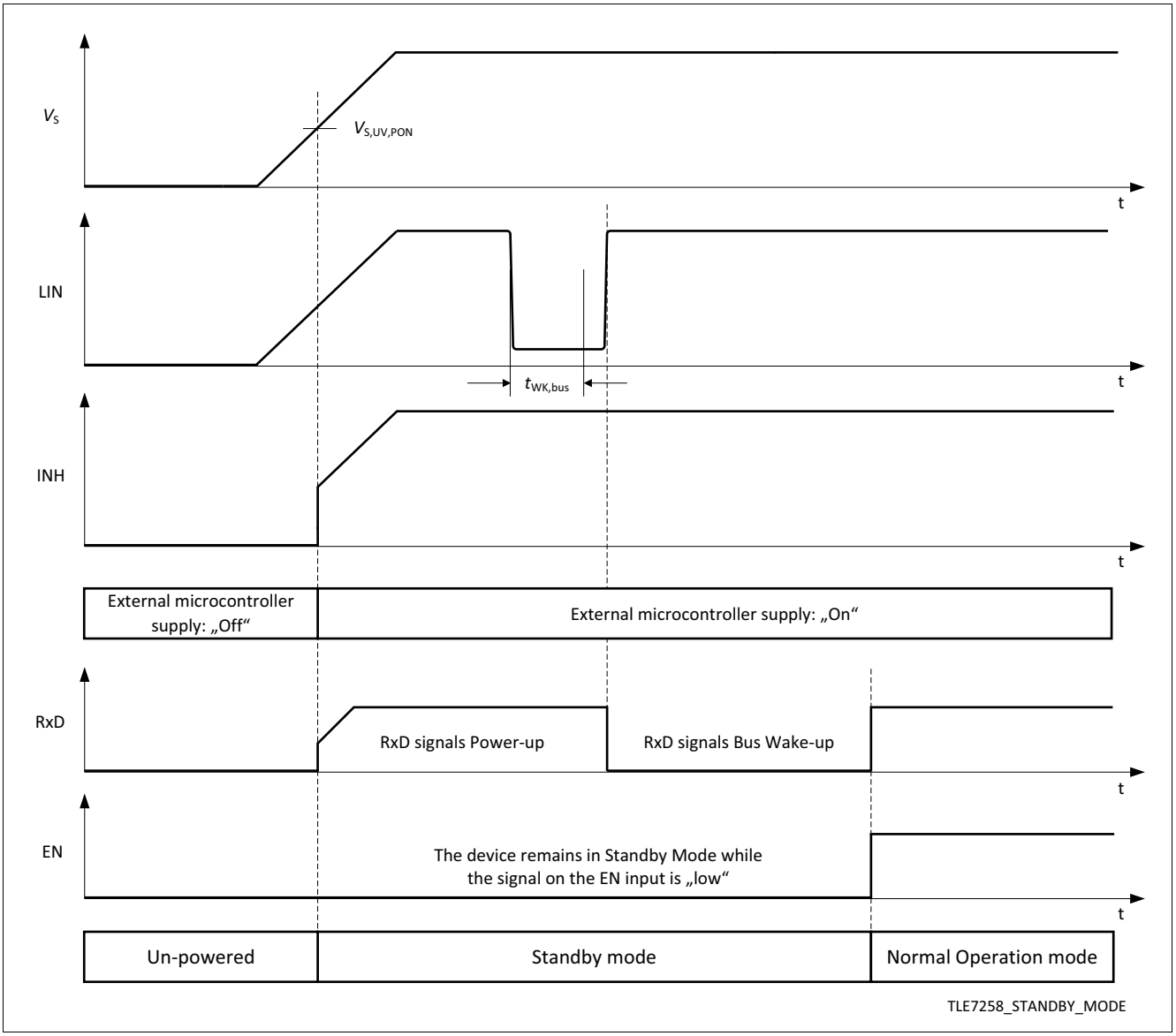


Figure 6 Entering standby mode after power-up

3.4 Sleep mode

Sleep mode is a low power mode with quiescent current consumption reduced to a minimum while the device is still able to wake-up by a message on the LIN bus.

To switch the TLE7258 from normal operation mode to sleep mode, the EN input has to be set to “low”. Conversely a logical “high” signal on the EN input sets the device directly back to normal operation mode (see **Figure 4**). The TLE7258 can only enter sleep mode from normal operation mode.

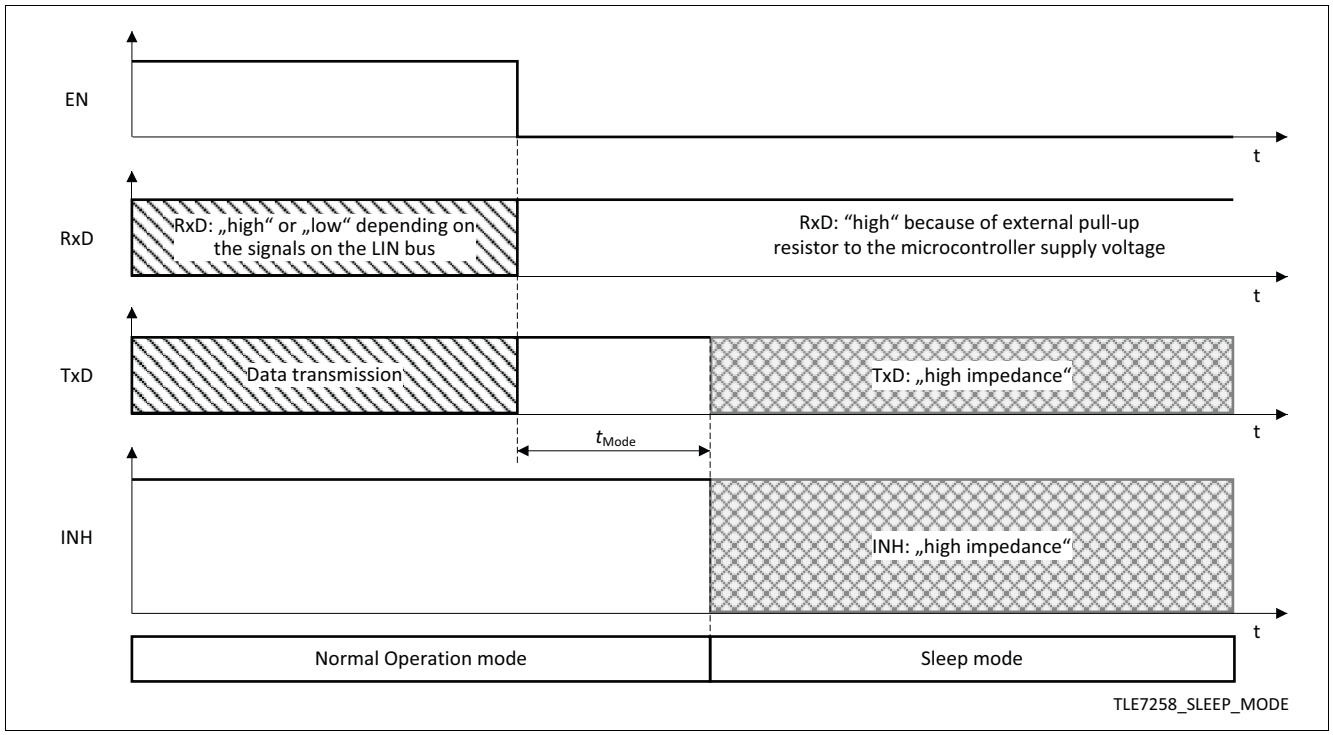


Figure 7 Entering sleep mode from normal operation mode

While the TLE7258 is in sleep mode the following functions are available:

- The transmitter is turned off.
- The receiver is turned off.
- The BUS output is terminated to V_S via the internal termination resistor R_{BUS} (see **Figure 1**).
- The RxD output is “high” if a pull-up resistor is connected to the external microcontroller supply.
- The TxD input is disabled and the internal pull-up current source is switched off.
- The INH output is switched off and is floating.
- The bus wake-up comparator is active and will cause transition to standby mode in case of a wake-up event.
- In sleep mode only the power-on reset level of the undervoltage detection is active (see **“Undervoltage detection” on Page 15**).
- The EN input remains active. A “high” signal on the EN input triggers a transition to normal operation mode.

3.5 Bus wake-up event

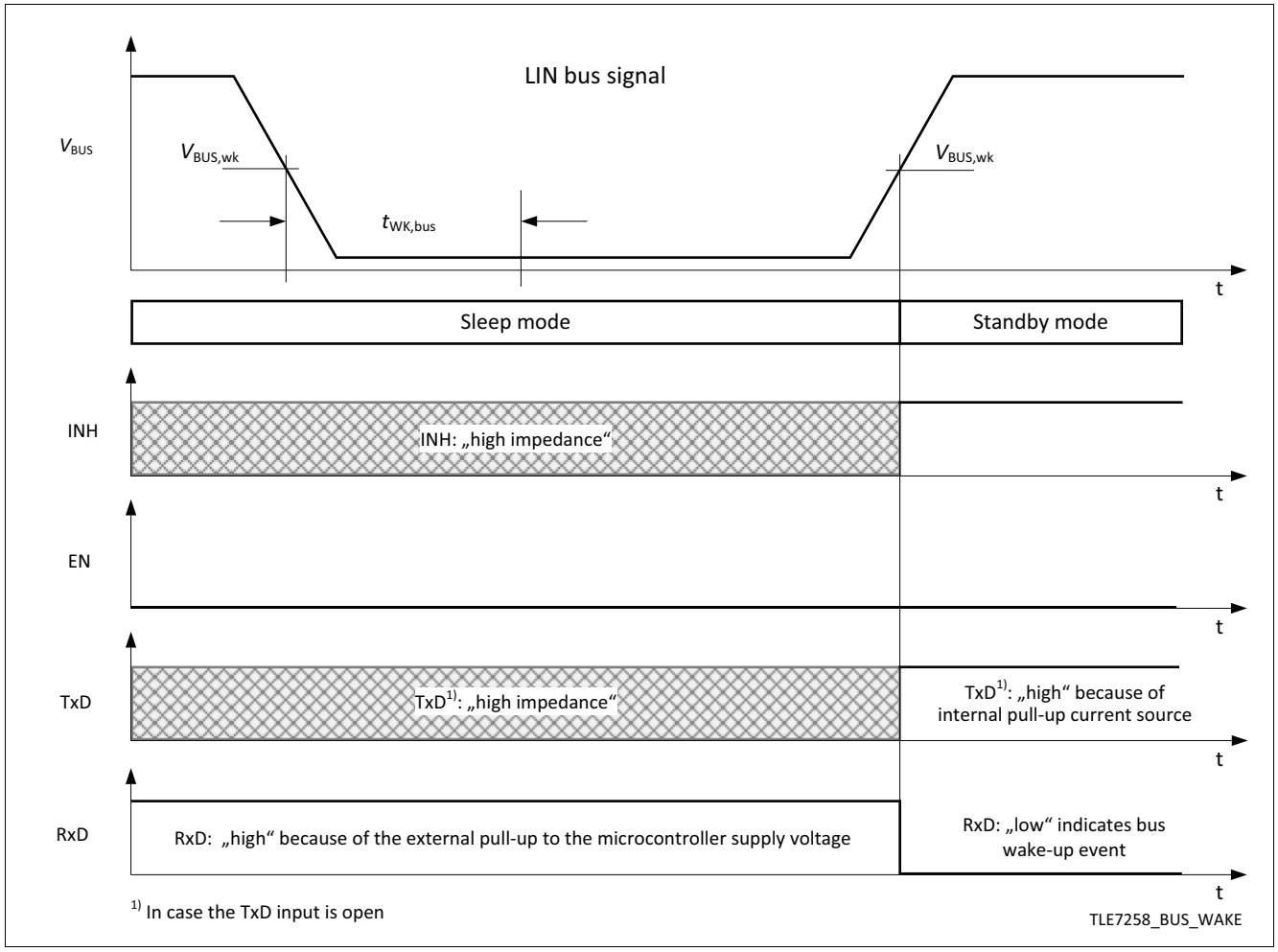


Figure 8 Bus wake-up behavior

A bus wake-up event, also called remote wake-up, changes the operation mode from sleep mode to standby mode. A falling edge on the LIN bus, followed by a “dominant” bus signal for the time $t_{WK,bus}$ results in a bus wake-up event. The mode change to standby mode becomes active with the following rising edge on the LIN bus. The TLE7258 remains in sleep mode until it detects a state change on the LIN bus from “dominant” to “recessive” (see **Figure 8**).

In standby mode a logical “low” signal on the RxD output indicates a bus wake-up event.

In case the TLE7258 detects a bus wake-up event while already being in standby mode after power-up, the wake-up event will be signaled with a logical “low” level on RxD and override the power-on wake source (see **Figure 6**).

3.6 Mode transition via EN input

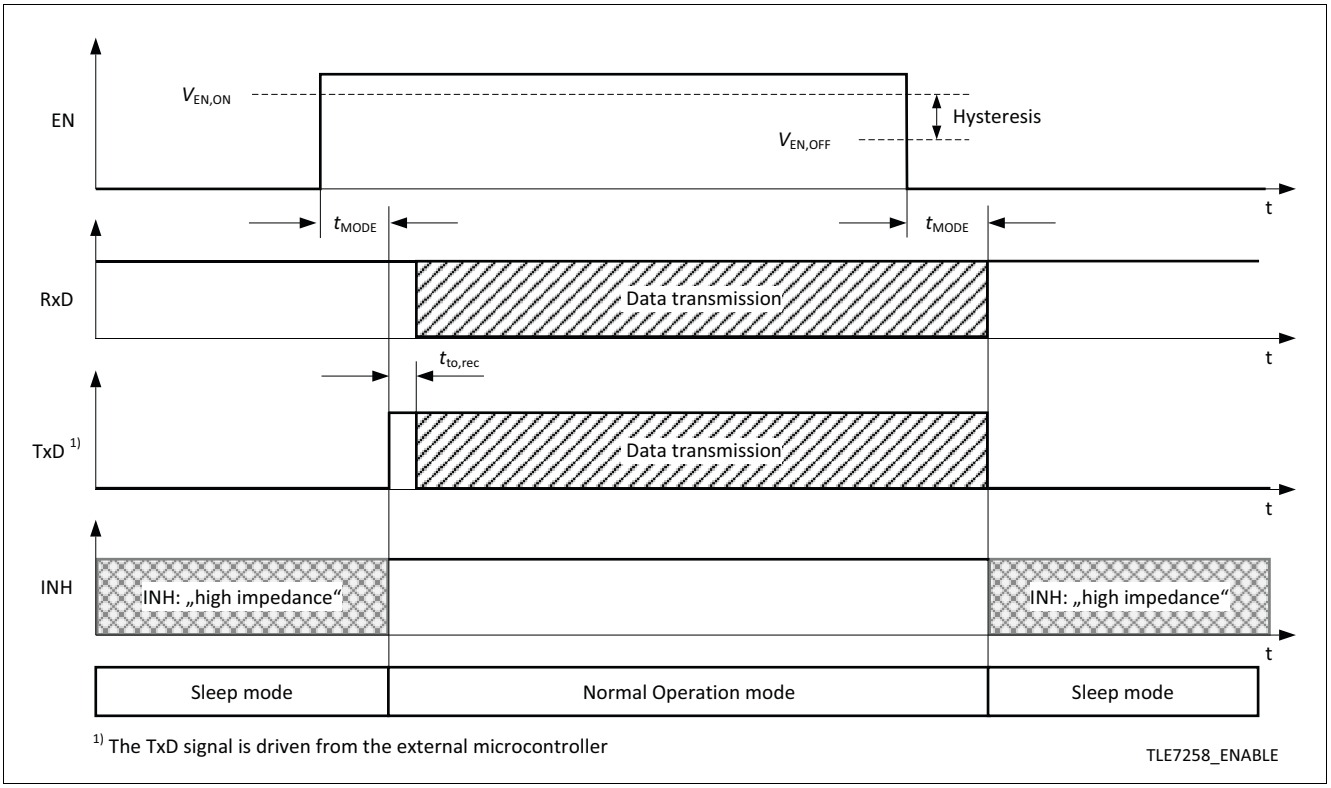


Figure 9 Entering normal operation mode from sleep mode

The EN input is used for operation mode control of the TLE7258. By setting the EN input logical “high” for the time tMODE while being sleep or standby mode, a transition to normal operation mode will be triggered (see **Figure 9**). The EN input has an integrated pull-down resistor to ensure the device remains in sleep or standby mode even if the EN pin is left open. The EN input has an integrated hysteresis.

A signal transition from logical “high” to “low” on the EN input changes the operation mode from normal operation mode to sleep mode (see **Figure 5**).

The TLE7258 changes the operation modes regardless of the signal on the BUS pin. In the case of a short circuit between the LIN bus and GND, resulting in a permanent “dominant” signal, the TLE7258 can be set to sleep mode by setting the EN input to logical “low”.

After a mode change to normal operation mode, a logical “high” signal for the time $t_{to,rec}$ on the TxD input is required to release the data communication.

3.7 Overtemperature protection

The TLE7258 has an integrated overtemperature sensor to protect the device against thermal overstress on the transmitter. In case of an overtemperature event, the transmitter will be disabled (see **Figure 10**). An overtemperature event will not cause any mode change and will not be directly indicated on the RxD output or the TxD input.

When the junction temperature falls below the thermal shut down level $T_J < T_{JSD}$, the transmitter will be reactivated. After an over-temperature recovery the TxD input requires a logical “high” signal before restarting data transmission.

A 10°C hysteresis avoids toggling during the temperature shut down.

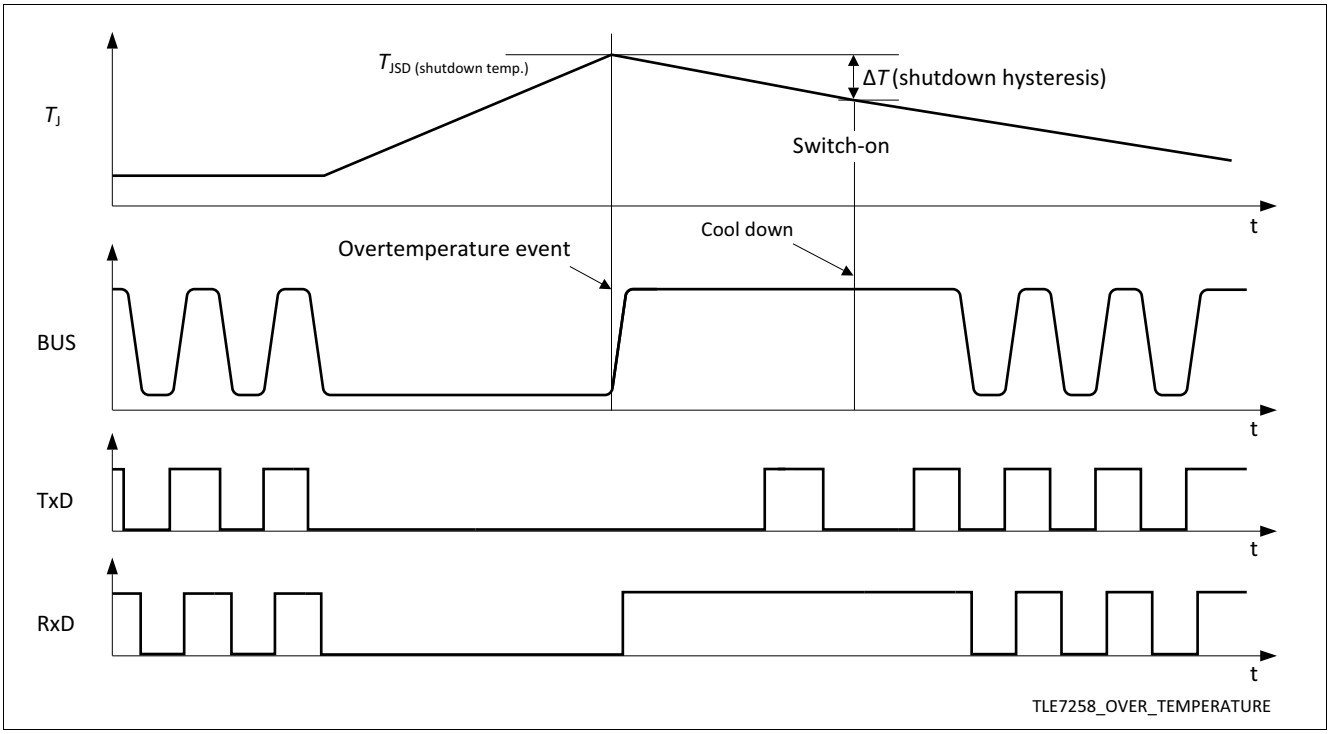


Figure 10 Overtemperature shut down

3.8 Undervoltage detection

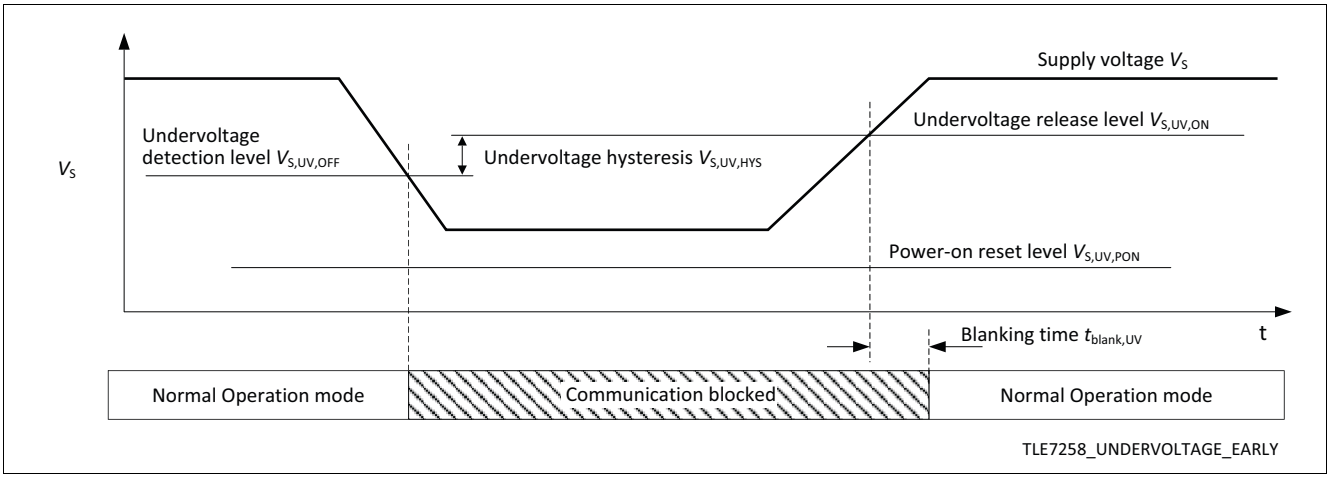


Figure 11 Early undervoltage detection

The TLE7258 has undervoltage detection on the V_S supply pin with two different thresholds:

- In normal operation mode the TLE7258 blocks the communication between the LIN bus and the microcontroller when detecting undervoltage events. However, no mode change will occur. After V_S rises above the undervoltage release level $V_{S,UV,REL}$, the bus communication interface will be released when the signal on the TxD input goes “high”. See **Figure 11**.
- In case the power supply V_S drops down below the power-on reset level $V_{S,UV,PON}$ the TLE7258 not only blocks the communication between the LIN bus and the microcontroller, it also changes the operation mode to standby mode after V_S supply recovery. In standby mode the TLE7258 indicates a power-up event on the RxD output. The power-on reset level is active in all operation modes.See **Figure 12**.

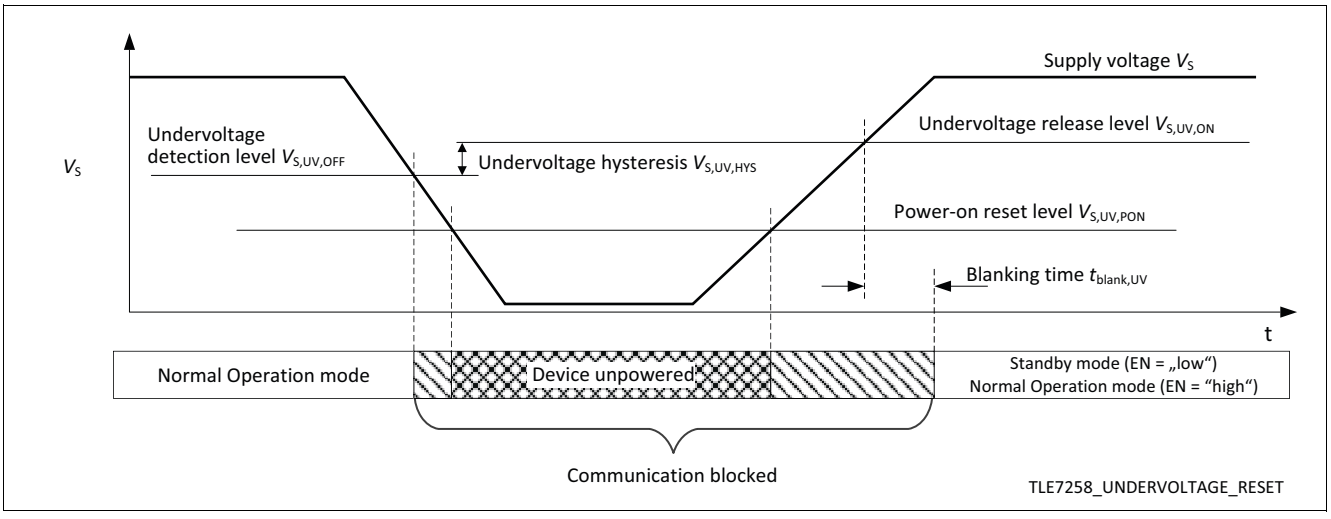


Figure 12 Undervoltage detection and power-on reset

3.9 TxD time-out

The TxD time-out feature protects the LIN bus against permanent blocking in case the logical signal on the TxD input is continuously “low”, caused by e.g. a malfunctioning microcontroller or a short circuit on the printed circuit board. In normal operation mode, a logical “low” signal on the TxD input for the time tTxD disables the output stage of the transmitter (see **Figure 13**). The receiver will remain active and the data on the bus are still monitored on the RxD output.

The TLE7258 will release the output stage after a TxD time-out event first when detecting a logical “high” signal on the TxD input for the time tto,rec.

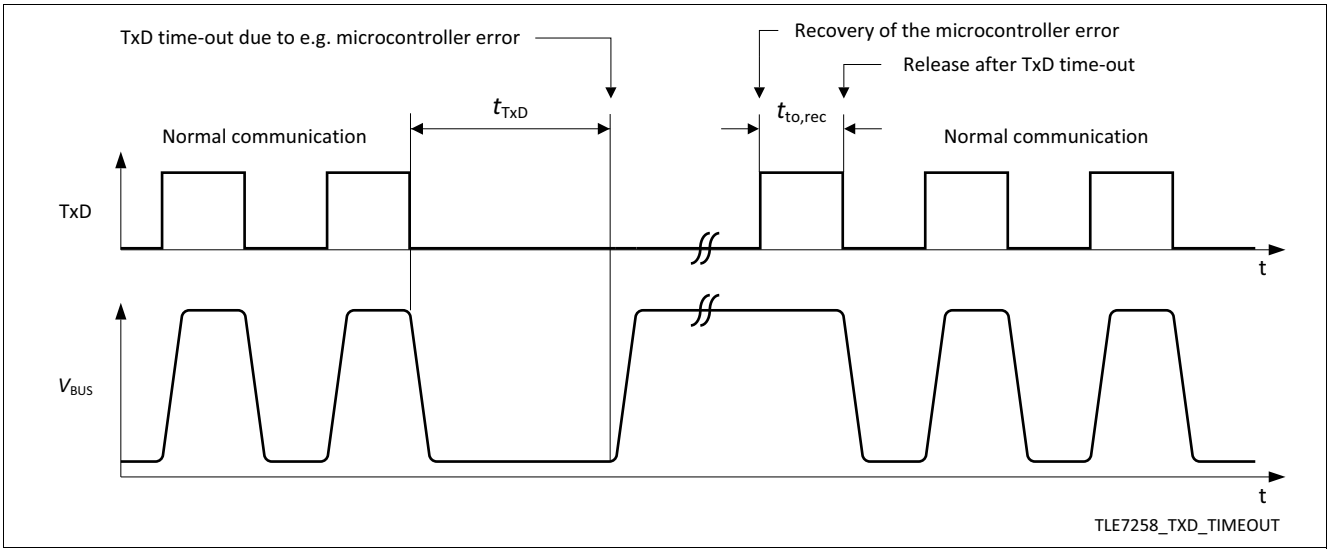


Figure 13 TxD time-out

3.10 3.3 V and 5 V logic capability

The TLE7258 can be used for 3.3 V and 5 V microcontrollers. The logic inputs and the outputs are capable to operate with both voltage levels. The RxD output needs an external pull-up resistor to the microcontroller supply to define the voltage level (see **Chapter 6.6 “RxD Pull-up resistor” on Page 26** and **Figure 16**).

3.11 Short circuit

The BUS pin of TLE7258 can withstand short circuits to either GND or to the V_S power supply. The integrated over-temperature protection may disable the transmitter in case of a permanent short circuit on the bus pin is causing the overheating.

4 General product characteristics

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin; unless otherwise specified

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Battery supply voltage	V_S	-0.3	–	40	V	LIN Spec 2.2A (Par. 11)	1.1.1
BUS input voltage	$V_{BUS,G}$	-27	–	40	V	–	1.1.2
Logic voltages at EN, TxD, RxD	V_{logic}	-0.3	–	6.0	V	–	1.1.3
INH voltage	V_{INH}	-0.3	–	V_S + 0.3	V	–	1.1.4
Currents							
Output current at RxD	I_{RxD}	0	–	15	mA	–	1.2.1
Output current at INH	I_{INH}	-5	–	5	mA	–	1.2.2
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	1.3.1
Storage temperature	T_s	-55	–	150	°C	–	1.3.2
ESD susceptibility							
Electrostatic discharge voltage at V_S, BUS	V_{ESD}	-10	–	10	kV	Human Body Model (100 pF via 1.5 kΩ)[2)]	1.4.1
Electrostatic discharge voltage all other pins	V_{ESD}	-4	–	4	kV	Human Body Model (100 pF via 1.5 kΩ)[2)]	1.4.2
Electrostatic discharge voltage all pins	V_{ESD}	-1	–	1	kV	Charged Device Model[3)]	1.4.3

1) Not subject to production test, specified by design
2) ESD susceptibility HBM according to ANSI / ESDA / JEDEC JS-001
3) ESD susceptibility, Charged Device Model “CDM” EIA / JESD 22-C101 or ESDA STM5.3.1

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Extended supply voltage range for operation	$V_{S(ext)}$	18	–	40	V	Parameter deviations possible	2.1.1
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	18	V	LIN Spec 2.2A (Par. 10)	2.1.2
Thermal parameters							
Junction temperature	T_j	-40	–	150	°C	1)	2.2.1

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal characteristics

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 5 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistance, PG-DSO-8 package version							
Junction ambient	R_{thJA}	–	130	–	K/W	2)	3.1.1
Thermal resistance, PG-TSON-8 package version							
Junction ambient	R_{thJA}	–	60	–	K/W	2)	3.2.1
		–	190	–	K/W	3)	3.2.2
		–	70	–	K/W	300 mm2 heatsink on PCB[3)]	3.2.3
Thermal shutdown junction temperature							
Thermal shutdown temperature	T_{JSD}	150	175	200	°C	–	3.3.1
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	3.3.2

1) Not subject to production test, specified by design

2) Specified RthJA value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (TLE7258) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 mm Cu, 2 x 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted to the first inner copper layer.

3) Specified RthJA value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board; The product (TLE7258) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1 inner copper layer (1 x 70 mm Cu).

5 Electrical characteristics

5.1 Functional device characteristics

Table 6 Electrical characteristics

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption							
Current consumption at V_S, Recessive state	$I_{S,rec}$	0.1	0.6	2.0	mA	INH open, without R_L; V_{TxD} = “high”	4.1.1
Current consumption at V_S, Dominate state	$I_{S,dom}$	0.1	1.1	3.0	mA	INH open, without R_L; V_{TxD} = 0 V	4.1.2
Current consumption at V_S, Standby mode	$I_{S,standby}$	100	350	900	µA	Standby mode, V_{BUS} = V_S	4.1.3
Current consumption at V_S, Sleep mode	$I_{S,sleep,typ}$	1	10	15	µA	Sleep mode, T_j < 40 °C; V_S = 13.5 V; V_{BUS} = V_S	4.1.4
Current consumption at V_S, Sleep mode	$I_{S,sleep}$	1	10	25	µA	Sleep mode, V_{BUS} = V_S	4.1.5
Current consumption at V_S, Sleep mode. Bus shorted to GND	I_{S,SC_GND}	100	–	700	µA	Sleep mode, V_S = 13.5 V; V_{BUS} = 0 V	4.1.6
Undervoltage detection							
Power-on reset level on V_S	$V_{S,UV,PON}$	–	–	4.3	V	Reset level for mode change	4.2.1
Undervoltage threshold, V_S on	$V_{S,UV,ON}$	4.7	5.15	5.5	V	Rising edge	4.2.2
Undervoltage threshold, V_S off	$V_{S,UV,OFF}$	4.4	4.85	5.2	V	Falling edge	4.2.3
Undervoltage detection hysteresis	$V_{S,UV,HYS}$	–	300	–	mV	1)	4.2.4
Undervoltage blanking time	$t_{BLANK,UV}$	–	10	–	µs	1)	4.2.5
Receiver output: RxD							
“High” level leakage current	$I_{RD,H,leak}$	–	–	5	µA	V_{RxD} = 5 V; V_{BUS} = V_S	4.3.1
“Low” level output current	$I_{RD,L}$	1.3	–	–	mA	V_{RxD} = 0.4 V; V_{BUS} = 0 V	4.3.2
Transmission input: TxD							
“High” level input voltage range	$V_{TD,H}$	2	–	6.0	V	Recessive state	4.4.1
“Low” level input voltage range	$V_{TD,L}$	-0.3	–	0.8	V	Dominant state	4.4.2
Input hysteresis	$V_{TD,hys}$	–	200	–	mV	1)	4.4.3

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pull-up current	I_{TD}	-60	–	-20	µA	V_{TxD} = 0 V; Normal operation mode or standby mode	4.4.4
Enable input: EN							
"High" level input voltage range	$V_{EN,ON}$	2	–	6.0	V	Normal operation mode	4.5.1
"Low" level input voltage range	$V_{EN,OFF}$	-0.3	–	0.8	V	Sleep mode or standby mode	4.5.2
Input hysteresis	$V_{EN,hys}$	–	200	–	mV	1)	4.5.3
Pull-down resistance	R_{EN}	15	30	60	kΩ	–	4.5.4
Inhibit output: INH							
Inhibit voltage drop	ΔV_{INH}	–	–	1.0	V	I_{INH} = -2.0 mA	4.6.1
Leakage current	$I_{INH,lk}$	-5.0	–	5.0	µA	Sleep mode; V_{INH} = 0 V	4.6.2
Bus receiver: BUS							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.44 × V_S	–	V	–	4.7.1
Receiver dominant state	V_{BUSdom}	–	–	0.4 × V_S	V	LIN Spec 2.2A (Par. 17)	4.7.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	–	0.56 × V_S	0.6 × V_S	V	–	4.7.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	–	V	LIN Spec 2.2A (Par. 18)	4.7.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	LIN Spec 2.2A (Par. 19)2)	4.7.5
Receiver hysteresis	V_{HYS}	0.07 × V_S	0.12 × V_S	0.175 × V_S	V	LIN Spec 2.2A (Par. 20)3)	4.7.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.40 × V_S	0.5 × V_S	0.6 × V_S	V	–	4.7.7
Bus Transmitter: BUS							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = "high"; Open load	4.8.1
Bus short circuit current	I_{BUS_LIM}	40	85	125	mA	V_{BUS} = 13.5 V; LIN Spec 2.2A (Par. 12);	4.8.2
Leakage current	$I_{BUS\_NO\_GND}$	-1	-0.5	–	mA	V_S = 0 V; V_{BUS} = -12 V; LIN Spec 2.2A (Par. 15)	4.8.3
Leakage current	$I_{BUS\_NO\_BAT}$	–	1	5	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2A (Par. 16)	4.8.4
Leakage current	$I_{BUS\_PAS\_dom}$	-1	-0.5	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2A (Par. 13)	4.8.5

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 18 V; R_L = 500 Ω; -40 °C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Leakage current	$I_{BUS\_PAS\_rec}$	–	1	5	µA	V_S = 8 V; V_{BUS} = 18 V;	4.8.6
Forward voltage serial diode	$V_{SerDiode}$	0.4	–	1.0	V	$I_{SerDiode}$ = 75 µA; LIN Spec 2.2A (Par. 21)	4.8.7
Bus pull-up resistance	R_{slave}	20	40	60	kΩ	LIN Spec 2.2A (Par. 26)	4.8.8
Bus dominant output voltage maximum load	$V_{BUS,do}$	 – –	 – –	 1.4 2.0	 V V	V_{TxD} = 0 V; R_L = 500 Ω; V_S = 7 V; V_S = 18 V;	4.8.9
Dynamic Transceiver Characteristics							
Propagation delay: LIN bus dominant to RxD "low" LIN bus recessive to RxD "high"	 t_{rx_pdft} t_{rx_pdr}	 1 1	 3.5 3.5	 6 6	 µs µs	LIN Spec 2.2A (Par. 31) R_{RxD} = 2.4 kΩ; C_{RxD} = 20 pF	4.9.1
Receiver delay symmetry	t_{rx_sym}	-2	–	2	µs	LIN Spec 2.2A (Par. 32) $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$; R_{RxD} = 2.4 kΩ; C_{RxD} = 20 pF	4.9.2
Dominant time for bus wake-up	$t_{WK,bus}$	30	–	150	µs	–	4.9.3
Delay time for mode change	t_{MODE}	–	–	50	µs	[4]	4.9.4
TxD time-out	t_{TxD}	8	18	28	ms	–	4.9.5
TxD recessive time to release transmitter	$t_{to,rec}$	–	–	10	µs	[1]	4.9.6
Duty cycle D1 (for worst case at 20 kBit/s)	*D1*	0.396	–	–	–	Duty cycle 1 [5] $TH_{Rec}(max) = 0.744 \times V_S$; $TH_{Dom}(max) = 0.581 \times V_S$; V_S = 7.0 … 18 V; t_{bit} = 50 µs; $D1 = t_{bus\_rec(min)} / 2 \times t_{bit}$; LIN Spec 2.2A (Par. 27)	4.9.7
Duty cycle D1 for V_S supply 5.5 V to 7.0 V (for worst case at 20 kBit/s)	*D1*	0.396	–	–	–	Duty cycle 1 [5] $TH_{Rec}(max) = 0.760 \times V_S$; $TH_{Dom}(max) = 0.593 \times V_S$; 5.5 V < V_S < 7.0 V; t_{bit} = 50 µs; $D1 = t_{bus\_rec(min)} / 2 \times t_{bit}$	4.9.8
Duty cycle D2 (for worst case at 20 kBit/s)	*D2*	–	–	0.581	–	Duty cycle 2 [5] $TH_{Rec}(min) = 0.422 \times V_S$; $TH_{Dom}(min) = 0.284 \times V_S$; V_S = 7.6 … 18 V; t_{bit} = 50 µs; $D2 = t_{bus\_rec(max)} / 2 \times t_{bit}$; LIN Spec 2.2A (Par. 28)	4.9.9

Table 6 Electrical characteristics (cont'd)

5.5 V < V_S < 18 V; R_L = 500 Ω; -40°C < T_j < 150°C;
all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Duty cycle D2 for V_S supply 6.1 V to 7.6 V (for worst case at 20 kBit/s)	*D2*	–	–	0.581	–	Duty cycle 2 [5] TH_{Rec}(min)= 0.410 × V_S; TH_{Dom}(min)= 0.275 × V_S; 6.1 V < V_S < 7.6 V; t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$ / 2 × t_{bit}	4.9.10
Duty cycle D3 (for worst case at 10.4 kBit/s)	*D3*	0.417	–	–	–	Duty cycle 3 [5] TH_{Rec}(max) = 0.778 × V_S; TH_{Dom}(max) =0.616 × V_S; V_S = 7.0 … 18 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$ / 2 × t_{bit}; LIN Spec 2.2A (Par. 29)	4.9.11
Duty cycle D3 for V_S supply 5.5 V to 7.0 V (for worst case at 10.4 kBit/s)	*D3*	0.417	–	–	–	Duty cycle 3 [5] TH_{Rec}(max) = 0.797 × V_S; TH_{Dom}(max) = 0.630 × V_S; 5.5 V < V_S < 7.0 V; t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$ / 2 × t_{bit};	4.9.12
Duty cycle D4 (for worst case at 10.4 kBit/s)	*D4*	–	–	0.590	–	Duty cycle 4 [5] TH_{Rec}(min) = 0.389 × V_S; TH_{Dom}(min) = 0.251 × V_S; V_S = 7.6 … 18 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$ / 2 × t_{bit}; LIN Spec 2.2A (Par. 30)	4.9.13
Duty cycle D4 for V_S supply 6.1 V to 7.6 V (for worst case at 10.4 kBit/s)	*D4*	–	–	0.590	–	Duty cycle 4 [5] TH_{Rec}(min) = 0.378 × V_S; TH_{Dom}(min)= 0.242 × V_S; 6.1 V < V_S < 7.6 V; t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$ / 2 × t_{bit};	4.9.14

1) Not subject to production test, specified by design
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec}) / 2$
3) $V_{HYS} = V_{th\_rec} - V_{th\_dom}$
4) Delay time specified for a load of 10 kΩ / 20 pF on the INH output
5) Bus load concerning LIN Spec 2.2A:
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_L
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_L
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_L

5.2 Diagrams

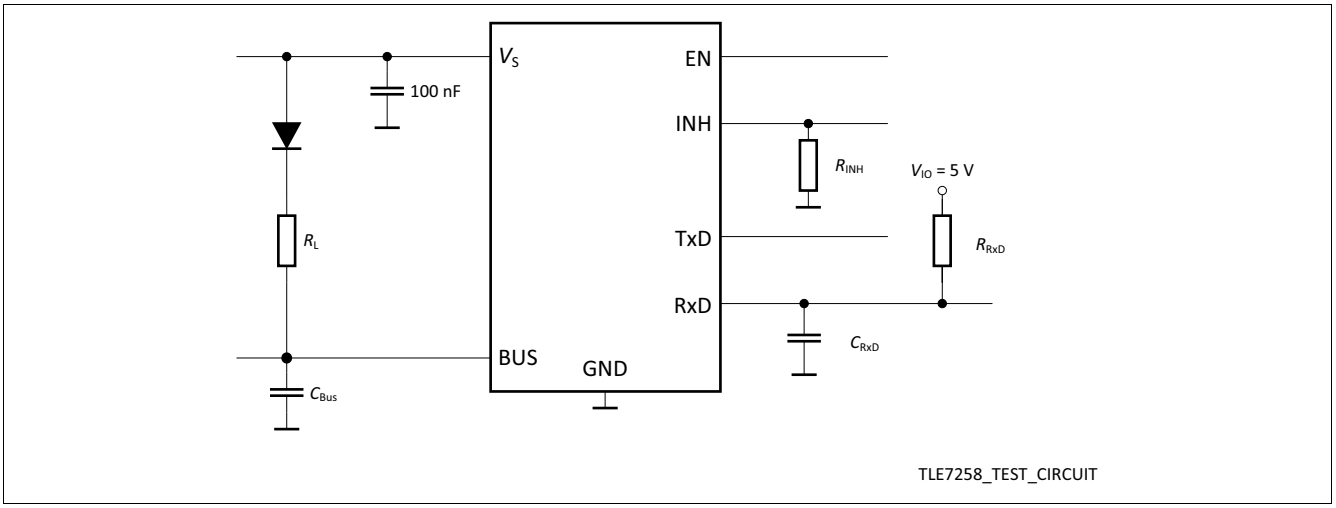


Figure 14 Simplified test circuit

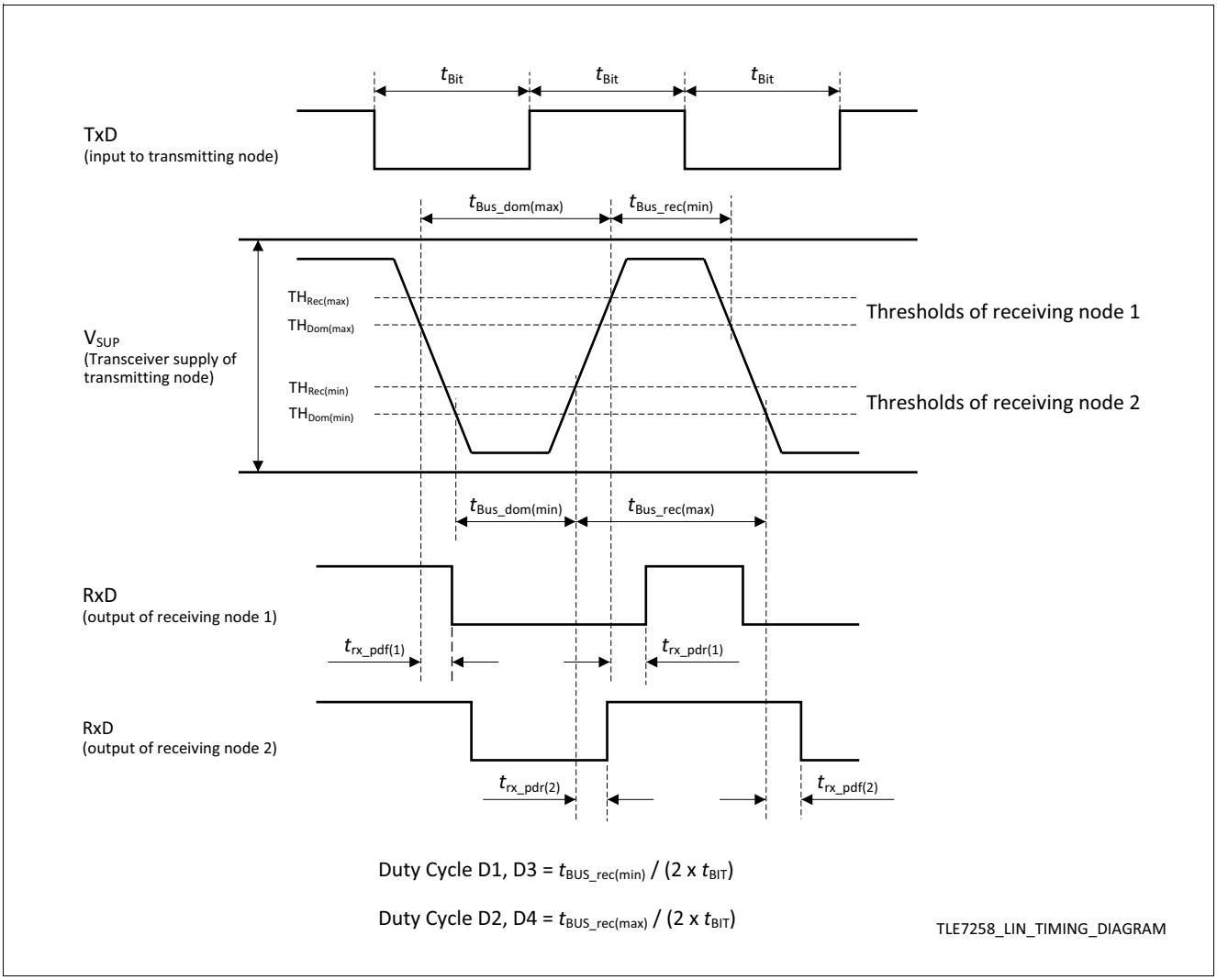


Figure 15 Timing diagram for dynamic characteristics

6 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

6.1 Application example

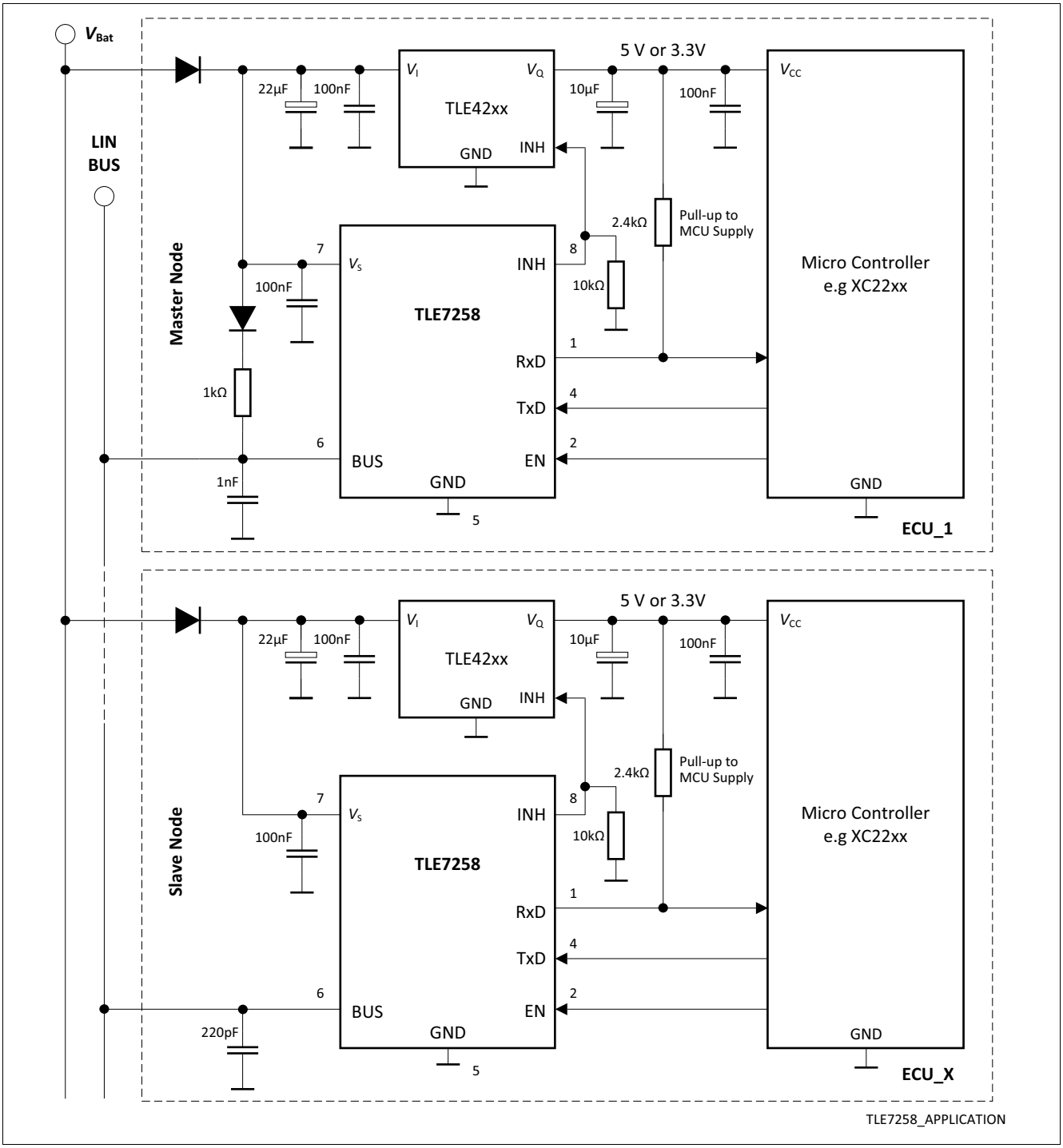


Figure 16 Simplified application circuit

6.2 ESD Susceptibility according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 7 ESD Susceptibility according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin V_S, BUS versus GND	+10	kV	1)Positive pulse
Electrostatic discharge voltage at pin V_S, BUS versus GND	-10	kV	1)Negative pulse

1) ESD susceptibility “ESD GUN” according IEC 61000-4-2, tested by external test house.

6.3 Transient robustness according to ISO 7637-2

Test for transient robustness according to ISO 7637-2 have been performed. The results and test conditions are available in a separate test report.

Table 8 Automotive Transient Robustness according to ISO 7637-2

Performed Test	Result	Unit	Remarks
Pulse 1	-100	V	1)
Pulse 2	+75	V	1)
Pulse 3a	-150	V	1)
Pulse 3b	+100	V	1)

1) Automotive Transient Robustness according to ISO 7637-2, tested by external test house.

6.4 LIN Physical layer compatibility

The TLE7258 fulfills the Physical Layer Specification of LIN 1.2, 1.3, 2.0, 2.1, 2.2 and 2.2A.

The differences between LIN specification 1.2 and 1.3 is mainly the physical layer specification. The reason was to improve the compatibility between the nodes.

The LIN specification 2.0 is a super set of the 1.3 version. The 2.0 version offers new features. However, it is possible to use the LIN 1.3 slave node in a 2.0 node cluster, as long as the new features are not used. Vice versa it is possible to use a LIN 2.0 node in the 1.3 cluster without using the new features.

In terms of the physical layer the LIN 2.1, LIN 2.2 and LIN 2.2A Specification does not include any changes and is fully compliant to the LIN Specification 2.0.

LIN 2.2A is the latest version of the LIN specification, released in December 2010. The physical layer specification of LIN 2.2A will be included in the ISO 17987-4 without modifications.

Additionally, the TLE7258 is compliant to the SAE J2602-2 standard for usage in the US automotive market.

6.5 TxD Fail-safe input

The TxD input has an internal pull-up structure to avoid any bus disturbance in case the TxD input is open and floating. In case of an not connected TxD input, the pin is pulled to an internal voltage supply (see **Figure 1**) and the output to the LIN bus on the BUS pin is always “recessive”. Therefore the TLE7258 can not disturb the communication on the LIN bus.

In order to optimize the quiescent current of the TLE7258 in sleep mode, the pull-up structure inside the TxD input is disabled in sleep mode. The logic inside the TxD input is not reacting at any signal change provide to the TxD input pin and the transmitter is turned off. In sleep mode the TLE7258 can not disturb or block the LIN bus in any case.

Table 9 TxD termination

Operation mode	Remarks
Normal operation mode	The internal pull-up structure is active, in case the TxD input is open the TxD input signal is “high” and the output on the BUS pin is “recessive”
Standby mode	The internal pull-up structure is active, in case the TxD input is open the TxD input signal is “high”. In Standby mode the transmitter is turned off and therefore the output on the BUS pin always is “recessive”
Sleep mode	The internal pull-up structure is inactive, in case the TxD input is open the TxD input signal is “floating”. In sleep mode the transmitter is turned off and therefore the output on the BUS pin always is “recessive”

6.6 RxD Pull-up resistor

The receive data output (RxD) provides an open drain behavior for allowing the output level to be adapted to the microcontroller supply voltage. Thus 3.3 V microcontroller derivatives without 5 V tolerant ports can be used. In case the microcontroller port pin does not provide an integrated pull-up, an external pull-up resistor connected to the microcontroller’s V_{CC} supply voltage is required.

The typical RxD pin current / voltage characteristic over temperature is given in **Figure 17**. With the applications microcontroller port pins’ (Rx) minimum “high”-level and maximum “low”-level input voltage the pull-up resistor can be dimensioned. For most applications a pull-up resistor R_{Rx} of 2.4 kΩ is recommended.

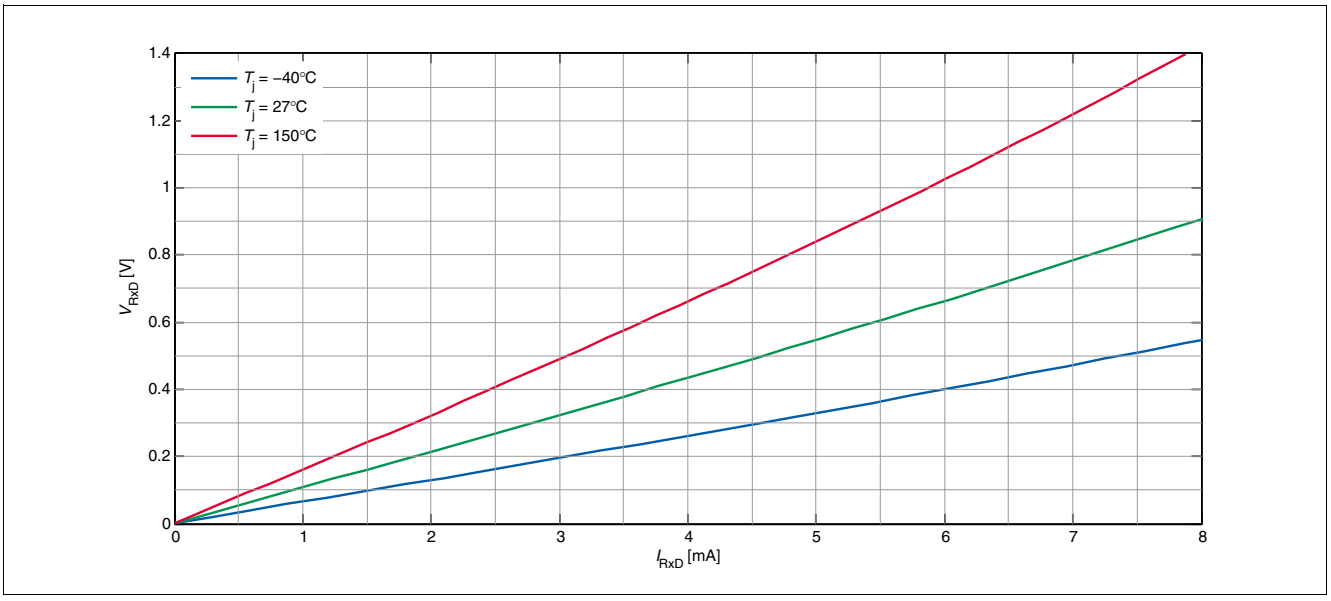


Figure 17 Typical RxD output sink characteristics

6.7 Compatibility with other Infineon LIN transceivers

Infineon offers a complete LIN transceiver family consisting of devices in PG-DSO-8 package (TLE7257SJ, TLE7258SJ and TLE7259-3GE) and PG-TSON-8 package (TLE7257LE, TLE7258D, TLE7258LE and TLE7259-3LE). All these devices are pin-to-pin compatible, with the only differences at the pins named N.C. (= Not Connected). The N.C. pins can be left open on the PCB in applications where these functionalities are not needed. The N.C. pins are internally not bonded, so the devices will not be affected if these pins are connected to signals on the application PCB.

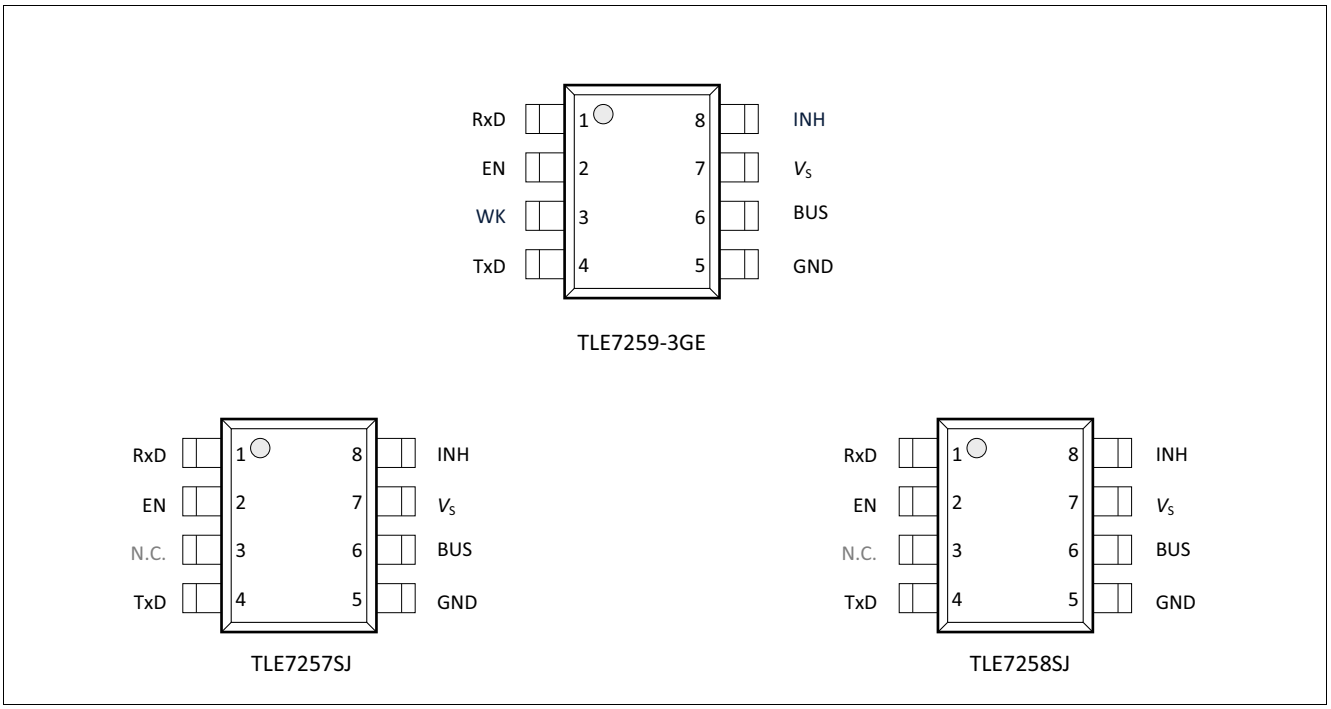


Figure 18 Pin compatibility between TLE7257SJ, TLE7258SJ and TLE7259-3GE

Table 10 Functionality of LIN transceiver family, PG-DSO-8 package

Device	TLE7257SJ	TLE7258SJ	TLE7259-3GE
Applications	Standard LIN Master node	Standard LIN Slave node	High End LIN All kind of nodes
Features			
Fast Programming mode	–	–	✓
Local Wake input	–	–	✓
Inhibit output usage	VREG control	VREG control	VREG control Master Termination
TxD Time-out	✓	✓	✓
Power-Up mode	Sleep mode	Standby mode	Standby mode

The functional difference between the devices in the Infineon LIN transceiver family is summarized in **Table 10** and in **Table 11**. For mode details on the functional and parametric differences, please refer to the respective part's datasheet.

Application information

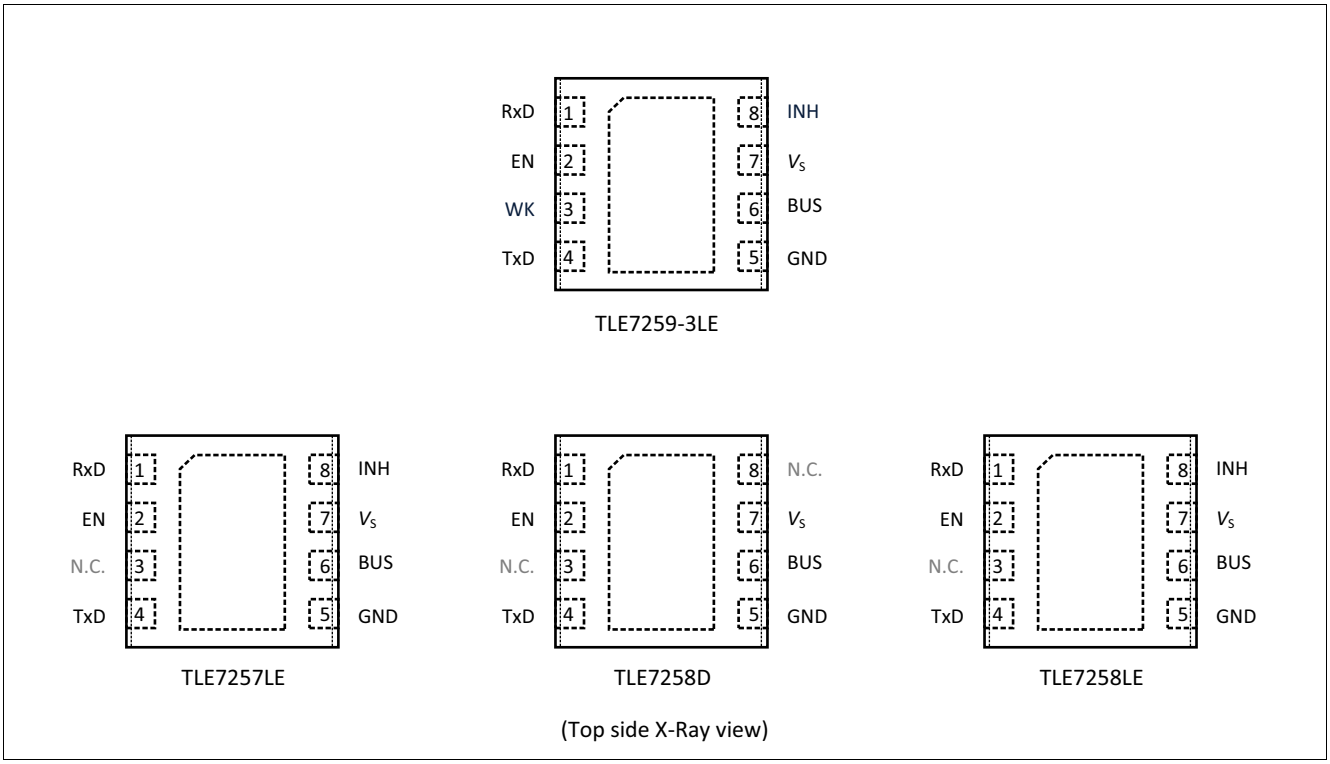


Figure 19 Pin compatibility between TLE7257LE, TLE7258LE, TLE7258D and TLE7259-3LE

Table 11 Functionality of LIN transceiver family, PG-TSON-8 package

Device	TLE7257LE	TLE7258LE	TLE7258D	TLE7259-3LE
Applications	Standard LIN Master node	Standard LIN Slave node	K-line MOST ECL	High end LIN All kind of nodes
Features				
Fast Programming mode	–	–	–	✓
Local Wake input	–	–	–	✓
Inhibit output usage	VREG control	VREG control	–	VREG control master termination
TxD Time-out	✓	✓	–	✓
Power-Up mode	Sleep mode	Standby mode	Standby mode	Standby mode

7 Package outlines

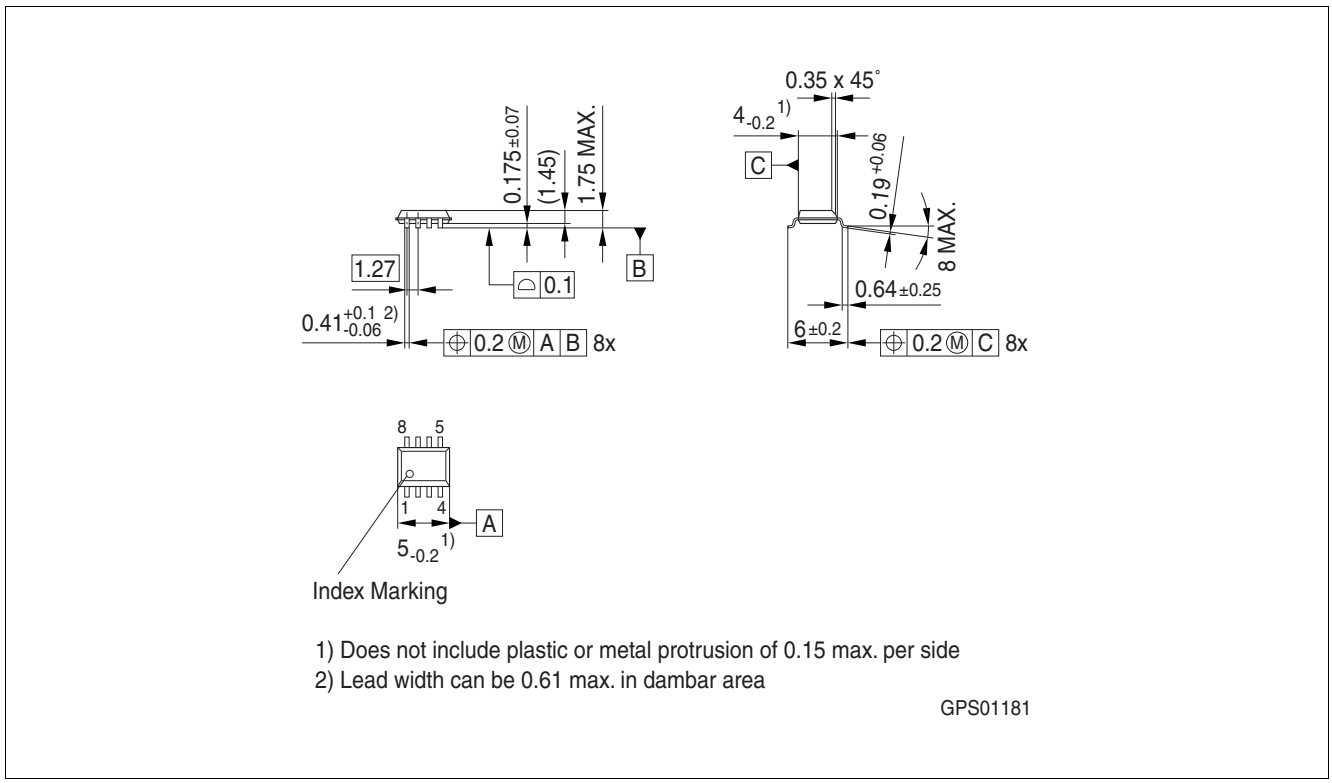


Figure 20 PG-DSO-8 (Plastic dual small outline PG-DSO-8)

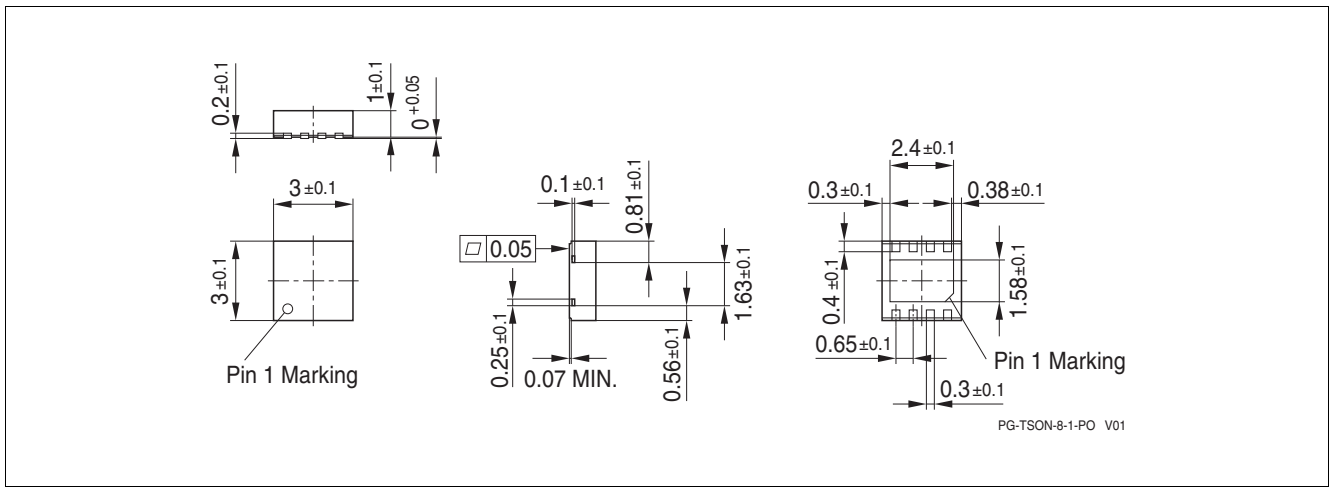


Figure 21 PG-TSON-8 (Plastic thin small outline nonleaded PG-TSON-8)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision history

Table 12 Revision history

Revision	Data	Changes
1.2	2022-04-27	Updated layout and template
1.1	2015-8-20	Data sheet updated based on Data sheet rev. 1.0 Marking of SJ type updated
1.0	2013-10-16	Data Sheet created.

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