



## Overview

### Basic Features

- 16-bit serial peripheral interface for control and diagnosis
- Daisy Chain capability SPI also compatible with 8-bit SPI devices
- 2 CMOS compatible parallel input pins with Input Mapping functionality
- Cranking capability down to  $V_S = 3.0\text{ V}$  (supports LV124)
- Digital supply voltage range compatible with 3.3 V and 5 V microcontrollers
- Very low quiescent current (with usage of IDLE pin)
- Limp Home mode (with usage of IDLE and IN pins)
- Green Product (RoHS compliant)
- AEC Qualified

### Protection Features

- Reverse battery protection on  $V_S$  without external components
- Short circuit to ground and battery protection
- Stable behavior at under voltage conditions (“Lower Supply Voltage Range for Extended Operation”)
- Over Current latch OFF
- Thermal shutdown latch OFF
- Overvoltage protection
- Loss of ground protection
- Loss of battery protection
- Electrostatic discharge (ESD) protection

### Diagnostic Features

- Latched diagnostic information via SPI register
- Over Load detection at ON state
- Open Load detection at OFF state using Output Status Monitor function
- Output Status Monitor
- Input Status Monitor

### Application Specific Features

- Fail-safe activation via Input pins in Limp-Home Mode
- SPI with Daisy Chain capability
- Safe operation at low battery voltage (cranking)

### Description

The TLE75004-EPD is a four channel low-side power switch in PG-TSDSO-14 package providing embedded protective functions. It is specially designed to control relays and LEDs in automotive and industrial applications.

A serial peripheral interface (SPI) is utilized for control and diagnosis of the loads as well as of the device. For direct control and PWM there are two input pins available connected to two outputs by default. Additional or different outputs can be controlled by the same input pins (programmable via SPI).

**Overview**

**Table 1 Product Summary**

Parameter	Symbol	Values
Analog supply voltage	$V_S$	3.0 V ... 28 V
Digital supply voltage	$V_{DD}$	3.0 V ... 5.5 V
Minimum overvoltage protection	$V_{S(AZ)}$	42 V (see <a href="#">Chapter 8.5</a> for details)
Maximum on-state resistance at $T_J = 150\text{ °C}$	$R_{DS(ON)}$	2.2 $\Omega$
Nominal load current ( $T_A = 85\text{ °C}$ , all channels)	$I_{L(NOM)}$	470 mA
Maximum Energy dissipation - repetitive	$E_{AR}$	10 mJ @ $I_{L(EAR)} = 220\text{ mA}$
Minimum Drain to Source clamping voltage	$V_{DS(CL)}$	42 V
Maximum overload switch OFF threshold	$I_{L(OVLO)}$	2.3 A
Maximum total quiescent current at $T_J \leq 85\text{ °C}$	$I_{SLEEP}$	5 $\mu\text{A}$
Maximum SPI clock frequency	$f_{SCLK}$	5 MHz

**Detailed Description**

The TLE75004-EPD is a four channel low-side switch providing embedded protective functions. The output stages incorporate four low-side switches (typical  $R_{DS(ON)}$  at  $T_J = 25\text{ °C}$  is 1  $\Omega$ ).

The 16-bit serial peripheral interface (SPI) is utilized to control and diagnose the device and the loads. The SPI interface provides daisy chain capability in order to assemble multiple devices (also devices with 8 bit SPI) in one SPI chain by using the same number of microcontroller pins.

This device is designed for low supply voltage operation, therefore being able to keep its state at low battery voltage ( $V_S \geq 3.0\text{ V}$ ). The SPI functionality, including the possibility to program the device, is available only when the digital power supply is present (see [Chapter 6](#) for more details).

The TLE75004-EPD is equipped with two input pins that are connected to two outputs, making them controllable even when the digital supply voltage is not available. With the Input Mapping functionality it is possible to connect the input pins to different outputs, or assign more outputs to the same input pin. In this case more channels can be controlled with one signal applied to one input pin.

In Limp Home mode (Fail-Safe mode) the input pins are directly routed to channels 2 and 3. When IDLE pin is “low”, it is possible to activate the two channels using the input pins independently from the presence of the digital supply voltage.

The device provides diagnosis of the load via Open Load at OFF state (with **DIAG\_OSM.OUTn** bits) and short circuit detection. For Open Load at OFF state detection, an internal current source  $I_{OL}$  can be activated via SPI.

Each output stage is protected against short circuit. In case of Overload, the affected channel switches OFF when the Overload Detection Current  $I_{L(OVLn)}$  is reached and can be reactivated via SPI. In Limp Home mode operation, the channels connected to an input pin set to “high” restart automatically after Output Restart time  $t_{RETRY(LH)}$  is elapsed. Temperature sensors are available for each channel to protect the device against Over Temperature.

The power transistors are built by N-channel power MOSFET . The inputs are ground referenced TTL compatible. The device is monolithically integrated in Smart Power Technology.

Block Diagram and Terms

## 2 Block Diagram and Terms

### 2.1 Block Diagram

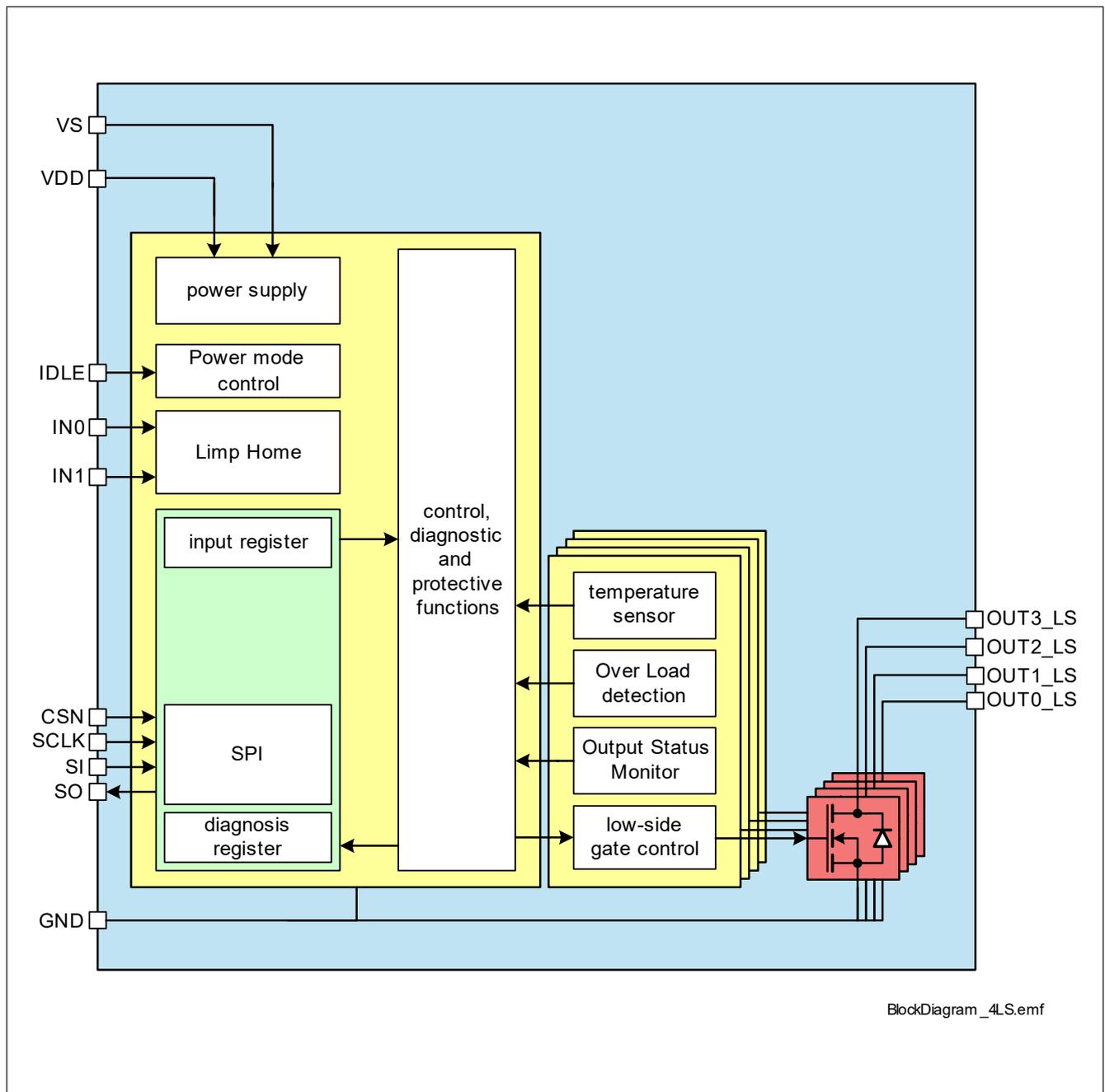


Figure 2 Block Diagram of TLE75004-EPD

Block Diagram and Terms

2.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

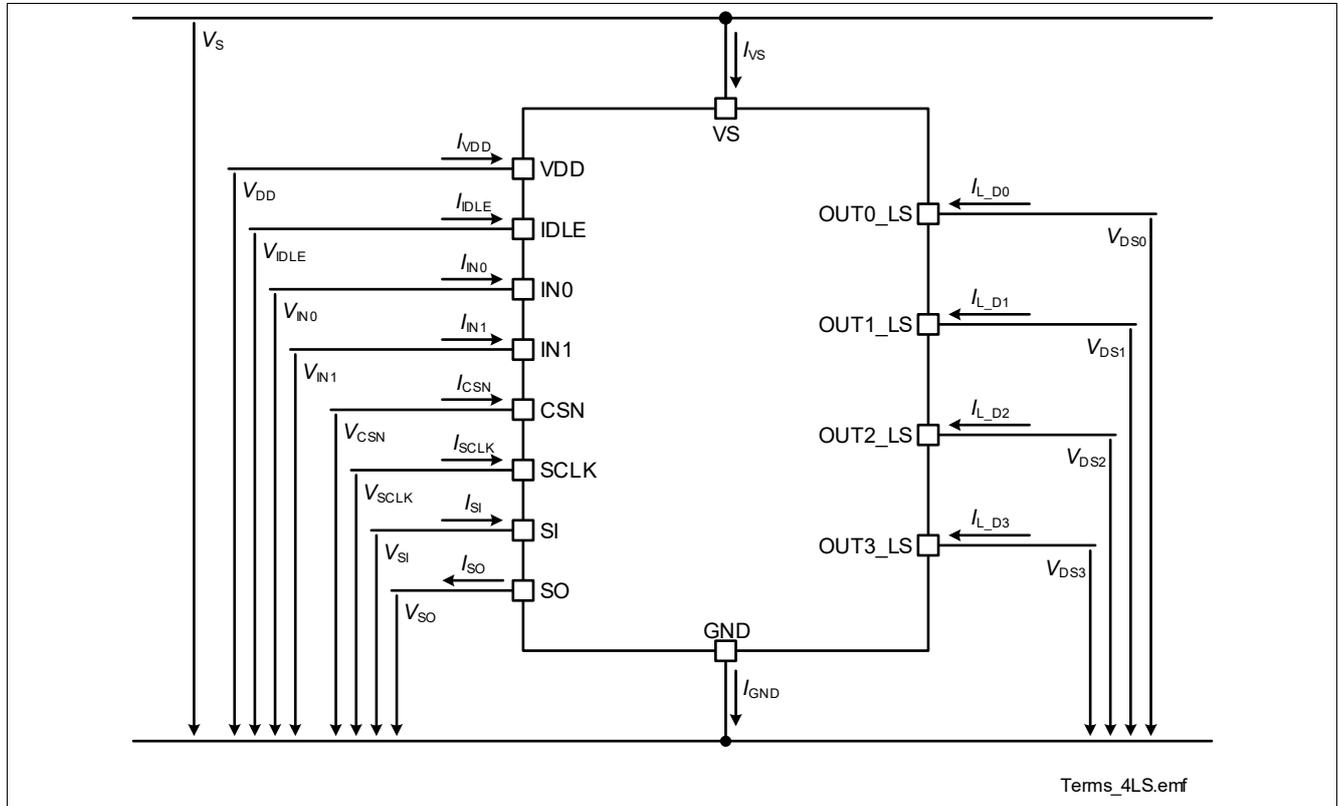


Figure 3 Voltage and Current definition

In all tables of electrical characteristics the channel related symbols without channel numbers are valid for each channel separately (e.g.  $V_{DS}$  specification is valid for  $V_{DS0} \dots V_{DS3}$ ).

Furthermore, parameters relative to output current can be indicated without specifying whether the current is going into the Drain pin or going out of the Source pin, unless otherwise specified. For instance, nominal output current can be indicated in the following ways:  $I_{L(NOM)}$   $I_{L\_LS(NOM)}$   $I_{L\_D(NOM)}$

All SPI registers bits are marked as follows: ADDR . PARAMETER (e.g. HWCR . RST) with the exception of the bits in the Diagnosis frames which are marked only with PARAMETER (e.g. UVRVS).

Pin Configuration

### 3 Pin Configuration

#### 3.1 Pin Assignment

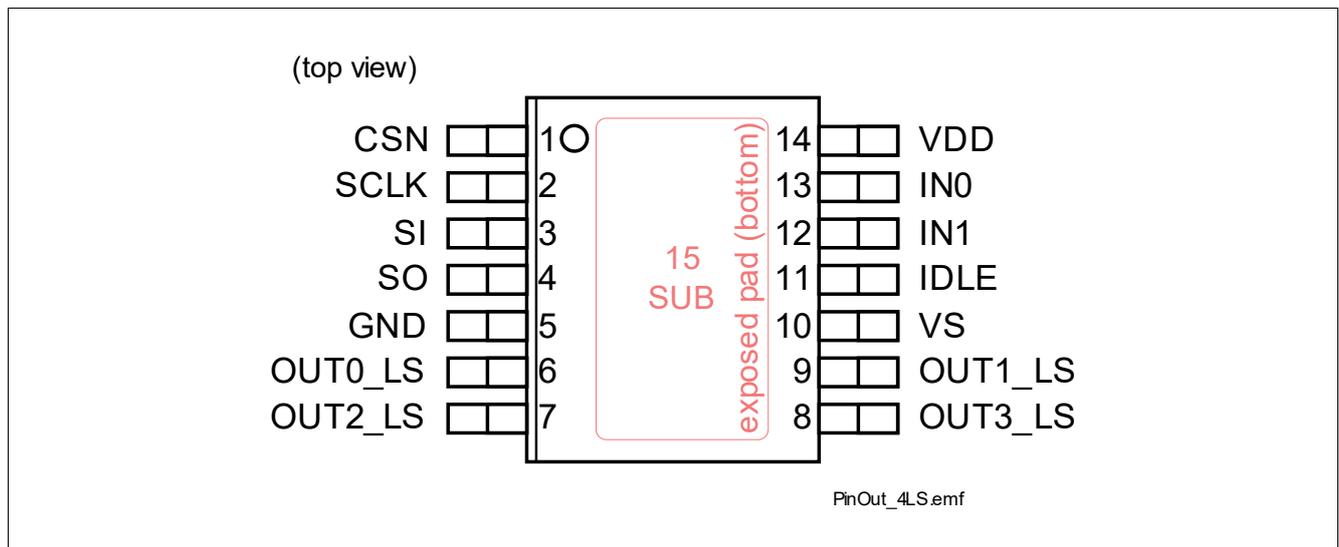


Figure 4 Pin Configuration TLE75004-EPD in PG-TSDSO-14

## Pin Configuration

### 3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
<b>Power Supply Pins</b>			
10	VS	–	<b>Analog supply <math>V_S</math></b> Positive supply voltage for power switches gate control (incl. protections)
14	VDD	–	<b>Digital supply <math>V_{DD}</math></b> Supply voltage for SPI with support function to $V_S$
5	GND	–	<b>Ground</b> Ground connection
<b>SPI Pins</b>			
1	CSN	I	<b>Chip Select</b> “low” active, integrated pull-up to $V_{DD}$
2	SCLK	I	<b>Serial Clock</b> “high” active, integrated pull-down to ground
3	SI	I	<b>Serial Input</b> “high” active, integrated pull-down to ground
4	SO	O	<b>Serial Output</b> “Z” (tri-state) when CSN is “high”
<b>Input and Stand-by Pins</b>			
11	IDLE	I	<b>Idle mode</b> power mode control, “high” active, integrated pull-down to ground
13	IN0	I	<b>Input pin 0</b> connected to channel 2 by default and in Limp Home mode, “high” active, integrated pull-down to ground
12	IN1	I	<b>Input pin 1</b> connected to channel 3 by default and Limp Home mode, “high” active, integrated pull-down to ground
<b>Power Output Pins</b>			
6	OUT0_LS	O	Drain of low-side power transistor (channel 0)
7	OUT2_LS	O	Drain of low-side power transistor (channel 2)
8	OUT3_LS	O	Drain of low-side power transistor (channel 3)
9	OUT1_LS	O	Drain of low-side power transistor (channel 1)
<b>Cooling Tab</b>			
15	GND	–	<b>Exposed pad</b> It is recommended to connect it to PCB ground for cooling and EMC - not usable as electrical GND pin. Electrical ground must be provided by pin 5.

General Product Characteristics

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 2 Absolute Maximum Ratings** <sup>1)</sup>

$T_J = -40\text{ °C to }+150\text{ °C}$

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Supply Voltages</b>							
Analog Supply voltage	$V_S$	-0.3	–	28	V	–	P_4.1.1
Digital Supply voltage	$V_{DD}$	-0.3	–	5.5	V	–	P_4.1.2
Supply voltage for load dump protection	$V_{S(LD)}$	–	–	42	V	<sup>2)</sup>	P_4.1.3
Supply voltage for short circuit protection (single pulse)	$V_{S(SC)}$	0	–	28	V	–	P_4.1.4
Reverse polarity voltage	$-V_{S(REV)}$	–	–	16	V	<sup>3)</sup> $T_{J(0)} = 25\text{ °C}$ $t \leq 2\text{ min}$ See <a href="#">Chapter 11</a> for general setup. $R_L = 70\ \Omega$ on all channels	P_4.1.5
Current through VS pin	$I_{VS}$	-10	–	10	mA	$t \leq 2\text{ min}$	P_4.1.7
Current through VDD pin	$I_{VDD}$	-50	–	10	mA	$t \leq 2\text{ min}$	P_4.1.8
<b>Power Stages</b>							
Load current	$ I_L $	–	–	$I_{L(OVLO)}$	A	single channel	P_4.1.9
Voltage at power transistor	$V_{DS}$	-0.3	–	42	V	–	P_4.1.10
Maximum energy dissipation single pulse	$E_{AS}$	–	–	50	mJ	<sup>4)</sup> $T_{J(0)} = 25\text{ °C}$ $I_{L(0)} = 2 \cdot I_{L(EAR)}$	P_4.1.13
Maximum energy dissipation single pulse	$E_{AS}$	–	–	25	mJ	<sup>4)</sup> $T_{J(0)} = 150\text{ °C}$ $I_{L(0)} = 400\text{ mA}$	P_4.1.14
Maximum energy dissipation repetitive pulses - $I_{L(EAR)}$	$E_{AR}$	–	–	10	mJ	<sup>4)</sup> $T_{J(0)} = 85\text{ °C}$ $I_{L(0)} = I_{L(EAR)}$ $2 \cdot 10^6\text{ cycles}$	P_4.1.16
<b>IDLE pin</b>							
Voltage at IDLE pin	$V_{IDLE}$	-0.3		5.5	V	–	P_4.1.23
Current through IDLE pin	$I_{IDLE}$	-0.75		0.75	mA	–	P_4.1.25

**General Product Characteristics**

**Table 2 Absolute Maximum Ratings (cont'd)<sup>1)</sup>**

$T_J = -40\text{ °C to }+150\text{ °C}$

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current through IDLE pin	$I_{IDLE}$	-10.0		2.0	mA	$t \leq 2\text{ min.}$	P_4.1.26

**Input Pins**

Voltage at input pins	$V_{IN}$	-0.3		5.5	V	–	P_4.1.28
Current through input pins	$I_{IN}$	-0.75		0.75	mA	–	P_4.1.30
Current through input pins	$I_{IN}$	-10.0		2.0	mA	$t \leq 2\text{ min.}$	P_4.1.31

**SPI Pins**

Voltage at chip select pin	$V_{CSN}$	-0.3		5.5	V	–	P_4.1.33
Current through chip select pin	$I_{CSN}$	-0.75		0.75	mA	–	P_4.1.34
Current through chip select pin	$I_{CSN}$	-10.0		2.0	mA	$t \leq 2\text{ min.}$	P_4.1.35
Voltage at serial clock pin	$V_{SCLK}$	-0.3		5.5	V		P_4.1.37
Current through serial clock pin	$I_{SCLK}$	-0.75		0.75	mA	–	P_4.1.38
Current through serial clock pin	$I_{SCLK}$	-10.0		2.0	mA	$t \leq 2\text{ min.}$	P_4.1.39
Voltage at serial input pin	$V_{SI}$	-0.3		5.5	V		P_4.1.41
Current through serial input pin	$I_{SI}$	-0.75		0.75	mA	–	P_4.1.42
Current through serial input pin	$I_{SI}$	-10.0		2.0	mA	$t \leq 2\text{ min.}$	P_4.1.43
Voltage at serial output pin SO	$V_{SO}$	-0.3		$V_{DD}+0.3$	V		P_4.1.58
Current through serial output pin SO	$I_{SO}$	-0.75		0.75	mA		P_4.1.45
Current through serial output pin SO	$I_{SO}$	-2.0		10.0	mA	$t \leq 2\text{ min.}$	P_4.1.46

**Temperatures**

Junction Temperature	$T_J$	-40	–	150	°C	–	P_4.1.48
Storage Temperature	$T_{stg}$	-55	–	150	°C	–	P_4.1.49

**ESD Susceptibility**

ESD Susceptibility HBM OUT pins vs. $V_S$ or GND	$V_{ESD}$	-4	–	4	kV	<sup>5)</sup> HBM	P_4.1.50
ESD Susceptibility HBM other pins	$V_{ESD}$	-2	–	2	kV	<sup>5)</sup> HBM	P_4.1.51
ESD Susceptibility CDM Pin 1, 7, 8, 14 (corner pins)	$V_{ESD}$	-750	–	750	V	<sup>6)</sup> CDM	P_4.1.53
ESD Susceptibility CDM	$V_{ESD}$	-500	–	500	V	<sup>6)</sup> CDM	P_4.1.54

1) Not subject to production test, specified by design.

2) For a duration of  $t_{on} = 400\text{ ms}$ ;  $t_{on}/t_{off} = 10\%$ ; limited to 100 pulses

3) Device is mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; the Product (Chip+Package) was simulated on a 76.2 \* 114.3 \* 1.5 mm board with 2 inner copper layers (2 \* 70  $\mu\text{m}$  Cu, 2 \* 35  $\mu\text{m}$  Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

**General Product Characteristics**

- 4) Pulse shape represents inductive switch off:  $I_L(t) = I_L(0) \times (1 - t / t_{\text{pulse}})$ ;  $0 < t < t_{\text{pulse}}$
- 5) ESD susceptibility, Human Body Model “HBM” according to AEC Q100-002
- 6) ESD susceptibility, Charged Device Mode “CDM” according to AECQ100-011 Rev D

**Notes**

- 1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- 2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**4.2 Functional Range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	7	–	18	V	–	P_4.2.1
Upper Supply Voltage Range for Extended Operation	$V_{S(EXT,UP)}$	18	–	28	V	Parameter deviation possible	P_4.2.2
Lower Supply Voltage Range for Extended Operation	$V_{S(EXT,LOW)}$	3	–	7	V	Parameter deviation possible	P_4.2.3
Junction Temperature	$T_J$	-40	–	150	°C	–	P_4.2.4
Logic supply voltage	$V_{DD}$	3	–	5.5	V	–	P_4.2.5

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*

**General Product Characteristics**

**4.3 Thermal Resistance**

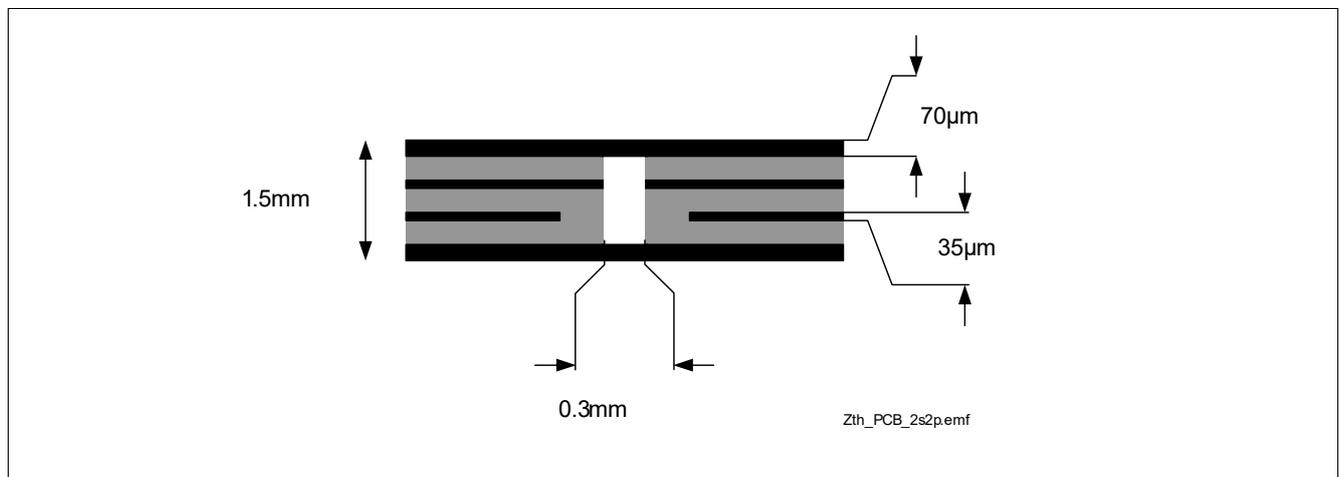
Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal Resistance**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	$R_{thJSP}$	–	5	7	K/W	1) measured to exposed pad (pin 15)	P_4.3.2
Junction to Ambient	$R_{thJA}$	–	40	–	K/W	2)	P_4.3.6

- 1) not subject to production test, specified by design
- 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 \* 114.3 \* 1.5 mm board with 2 inner copper layers (2 \* 70  $\mu$ m Cu, 2 \* 35  $\mu$ m Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

**4.3.1 PCB set up**



**Figure 5 2s2p PCB Cross Section**

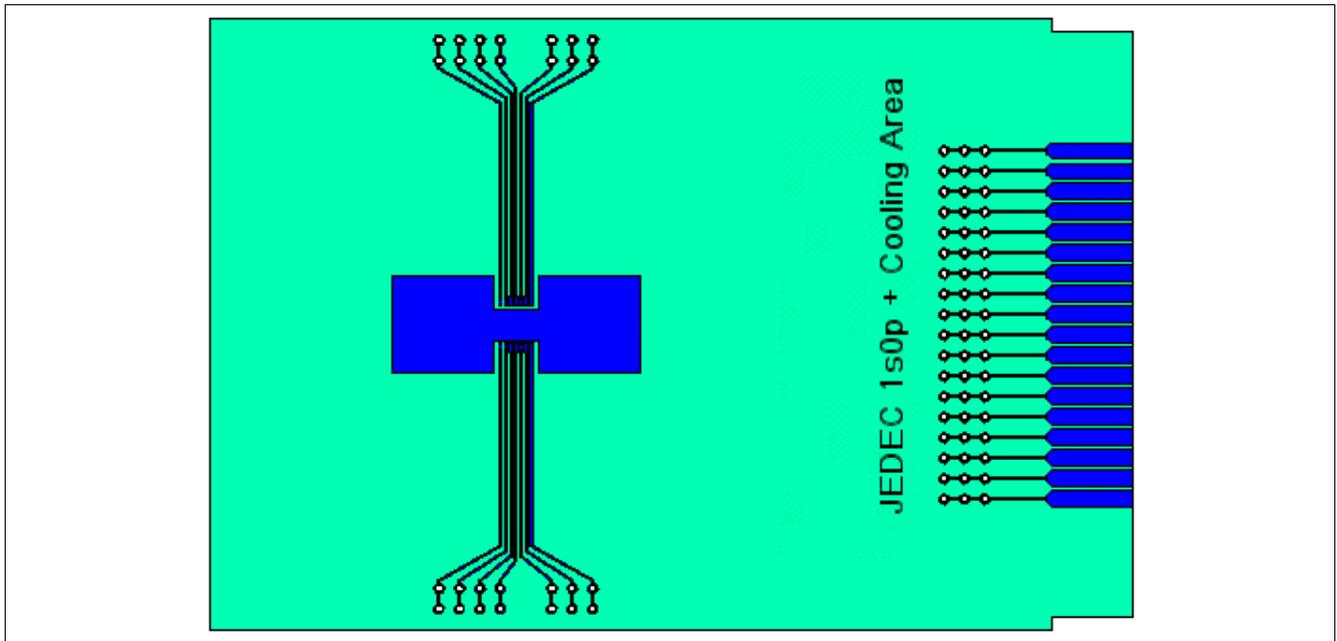


Figure 6 PC Board for Thermal Simulation with 600 mm<sup>2</sup> Cooling Area

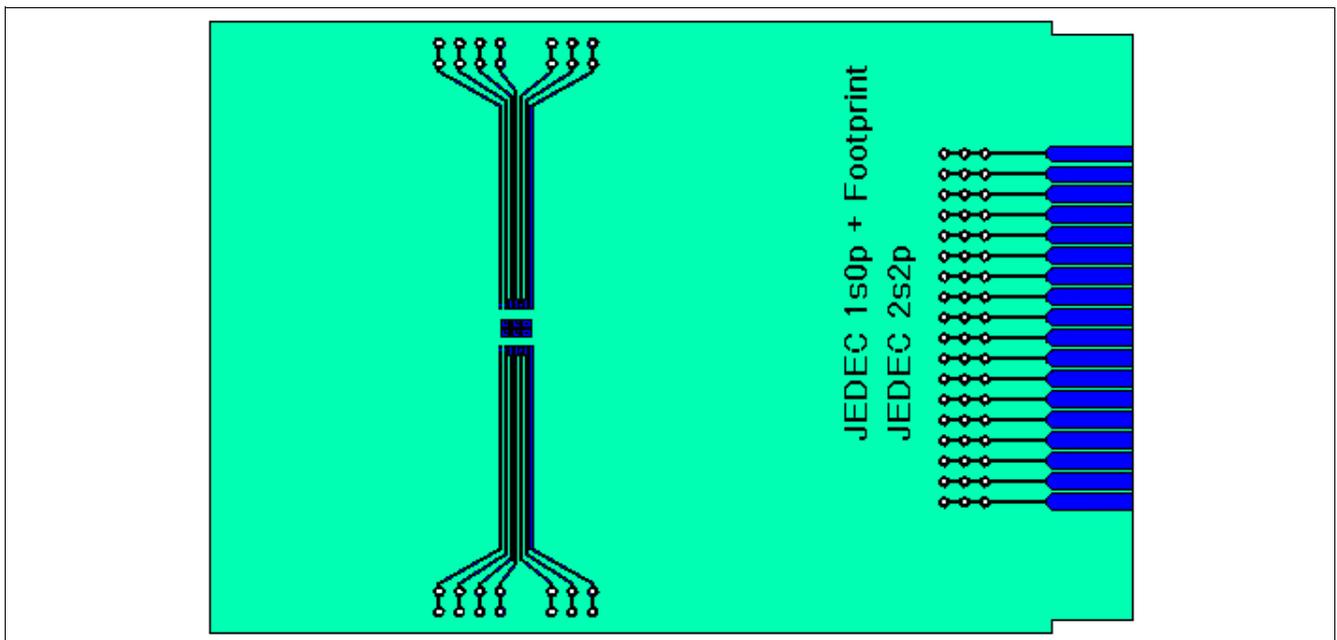


Figure 7 PC Board for Thermal Simulation with 2s2p Cooling Area

### 4.3.2 Thermal Impedance

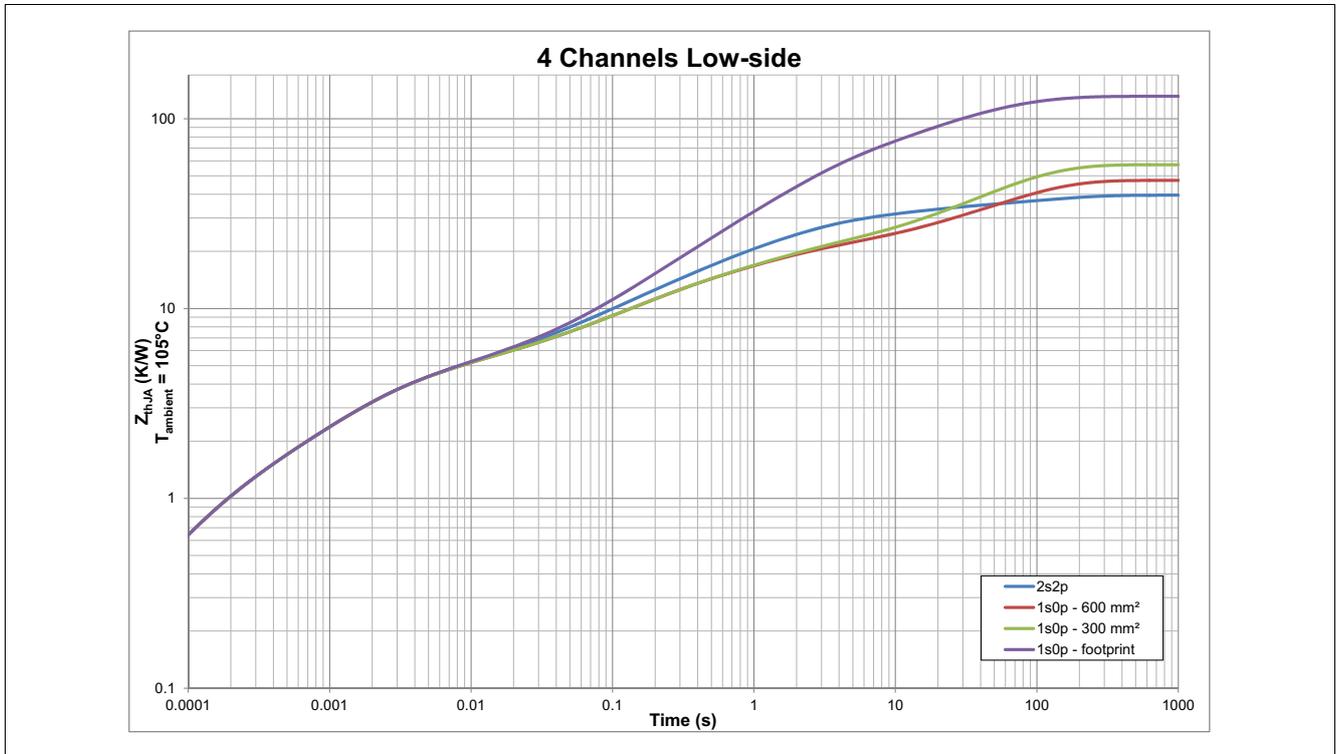


Figure 8 Typical Thermal Impedance. PCB setup according Chapter 4.3.1

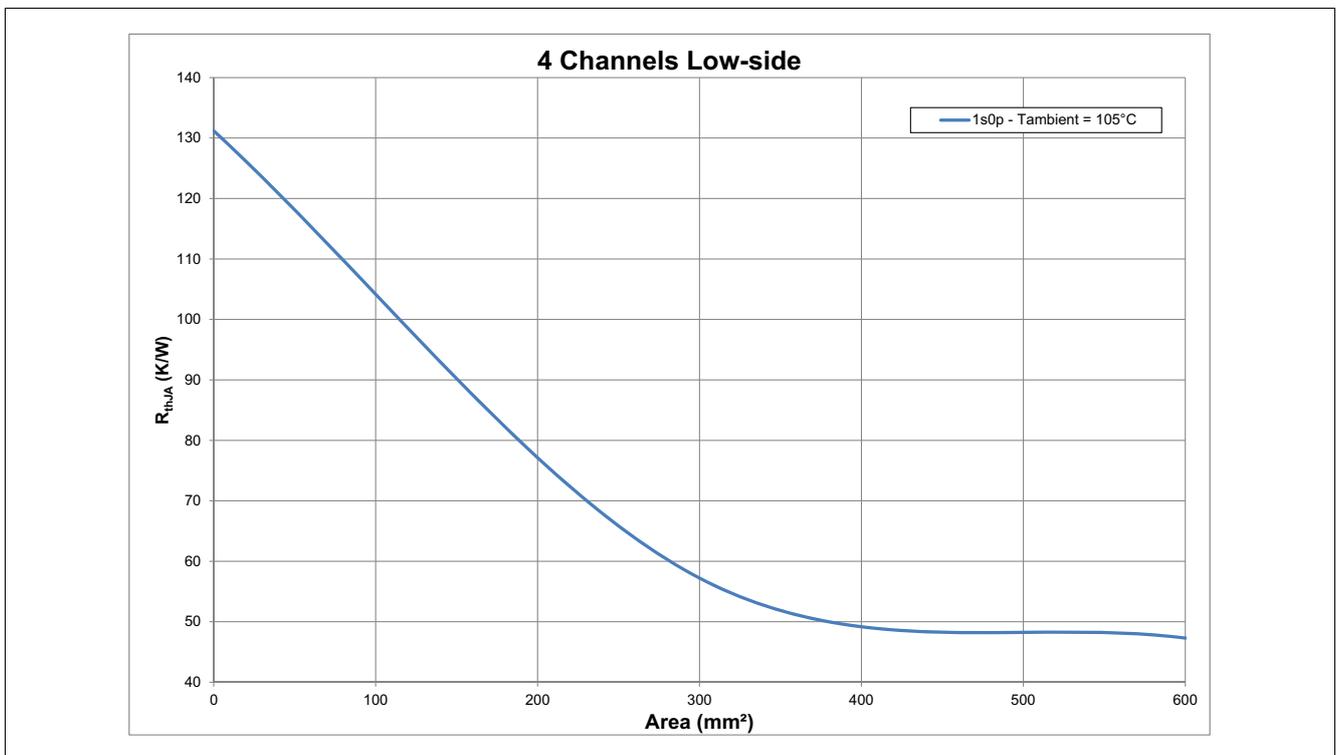


Figure 9 Typical Thermal Resistance. PCB setup 1s0p

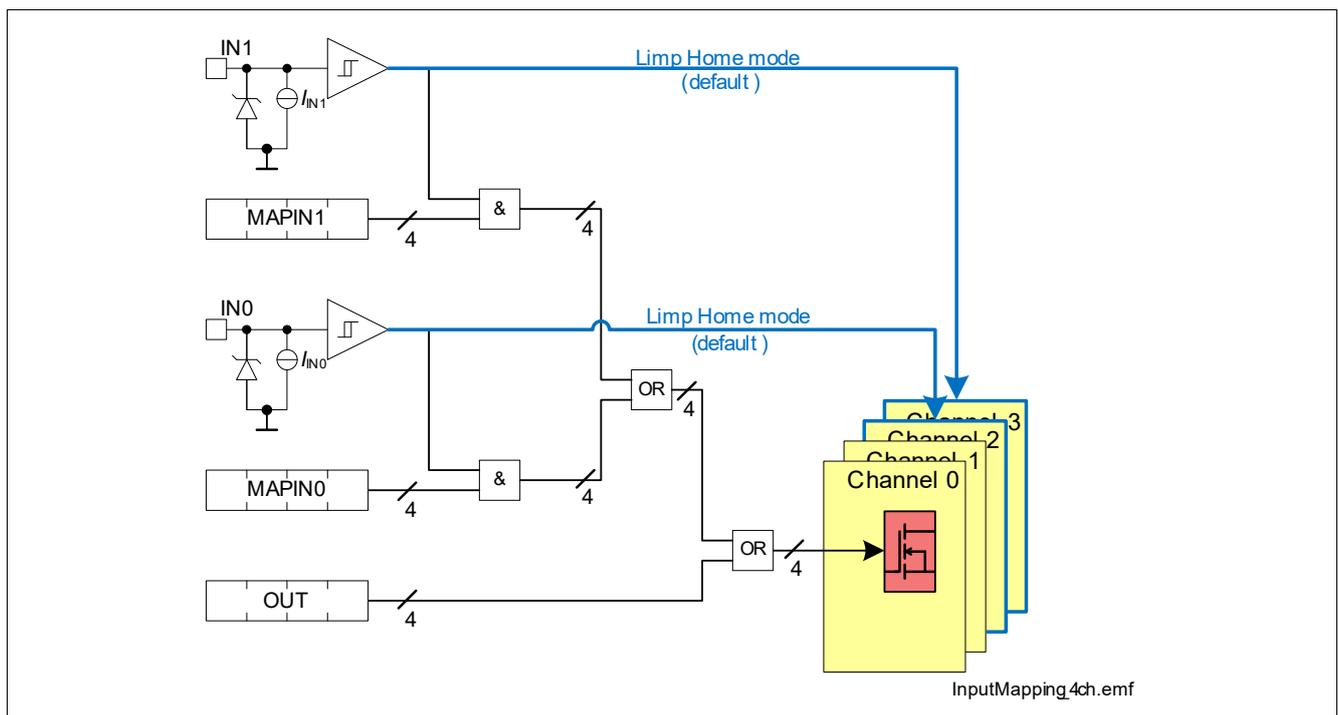
**Control Pins**

**5 Control Pins**

The device has three pins (IN0, IN1 and IDLE) to control directly the device without using SPI.

**5.1 Input pins**

TLE75004-EPD has two input pins available. Each input pin is connected by default to one channel (IN0 to channel 2, IN1 to channel 3). Input Mapping Registers **MAPIN0** and **MAPIN1** can be programmed to connect additional or different channels to each input pin, as shown in **Figure 10**. The signals driving the channels are an OR combination between **OUT** register status, IN0 and IN1 (according to Input Mapping registers status).



**Figure 10 Input Mapping**

The logic level of the input pins can be monitored via the Input Status Monitor Register (**INST**). The Input Status Monitor is operative also when TLE75004-EPD is in Limp Home mode. If one of the Input pins is set to “high” and the IDLE pin is set to “low”, the device switches into Limp Home mode and activates the channel mapped by default to the input pins. See **Chapter 6.1.5** for further details.

**5.2 IDLE pin**

The IDLE pin is used to bring the device into Sleep mode operation when is set to “low” and all input pins are set to “low”. When IDLE pin is set to “low” while one of the input pins is set to “high” the device enters Limp Home mode.

To ensure a proper mode transition, IDLE pin must be set for at least  $t_{IDLE2SLEEP}$  (P\_6.3.54, transition from “high” to “low”) or  $t_{SLEEP2IDLE}$  (P\_6.3.53, transition from “low” to “high”).

Setting the IDLE pin to “low” has the following consequences:

- All registers in the SPI are reset to default values
- $V_{DD}$  and  $V_S$  Undervoltage detection circuits are disabled to decrease current consumption (if both inputs are set to “low”)

### **Control Pins**

- No SPI communication is allowed (SO pin remains in high impedance state also when CSN pin is set to “low”) if both input pins are set to “low”

**Control Pins**

**5.3 Electrical Characteristics Control Pins**

**Table 5 Electrical Characteristics: Control Pins**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$  (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>IDLE pin</b>							
L-input level	$V_{IDLE(L)}$	0		0.8	V	–	P_5.3.1
H-input level	$V_{IDLE(H)}$	2.0		5.5	V	–	P_5.3.2
L-input current	$I_{IDLE(L)}$	5	12	20	$\mu\text{A}$	$V_{IDLE} = 0.8\text{ V}$	P_5.3.3
H-input current	$I_{IDLE(H)}$	14	28	45	$\mu\text{A}$	$V_{IDLE} = 2.0\text{ V}$	P_5.3.4
<b>Input Pins</b>							
L-input level	$V_{IN(L)}$	0		0.8	V	–	P_5.3.5
H-input level	$V_{IN(H)}$	2.0		5.5	V	–	P_5.3.6
L-input current	$I_{IN(L)}$	5	12	20	$\mu\text{A}$	$V_{IN} = 0.8\text{ V}$	P_5.3.7
H-input current	$I_{IN(H)}$	14	28	45	$\mu\text{A}$	$V_{IN} = 2.0\text{ V}$	P_5.3.8

**Power Supply**

## 6 Power Supply

The TLE75004-EPD is supplied by two supply voltages:

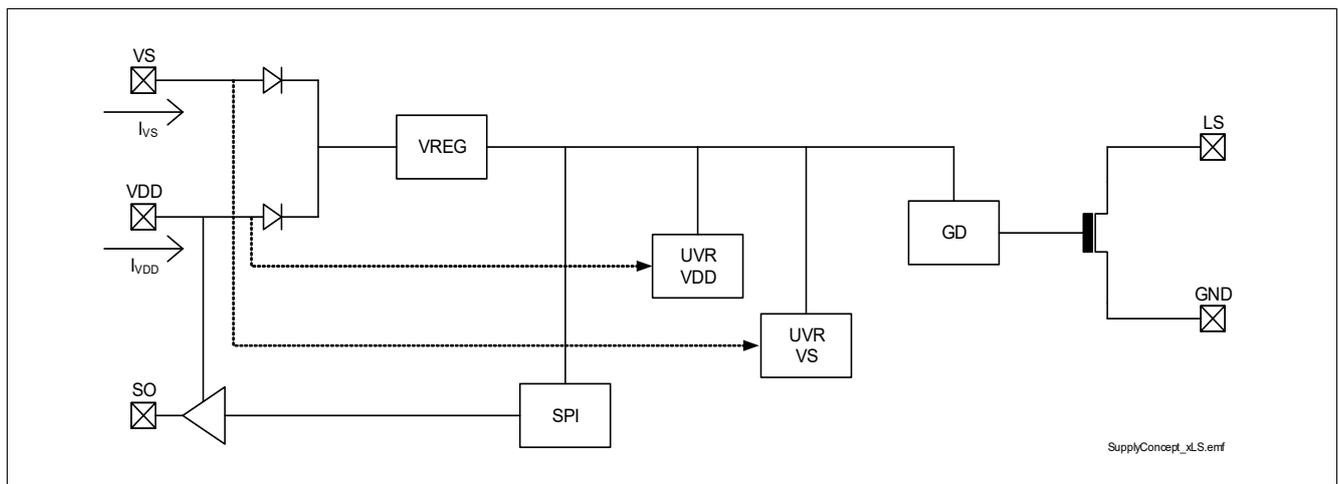
- $V_S$  (analog supply voltage used also for the logic)
- $V_{DD}$  (digital supply voltage)

The  $V_S$  supply line is connected to a battery feed and used, in combination with  $V_{DD}$  supply, for the driving circuitry of the power stages. In situations where  $V_S$  voltage drops below  $V_{DD}$  voltage (for instance during cranking events down to 3.0 V), an increased current consumption may be observed at VDD pin.

$V_S$  and  $V_{DD}$  supply voltages have an undervoltage detection circuit, which prevents the activation of the associated function in case the measured voltage is below the undervoltage threshold. More in detail:

- An undervoltage on both  $V_S$  and  $V_{DD}$  supply voltages prevents the activation of the power stages and any SPI communication (the SPI registers are reset)
- An undervoltage on  $V_{DD}$  supply prevents any SPI communication. SPI read/write registers are reset to default values.
- An undervoltage on  $V_S$  supply forces the TLE75004-EPD to drain all needed current for the low-side switches and for the logic from  $V_{DD}$  supply.

**Figure 11** shows a basic concept drawing of the interaction between supply pins VS and VDD, the output stage drivers and SO supply line.



**Figure 11 TLE75004-EPD Internal Power Supply concept**

When  $3.0\text{ V} \leq V_S \leq V_{DD} - V_{SDIFF}$  TLE75004-EPD operates in “Cranking Operative Range” (COR). In this condition the current consumption from VDD pin increases while it decreases from VS pin where the total current consumption remains within the specified limits. **Figure 12** shows the voltage levels at VS pin where the device goes in and out of COR. During the transition to and from COR operative region,  $I_{VS}$  and  $I_{VDD}$  change between values defined for normal operation and for COR operation. The sum of both current remains within limits specified in “Overall current consumption” section (see **Table 8**).

Power Supply

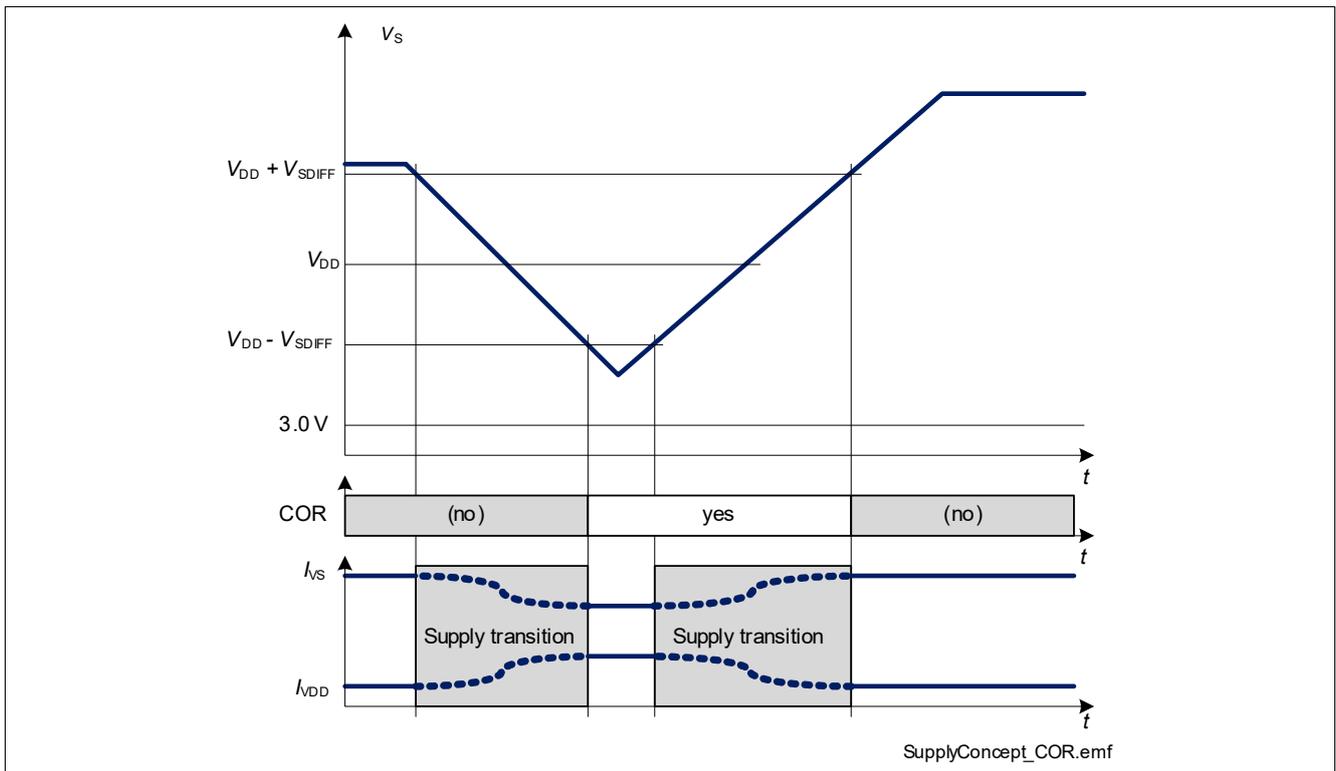


Figure 12 “Cranking Operative Range”

Furthermore, when  $V_{S(UV)} \leq V_S \leq V_{S(OP)}$  it may be not possible to switch ON a channel that was previously OFF. All channels that are already ON keep their state unless they are switched OFF via SPI or via INn pins. An overview of channel behavior according to different  $V_S$  and  $V_{DD}$  supply voltages is shown in [Table 6](#) (the table is valid after a successful power-up, see [Chapter 6.1.1](#) for more details).

**Power Supply**

**Table 6 Device capability as function of  $V_S$  and  $V_{DD}$**

	$V_{DD} \leq V_{DD(UV)}$ ( $V_{DD(UV)} = P\_6.3.25$ )	$V_{DD} = V_{DD(LOP)}$ ( $V_{DD(LOP)} = P\_6.3.24$ )	$V_{DD} > V_{DD(LOP)}$
$V_S \leq 3.0\text{ V}$  $3.0\text{ V} = V_{S(UV),max}$ ( $P\_6.3.1$ )	channels cannot be controlled	channels can be switched ON and OFF (SPI control) ( $R_{DS(ON)}$ deviations possible)	channels can be switched ON and OFF (SPI control) ( $R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available ( $f_{SCLK} = 0\text{ MHz}$ )	SPI communication possible ( $f_{SCLK} = 1\text{ MHz}$ ) ( $P\_10.4.34$ )	SPI communication possible ( $f_{SCLK} = 5\text{ MHz}$ ) ( $P\_10.4.22$ )
	Limp Home mode not available	Limp Home mode available ( $R_{DS(ON)}$ deviations possible)	Limp Home mode available ( $R_{DS(ON)}$ deviations possible)
$3.0\text{ V} < V_S \leq V_{S(OP)}$ ( $V_{S(OP)} = P\_6.3.2$ )	channels cannot be controlled by SPI	channels can be switched ON and OFF (SPI control) <sup>1)</sup> ( $R_{DS(ON)}$ deviations possible)	channels can be switched ON and OFF (SPI control) <sup>1)</sup> ( $R_{DS(ON)}$ deviations possible)
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available ( $f_{SCLK} = 0\text{ MHz}$ )	SPI communication possible ( $f_{SCLK} = 1\text{ MHz}$ ) ( $P\_10.4.34$ )	SPI communication possible ( $f_{SCLK} = 5\text{ MHz}$ ) ( $P\_10.4.22$ )
	Limp Home mode available <sup>1)</sup> ( $R_{DS(ON)}$ deviations possible)	Limp Home mode available <sup>1)</sup> ( $R_{DS(ON)}$ deviations possible)	Limp Home mode available ( $R_{DS(ON)}$ deviations possible)
$V_S > V_{S(OP)}$	channels cannot be controlled by SPI	channels can be switched ON and OFF (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$ )	channels can be switched ON and OFF (small $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$ )
	SPI registers reset	SPI registers available	SPI registers available
	SPI communication not available ( $f_{SCLK} = 0\text{ MHz}$ )	SPI communication possible ( $f_{SCLK} = 5\text{ MHz}$ ) ( $P\_10.4.22$ )	SPI communication possible ( $f_{SCLK} = 5\text{ MHz}$ ) ( $P\_10.4.22$ )
	Limp Home mode available ( $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$ )	Limp Home mode available ( $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$ )	Limp Home mode available ( $R_{DS(ON)}$ dev. possible when $V_S = V_{S(EXT,LOW)}$ )

1) undervoltage condition on  $V_S$  must be considered - see [Chapter 6.2.1](#) for more details

Power Supply

6.1 Operation Modes

TLE75004-EPD has the following operation modes:

- Sleep mode
- Idle mode
- Active mode
- Limp Home mode

The transition between operation modes is determined according to following levels and states:

- logic level at IDLE pin
- logic level at INn pins
- **OUT.OUTn** bits state
- **HWCR.ACT** bit state

The state diagram including the possible transitions is shown in **Figure 13**. The behaviour of TLE75004-EPD as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors  $V_S$  and  $V_{DD}$  supply voltages, some changes within the same operation mode can be seen accordingly.

The operation mode of the TLE75004-EPD can be observed by:

- status of output channels
- status of SPI registers
- current consumption at VDD pin ( $I_{VDD}$ )
- current consumption at VS pin ( $I_{VS}$ )

The default operation mode to switch ON the loads is Active mode. If the device is not in Active mode and a request to switch ON one or more outputs comes (via SPI or via Input pins), it will switch into Active or Limp Home mode, according to IDLE pin status. Due to the time needed for such transitions, output turn-on time  $t_{ON}$  will be extended due to the mode transition latency.

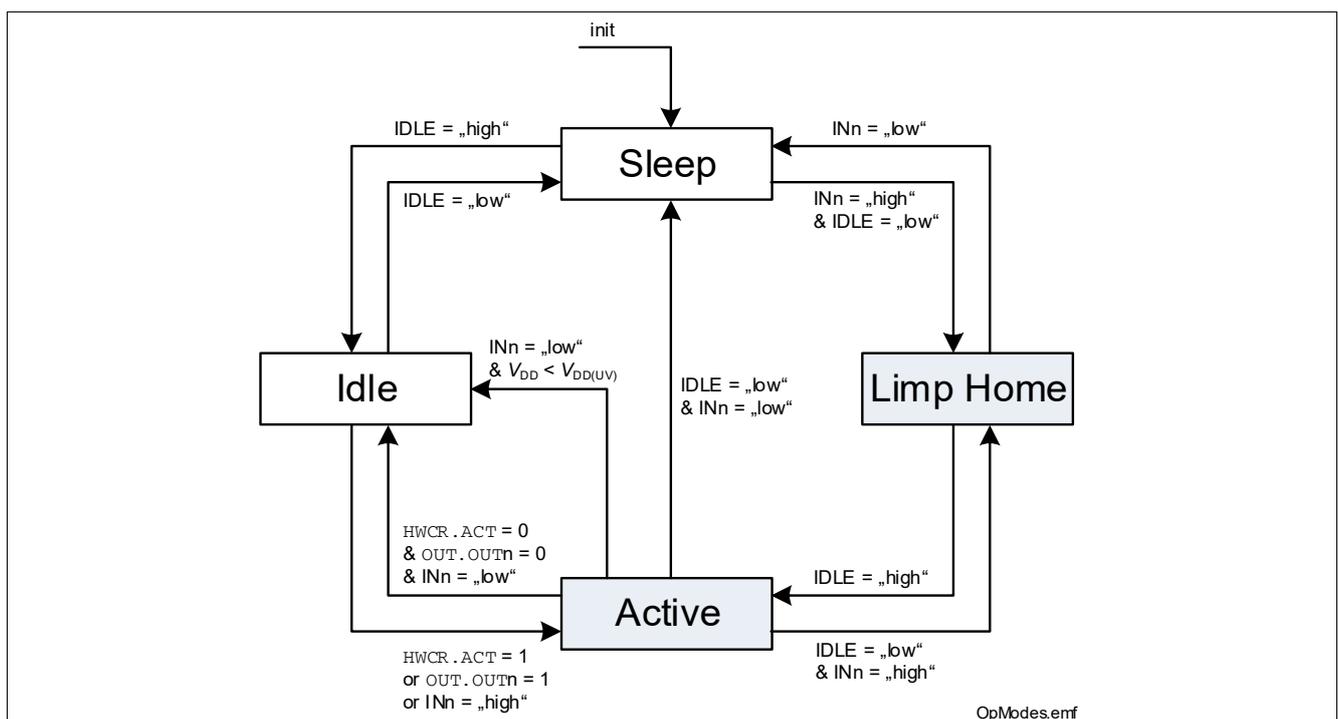


Figure 13 Operation Mode state diagram

**Power Supply**

**Table 7** shows the correlation between device operation modes,  $V_S$  and  $V_{DD}$  supply voltages, and state of the most important functions (channels operativity, SPI communication and SPI registers).

**Table 7 Device function in relation to operation modes,  $V_S$  and  $V_{DD}$  voltages**

Operation Mode	Function	Undervoltage condition on $V_S$ <sup>1)</sup> $V_{DD} \leq V_{DD(UV)}$	Undervoltage condition on $V_S$ $V_{DD} > V_{DD(UV)}$	$V_S$ not in undervoltage $V_{DD} \leq V_{DD(UV)}$	$V_S$ not in undervoltage $V_{DD} > V_{DD(UV)}$
Sleep	Channels	not available	not available	not available	not available
	SPI comm.	not available	not available	not available	not available
	SPI registers	reset	reset	reset	reset
Idle	Channels	not available	not available	not available	not available
	SPI comm.	not available	✓	not available	✓
	SPI registers	reset	✓	reset	✓
Active	Channels	not available	✓	✓ (IN pins only)	✓
	SPI comm.	not available	✓	not available	✓
	SPI registers	reset	✓	reset	✓
Limp Home	Channels	not available	✓ (IN pins only)	✓ (IN pins only)	✓ (IN pins only)
	SPI comm.	not available	✓ (read-only)	not available	✓ (read-only)
	SPI registers	reset	✓ (read-only) <sup>2)</sup>	reset	✓ (read-only) <sup>2)</sup>

1) see [Chapter 6.2.1](#) for more details

2) see [Chapter 6.1.5](#) for a detailed overview

### 6.1.1 Power-up

The Power-up condition is satisfied when one of the supply voltages ( $V_S$  or  $V_{DD}$ ) is applied to the device and the INn or IDLE pins are set to “high”. If  $V_S$  is above the threshold  $V_{S(OP)}$  or if  $V_{DD}$  is above the threshold  $V_{DD(LOP)}$  the internal power-on signal is set.

### 6.1.2 Sleep mode

When TLE75004-EPD is in Sleep mode, all outputs are OFF and the SPI registers are reset, independently from the supply voltages. The current consumption is minimum. See parameters  $I_{VDD(SLEEP)}$  and  $I_{VS(SLEEP)}$ , or parameter  $I_{SLEEP}$  for the whole device.

### 6.1.3 Idle mode

In Idle mode, the current consumption of the device can reach the limits given by parameters  $I_{VDD(IDLE)}$  and  $I_{VS(IDLE)}$ , or by parameter  $I_{IDLE}$  for the whole device. The internal voltage regulator is working. Diagnosis functions are not available. The output channels are switched OFF, independently from the supply voltages. When  $V_{DD}$  is available, the SPI registers are working and SPI communication is possible. In Idle mode the **ERRn** bits are not cleared for functional safety reasons.

## Power Supply

### 6.1.4 Active mode

Active mode is the normal operation mode of TLE75004-EPD when no Limp Home condition is set and it is necessary to drive some or all loads. Voltage levels of  $V_{DD}$  and  $V_S$  influence the behavior as described at the beginning of [Chapter 6](#). Device current consumption is specified with  $I_{VDD(ACTIVE)}$  and  $I_{VS(ACTIVE)}$  ( $I_{ACTIVE}$  for the whole device). The device enters Active mode when IDLE pin is set to “high” and one of the input pins is set to “high” or one **OUT.OUTn** bit is set to “1”. If **HWCR.ACT** is set to “0”, the device returns to Idle mode as soon as all input pins are set to “low” and **OUT.OUTn** bits are set to “0”. If **HWCR.ACT** is set to “1”, the device remains in Active mode independently of the status of input pins and **OUT.OUTn** bits. An undervoltage condition on  $V_{DD}$  supply brings the device into Idle mode, if all input pins are set to “low”. Even if the registers **MAPINO** and **MAPIN1** are both set to “00<sub>H</sub>” but one of the input pins INN is set to “high”, the device goes into Active mode.

### 6.1.5 Limp Home mode

TLE75004-EPD enters Limp Home mode when IDLE pin is “low” and one of the input pins is set to “high”, switching ON the channel connected to it. SPI communication is possible but only in read-only mode (SPI registers can be read but cannot be written). More in detail:

- **UVRVS** and **LOPVDD** are set to “1”
- **MODE** bits are set to “01<sub>B</sub>” (Limp Home mode)
- **TER** bit is set to “1” on the first SPI command after entering Limp Home mode. Afterwards it works normally
- **OLOFF** bits is set to “0”
- **ERRn** bits work normally
- **DIAG\_OSM.OUTn** bits can be read and work normally
- All other registers are set to their default value and cannot be programmed as long as the device is in Limp Home mode

See [Table 6](#) for a detailed overview of supply voltage conditions required to switch ON channels 2 and 3 during Limp Home. All other channels are OFF.

A transmission of SPI commands during transition from Active to Limp Home mode or Limp Home to Active mode may result in undefined SPI responses.

### 6.1.6 Definition of Power Supply modes transition times

The channel turn-ON time is as defined by parameter  $t_{ON}$  when TLE75004-EPD is in Active mode or in Limp Home mode. In all other cases, it is necessary to add the transition time required to reach one of the two aforementioned Power Supply modes (as shown in [Figure 14](#)).

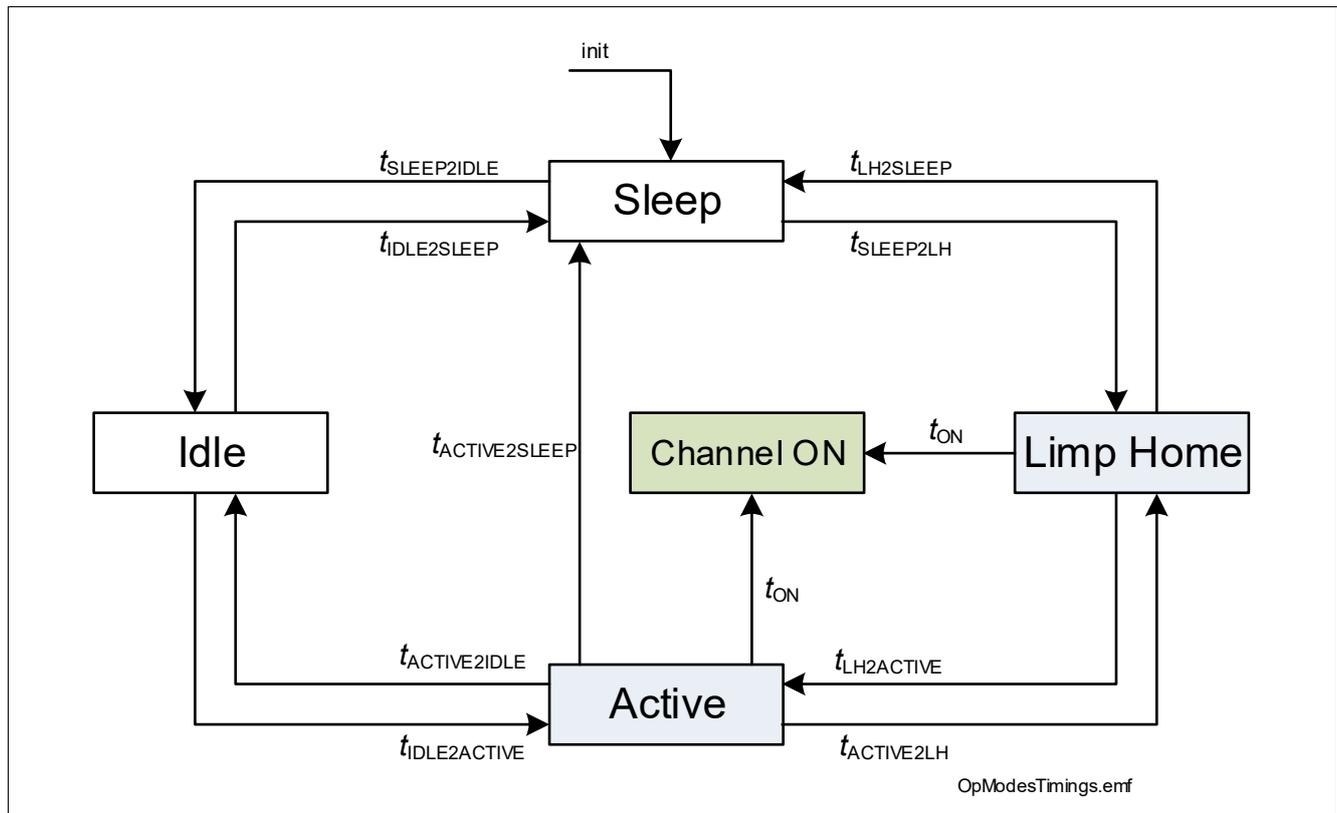


Figure 14 Transition Time diagram

## 6.2 Reset condition

One of the following 3 conditions resets the SPI registers to the default value:

- $V_{DD}$  is not present or below the undervoltage threshold  $V_{DD(UV)}$
- IDLE pin is set to “low”
- a reset command (**HWCR.RST** set to “1”) is executed
  - **ERRn** bits are not cleared by a reset command (for functional safety)
  - **UVRVS** and **LOPVDD** bits are cleared by a reset command

In particular, all channels are switched OFF (if there are no input pin set to “high”) and the Input Mapping configuration is reset.

### 6.2.1 Undervoltage on $V_S$

Between  $V_{S(UV)}$  and  $V_{S(OP)}$  the undervoltage mechanism is triggered. If the device is operative and the supply voltage drops below the undervoltage threshold  $V_{S(UV)}$ , the logic set the bit **UVRVS** to “1”. As soon as the supply voltage  $V_S$  is above the minimum voltage operative threshold  $V_{S(OP)}$ , the bit **UVRVS** is set to “0” after the first Standard Diagnosis readout. Undervoltage condition on  $V_S$  influences the status of the channels, as described in **Table 6**. **Figure 15** sketches the undervoltage behavior.

Power Supply

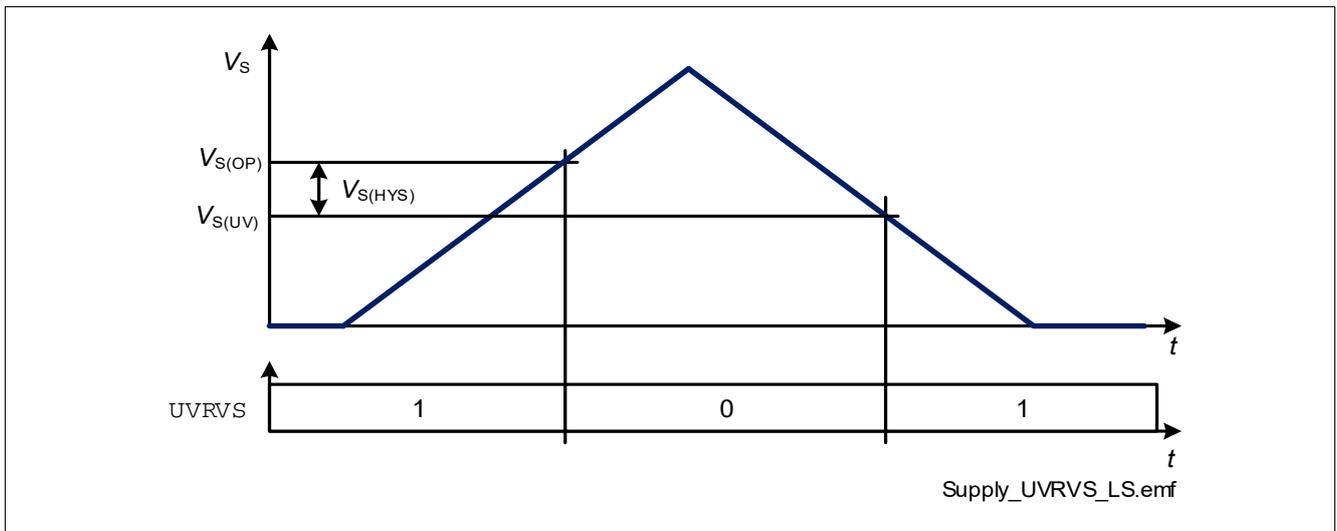


Figure 15  $V_S$  Undervoltage Behavior

### 6.2.2 Low Operating Power on $V_{DD}$

When  $V_{DD}$  supply voltage is in the range indicated by  $V_{DD(LOP)}$ , the bit **LOPVDD** is set to "1". As soon as  $V_{DD} > V_{DD(LOP)}$  the bit **LOPVDD** is set to "0" after the first Standard Diagnosis readout.

If  $V_{DD}$  supply voltage is not present, a voltage applied to pins CSN or SO can supply the internal logic (not recommended in normal operation due to internal design limitations).

Power Supply

6.3 Electrical Characteristics Power Supply

**Table 8 Electrical Characteristics Power Supply**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>VS pin</b>							
Analog supply undervoltage shutdown	$V_{S(UV)}$	1.5	–	3.0	V	OUTn = ON from $V_{DS} \leq 1\text{ V}$ to <b>UVRVS</b> = 1 <sub>B</sub> $R_L = 50\ \Omega$	P_6.3.1
Analog supply minimum operative voltage	$V_{S(OP)}$	–	–	4.0	V	<b>OUT.OUTn</b> = 1 <sub>B</sub> from <b>UVRVS</b> = 1 <sub>B</sub> to $V_{DS} \leq 1\text{ V}$ $R_L = 50\ \Omega$	P_6.3.2
Undervoltage shutdown hysteresis	$V_{S(HYS)}$	–	1	–	V	<sup>1)</sup>	P_6.3.3
Analog supply current consumption in Sleep mode with loads	$I_{VS(SLEEP)}$	–	0.1	3	$\mu\text{A}$	<sup>1)</sup> $V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J \leq 85\text{ °C}$	P_6.3.4
Analog supply current consumption in Sleep mode with loads	$I_{VS(SLEEP)}$	–	0.1	–	$\mu\text{A}$	<sup>1)</sup> $V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J \leq 85\text{ °C}$ $V_S = 13.5\text{ V}$	P_6.3.63
Analog supply current consumption in Sleep mode with loads	$I_{VS(SLEEP)}$	–	0.1	20	$\mu\text{A}$	$V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J = 150\text{ °C}$	P_6.3.5
Analog supply current consumption in Idle mode with loads	$I_{VS(IDLE)}$	–	–	2.2	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 0 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.6

**Power Supply**

**Table 8 Electrical Characteristics Power Supply (cont'd)**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog supply current consumption in Idle mode with loads (COR)	$I_{VS(IDLE)}$	–	–	0.3	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 0 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$ $V_S \leq V_{DD} - 1\text{ V}$	P_6.3.7
Analog supply current consumption in Active mode with loads - channels OFF	$I_{VS(ACTIVE)}$	–	–	3.2	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.11
Analog supply current consumption in Active mode with loads - channels OFF (COR)	$I_{VS(ACTIVE)}$	–	0.1	0.3	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$ $V_S \leq V_{DD} - 1\text{ V}$	P_6.3.12
Analog supply current consumption in Active mode with loads - channels ON	$I_{VS(ACTIVE)}$	–	–	3.2	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 1 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.19

**Power Supply**

**Table 8 Electrical Characteristics Power Supply (cont'd)**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Analog supply current consumption in Active mode with loads - channels ON (COR)	$I_{VS(ACTIVE)}$	–	0.1	0.3	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 1 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$ $V_S \leq V_{DD} - 1\text{ V}$	P_6.3.20
<b>VDD pin</b>							
Logic Supply Operating voltage	$V_{DD(OP)}$	3.0	–	5.5	V	$f_{SCLK} = 5\text{ MHz}$	P_6.3.23
Logic Supply Lower Operating Voltage	$V_{DD(LOP)}$	3.0	–	4.5	V	–	P_6.3.24
Undervoltage shutdown	$V_{DD(UV)}$	1	–	3.0	V	$V_{SI} = 0\text{ V}$ $V_{SCLK} = 0\text{ V}$ $V_{CSN} = 0\text{ V}$ SO from “low” to high impedance	P_6.3.25
Logic supply current in Sleep mode	$I_{VDD(SLEEP)}$	–	0.1	2.5	μA	<sup>1)</sup> $V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J \leq 85\text{ °C}$	P_6.3.26
Logic supply current in Sleep mode	$I_{VDD(SLEEP)}$	–	–	10	μA	$V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J = 150\text{ °C}$	P_6.3.27
Logic supply current in Idle mode	$I_{VDD(IDLE)}$	–	–	0.3	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 0 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.28
Logic supply current in Idle mode (COR)	$I_{VDD(IDLE)}$	–	–	2.2	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 0 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$ $V_S \leq V_{DD} - 1\text{ V}$	P_6.3.29

Power Supply

**Table 8 Electrical Characteristics Power Supply** (cont'd)

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Logic supply current in Active mode - channels OFF	$I_{VDD(ACTIVE)}$	–	–	0.3	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.30
Logic supply current in Active mode - channels OFF (COR)	$I_{VDD(ACTIVE)}$	–	–	3.2	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$ $V_S \leq V_{DD} - 1\text{ V}$	P_6.3.34
Logic supply current in Active mode - channels ON	$I_{VDD(ACTIVE)}$	–	–	0.3	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 1 $V_{CSN} = V_{DD}$	P_6.3.35
Logic supply current in Active mode - channels ON (COR)	$I_{VDD(ACTIVE)}$	–	–	3.2	mA	IDLE = “high” $V_{INn}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 1 <sub>B</sub> $V_{CSN} = V_{DD}$ $V_S = V_{DD} - 1\text{ V}$	P_6.3.38

**Overall current consumption**

Overall current consumption in Sleep mode $I_{VS(SLEEP)} + I_{VDD(SLEEP)}$	$I_{SLEEP}$	–	–	5	μA	<sup>1)</sup> $V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J \leq 85\text{ °C}$	P_6.3.40
Overall current consumption in Sleep mode $I_{VS(SLEEP)} + I_{VDD(SLEEP)}$	$I_{SLEEP}$	–	–	5	μA	<sup>1)</sup> $V_{IDLE}$ floating $V_{INn}$ floating $V_{CSN} = V_{DD}$ $T_J \leq 85\text{ °C}$ $V_S = 13.5\text{ V}$	P_6.3.64

**Power Supply**

**Table 8 Electrical Characteristics Power Supply (cont'd)**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in [Figure 3](#) (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overall current consumption in Sleep mode $I_{VS(SLEEP)} + I_{VDD(SLEEP)}$	$I_{SLEEP}$	–	–	30	μA	$V_{IDLE}$ floating $V_{INN}$ floating $V_{CSN} = V_{DD}$ $T_J = 150\text{ °C}$	P_6.3.41
Overall current consumption in Idle mode $I_{VS(IDLE)} + I_{VDD(IDLE)}$	$I_{IDLE}$	–	–	2.5	mA	IDLE = “high” $V_{INN}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 0 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.42
Overall current consumption in Active mode - channels OFF $I_{VS(ACTIVE)} + I_{VDD(ACTIVE)}$	$I_{ACTIVE}$	–	–	3.5	mA	IDLE = “high” $V_{INN}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 0 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.46
Overall current consumption in Active mode - channels ON $I_{VS(ACTIVE)} + I_{VDD(ACTIVE)}$	$I_{ACTIVE}$	–	–	3.5	mA	IDLE = “high” $V_{INN}$ floating $f_{SCLK} = 0\text{ MHz}$ <b>HWCR.ACT</b> = 1 <sub>B</sub> <b>OUT.OUTn</b> = 1 <sub>B</sub> <b>DIAG_IOL.OUTn</b> = 0 <sub>B</sub> $V_{CSN} = V_{DD}$	P_6.3.51
Voltage difference between $V_S$ and $V_{DD}$ supply lines	$V_{SDIFF}$	–	200	–	mV	<sup>1)</sup>	P_6.3.52

**Timings**

Sleep to Idle delay	$t_{SLEEP2IDLE}$	–	200	400	μs	<sup>1)</sup> from IDLE pin to <b>TER + INST</b> register = 8680 <sub>H</sub> (see <a href="#">Chapter 10.6.1</a> for details)	P_6.3.53
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Power Supply

**Table 8 Electrical Characteristics Power Supply** (cont'd)

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in [Figure 3](#) (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Idle to Sleep delay	$t_{IDLE2SLEEP}$	–	100	200	$\mu\text{s}$	<sup>1)</sup> from IDLE pin to Standard Diagnosis = 0000 <sub>H</sub> (see <a href="#">Chapter 10.5</a> for details) external pull-down SO to GND required	P_6.3.54
Idle to Active delay	$t_{IDLE2ACTIVE}$	–	100	200	$\mu\text{s}$	<sup>1)</sup> from INn or CSN pins to <b>MODE</b> = 10 <sub>B</sub>	P_6.3.55
Active to Idle delay	$t_{ACTIVE2IDLE}$	–	100	200	$\mu\text{s}$	<sup>1)</sup> from INn or CSN pins to <b>MODE</b> = 11 <sub>B</sub>	P_6.3.56
Sleep to Limp Home delay	$t_{SLEEP2LH}$	–	300 + $t_{ON}$	600 + $t_{ON}$	$\mu\text{s}$	<sup>1)</sup> from INn pins to $V_{DS} = 10\% V_S$	P_6.3.57
Limp Home to Sleep delay	$t_{LH2SLEEP}$	–	200 + $t_{OFF}$	400 + $t_{OFF}$	$\mu\text{s}$	<sup>1)</sup> from INn pins to Standard Diagnosis = 0000 <sub>H</sub> (see <a href="#">Chapter 10.6.1</a> for details). External pull-down SO to GND required	P_6.3.58
Limp Home to Active delay	$t_{LH2ACTIVE}$	–	50	100	$\mu\text{s}$	<sup>1)</sup> from IDLE pin to <b>MODE</b> = 10 <sub>B</sub>	P_6.3.59

**Power Supply**

**Table 8 Electrical Characteristics Power Supply (cont'd)**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$ , all voltages with respect to ground, positive currents flowing as described in **Figure 3** (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Active to Limp Home delay	$t_{ACTIVE2LH}$	–	50	100	$\mu\text{s}$	<sup>1)</sup> from IDLE pin to <b>TER + INST</b> register = 8683 <sub>H</sub> (IN0 = IN1 = “high”) or 8682 <sub>H</sub> (IN1 = “high”, IN0 = “low”) or 8681 <sub>H</sub> (IN1 = “low”, IN0 = “high”) (see <b>Chapter 10.5</b> for details)	P_6.3.60
Active to Sleep delay	$t_{ACTIVE2SLEEP}$	–	50	100	$\mu\text{s}$	<sup>1)</sup> from IDLE pin to Standard Diagnosis = 0000 <sub>H</sub> (see <b>Chapter 10.6.1</b> for details). External pull-down SO to GND required.	P_6.3.61

1) Not subject to production test - specified by design

**Power Stages**

## 7 Power Stages

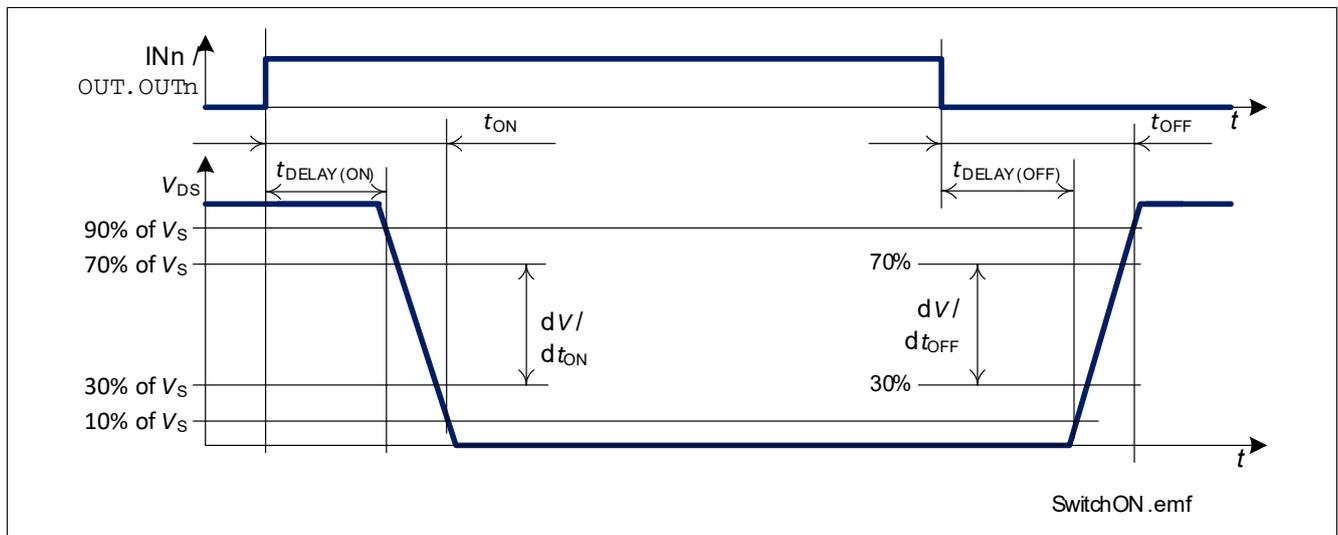
The TLE75004-EPD is an four channels low-side relay switch. The power stages are built by N-channel lateral power MOSFET transistors.

### 7.1 Output ON-state resistance

The ON-state resistance  $R_{DS(ON)}$  depends on the supply voltage as well as the junction temperature  $T_J$ .

#### 7.1.1 Switching Resistive Loads

When switching resistive loads the following switching times and slew rates can be considered.



**Figure 16 Switching a Resistive Load**

#### 7.1.2 Inductive Output Clamp

When switching off inductive loads, the voltage across the power switch rises to  $V_{DS(CL)}$  potential, because the inductance intends to continue driving the current. The voltage clamping is necessary to prevent device destruction.

**Figure 17** shows a concept drawing of the implementation. Nevertheless, the maximum allowed load inductance is limited. The clamping structure protects the device in all operative modes (Sleep, Idle, Active, Limp Home).

Power Stages

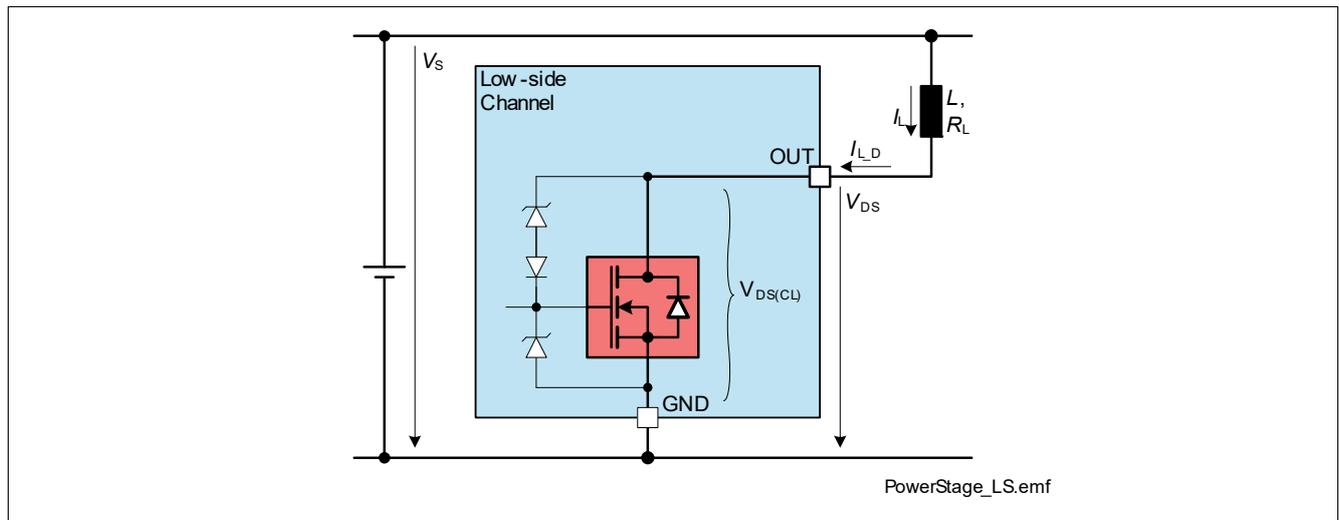


Figure 17 Output Clamp concept

### 7.1.3 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the TLE75004-EPD. Equation (7.1) shows how to calculate the energy for low-side switches:

$$E = V_{DS(CL)} \cdot \left[ \frac{V_S - V_{DS(CL)}}{R_L} \cdot \ln \left( 1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CL)}} \right) + I_L \right] \cdot \frac{L}{R_L} \quad (7.1)$$

The maximum energy, which is converted into heat, is limited by the thermal design of the component. The  $E_{AR}$  value provided in Table 2 assumes that all channels can dissipate the same energy when the inductances connected to the outputs are demagnetized at the same time.

## 7.2 Switching Channels in parallel

In case of appearance of a short circuit with channels in parallel, it may happen that the two channels switch OFF asynchronously, therefore bringing an additional thermal stress to the channel that switches OFF last. In order to avoid this condition, it is possible to parametrize in the SPI registers the parallel operation of two neighbour channels (bits **HWCR.PAR**). When operating in this mode, the fastest channel to react to an Over Load or Over Temperature condition will deactivate also the other. The inductive energy that two channels can handle once set in parallel is lower than twice the single channel energy (see P\_7.6.11). It is possible to synchronize the following couples of channels:

- channel 0 and channel 2 → **HWCR.PAR** (0) set to “1”
- channel 1 and channel 3 → **HWCR.PAR** (1) set to “1”

The synchronization bits influence only how the channels react to Over Load or Over Temperature conditions. Synchronized channels have to be switched ON and OFF individually by the micro-controller.

Power Stages

7.3 Electrical Characteristics Power Stages

**Table 9 Electrical Characteristics: Power Stage**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$  (unless otherwise specified)  
Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Output Characteristics</b>							
On-State Resistance	$R_{DS(ON)}$	–	1.0	–	$\Omega$	<sup>1)</sup> $T_J = 25\text{ °C}$	P_7.6.1
On-State Resistance	$R_{DS(ON)}$	–	1.8	2.2	$\Omega$	$T_J = 150\text{ °C}$ $I_L = I_{L(EAR)} = 220\text{ mA}$	P_7.6.2
Nominal load current (all channels active)	$I_{L(NOM)}$	–	470	500 <sup>2)3)</sup>	mA	<sup>1)</sup> $T_A = 85\text{ °C}$ $T_J \leq 150\text{ °C}$	P_7.6.6
Nominal load current (all channels active)	$I_{L(NOM)}$	–	370	500 <sup>2)3)</sup>	mA	<sup>1)</sup> $T_A = 105\text{ °C}$ $T_J \leq 150\text{ °C}$	P_7.6.7
Load current for maximum energy dissipation - repetitive (all channels active)	$I_{L(EAR)}$	–	220	–	mA	<sup>1)</sup> $T_A = 85\text{ °C}$ $T_J \leq 150\text{ °C}$	P_7.6.8
Maximum energy dissipation repetitive pulses - $2 \cdot I_{L(EAR)}$ (two channels in parallel)	$E_{AR}$	–	–	15	mJ	<sup>1)</sup> $T_{J(0)} = 85\text{ °C}$ $I_{L(0)} = 2 \cdot I_{L(EAR)}$ $2 \cdot 10^6$ cycles <b>HWCR.PAR</b> = "1" for affected channels	P_7.6.11
Power stage voltage drop at low battery	$V_{DS(OP)}$	–	–	1	V	$R_L = 50\ \Omega$ supplied by $V_S = 4\text{ V}$ $V_S = V_{S(OP),max}$ or $V_{DD} = 4.5\text{ V}$ , VS pin open refer to <b>Figure 17</b>	P_7.6.12
Drain to Source Output clamping voltage	$V_{DS(CL)}$	42	46	55	V	$I_L = 20\text{ mA}$	P_7.6.16
Output leakage current (each channel) $T_J \leq 85\text{ °C}$	$I_{L(OFF)}$	–	0.01	0.5	$\mu\text{A}$	<sup>1)</sup> $V_{IN} = 0\text{ V}$ or floating $V_{DS} = 28\text{ V}$ <b>OUT.OUTn</b> = 0 $T_J \leq 85\text{ °C}$	P_7.6.19

**Power Stages**

**Table 9 Electrical Characteristics: Power Stage (cont'd)**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$  (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current (each channel) $T_J = 150\text{ °C}$ (Low-Side channels)	$I_{L(OFF)}$	–	0.1	5	$\mu\text{A}$	<sup>1)</sup> $V_{IN} = 0\text{ V}$ or floating $V_{DS} = 28\text{ V}$ <b>OUT.OUTn</b> = 0 $T_J = 150\text{ °C}$	P_7.6.20

**Timings**

Turn-ON delay (from INn pin or bit to $V_{OUT} = 90\% V_S$ )	$t_{DELAY(ON)}$	1	4	8	$\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.21
Turn-OFF delay (from INn pin or bit to $V_{OUT} = 10\% V_S$ )	$t_{DELAY(OFF)}$	1	6	12	$\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.22
Turn-ON time (from INn pin or bit to $V_{OUT} = 10\% V_S$ )	$t_{ON}$	6	15	35	$\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.23
Turn-OFF time (from INn pin or bit to $V_{OUT} = 90\% V_S$ )	$t_{OFF}$	6	15	35	$\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.24
Turn-ON/OFF matching	$t_{ON} - t_{OFF}$	-10	0	10	$\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.25
Turn-ON slew rate $V_{DS} = 70\% \text{ to } 30\% V_S$	$dV/dt_{ON}$	0.7	1.3	1.9	$\text{V}/\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.26
Turn-OFF slew rate $V_{DS} = 30\% \text{ to } 70\% V_S$	$-dV/dt_{OFF}$	0.7	1.3	1.9	$\text{V}/\mu\text{s}$	$R_L = 50\ \Omega$ $V_S = 13.5\text{ V}$ Active mode or Limp Home mode	P_7.6.27
Internal reference frequency synchronization time	$t_{SYNC}$	–	5	10	$\mu\text{s}$	<sup>1)</sup>	P_7.6.45

1) Not subject to production test - specified by design

2) If one channel has  $I_{L(NOM),max}$  applied, the remaining channels must be underloaded accordingly so that  $T_J < 150\text{ °C}$

3)  $I_{L(NOM),max}$  can reach  $I_{L(OVL1),min}$

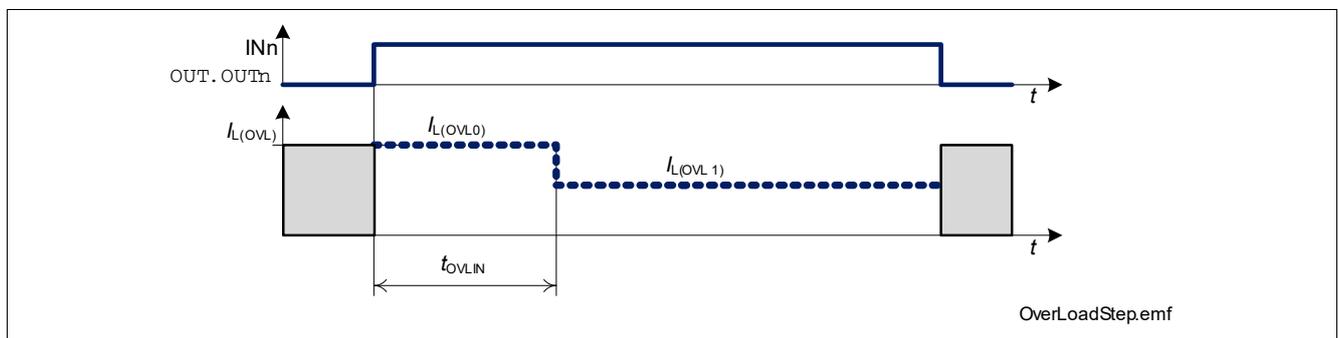
## 8 Protection Functions

### 8.1 Over Load Protection

The TLE75004-EPD is protected in case of over load or short circuit of the load. There are two over load current thresholds (see **Figure 18**):

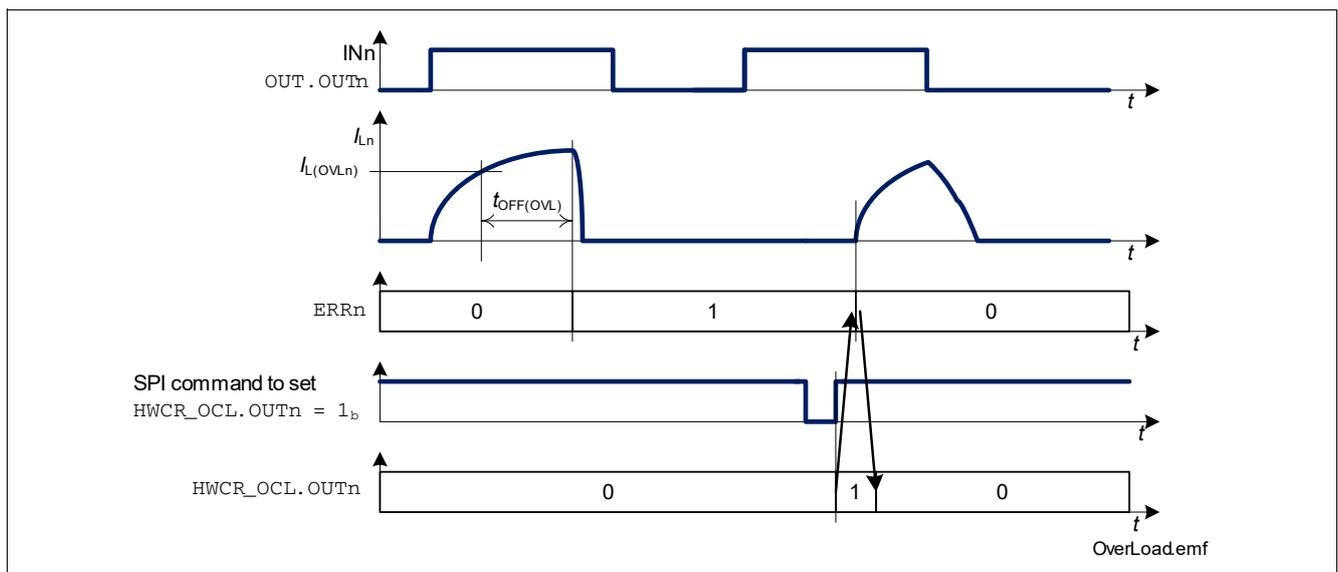
- $I_{L(OVL0)}$  between channel switch ON and  $t_{OVLIN}$
- $I_{L(OVL1)}$  after  $t_{OVLIN}$

Every time the channel is switched OFF for a time longer than  $2 * t_{SYNC}$  the over load current threshold is set back to  $I_{L(OVL0)}$ .



**Figure 18** Over Load current thresholds

In case the load current is higher than  $I_{L(OVL0)}$  or  $I_{L(OVL1)}$ , after time  $t_{OFF(OVL)}$  the over loaded channel is switched OFF and the according diagnosis bit **ERRn** is set. The channel can be switched ON after clearing the protection latch by setting the corresponding **HWCR\_OCL.OUTn** bit to “1”. This bit is set back to “0” internally after de-latching the channel. Please refer to **Figure 19** for details.



**Figure 19** Latch OFF at Over Load

### 8.2 Over Temperature Protection

A temperature sensor is integrated for each channel, causing an overheated channel to switch OFF to prevent destruction. The according diagnosis bit **ERRn** is set (combined with Over Load protection). The channel can

**Protection Functions**

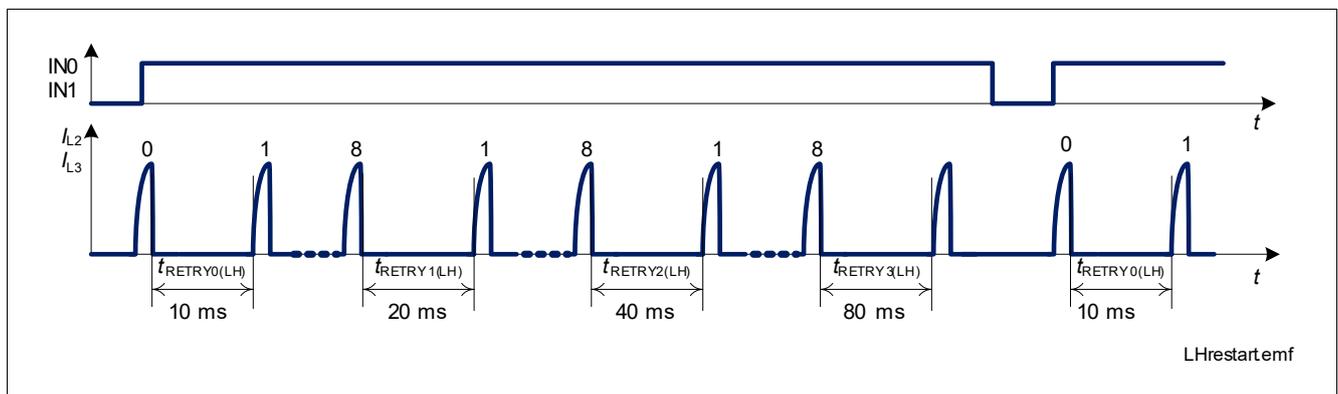
be switched ON after clearing the protection latch by setting the corresponding **HWCR\_OCL.OUTn** bit to “1”. This bit is set back to “0” internally after de-latching the channel.

**8.3 Over Temperature and Over Load Protection in Limp Home mode**

When TLE75004-EPD is in Limp Home mode, channels 2 and 3 can be switched ON using the input pins. In case of Over Load, Short Circuit or Over Temperature the channels switch OFF. If the input pins remain “high”, the channels restart with the following timings:

- 10 ms (first 8 retries)
- 20 ms (following 8 retries)
- 40 ms (following 8 retries)
- 80 ms (as long as the input pin remains “high” and the error is still present)

If at any time the input pin is set to “low” for longer than  $2 \cdot t_{SYNC}$ , the restart timer is reset. At the next channel activation while in Limp Home mode the timer starts from 10 ms again. See **Figure 20** for details. Over Load current thresholds behave as described in **Chapter 8.1**.



**Figure 20 Restart timer in Limp Home mode**

**8.4 Reverse Polarity Protection**

In Reverse Polarity (also known as Reverse Battery) condition, power dissipation is caused by the intrinsic body diode of each DMOS channel. Each ESD diode of the logic and supply pins contributes to total power dissipation. The reverse current through the channels has to be limited by the connected loads. The current through digital power supply  $V_{DD}$  and input pins has to be limited as well (please refer to the Absolute Maximum Ratings listed on **Chapter 4.1**).

*Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.*

**8.5 Over Voltage Protection**

In the case of supply voltages between  $V_{S(SC)}$  and  $V_{S(LD)}$  the output transistors are still operational and follow the input pins or the **OUT** register.

In addition to the output clamp for inductive loads as described in **Chapter 7.1.2**, there is a clamp mechanism available for over voltage protection for the logic and all channels, monitoring the voltage between VS and GND pins ( $V_{S(AZ)}$ ).

**Protection Functions**

**8.6 Electrical Characteristics Protection**

**Table 10 Electrical Characteristics Protection**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$  (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Over Load</b>							
Over Load detection current	$I_{L(OVL0)}$	1.3	1.7	2.3	A	$T_J = -40\text{ °C}$	P_8.8.19
Over Load detection current	$I_{L(OVL0)}$	1.25	1.55	2.3	A	<sup>1)</sup> $T_J = 25\text{ °C}$	P_8.8.20
Over Load detection current	$I_{L(OVL0)}$	1	1.45	2	A	$T_J = 150\text{ °C}$	P_8.8.21
Over Load detection current	$I_{L(OVL1)}$	0.7	0.95	1.3	A	$T_J = -40\text{ °C}$	P_8.8.22
Over Load detection current	$I_{L(OVL1)}$	0.65	0.85	1.3	A	<sup>1)</sup> $T_J = 25\text{ °C}$	P_8.8.23
Over Load detection current	$I_{L(OVL1)}$	0.5	0.8	1.25	A	$T_J = 150\text{ °C}$	P_8.8.24
Over Load threshold switch delay time	$t_{OVLIN}$	110	170	260	$\mu\text{s}$	<sup>1)</sup>	P_8.8.5
Over Load shut-down delay time	$t_{OFF(OVL)}$	4	7	11	$\mu\text{s}$	<sup>1)</sup>	P_8.8.26
<b>Over Temperature and Over Voltage</b>							
Thermal shut-down temperature	$T_{J(SC)}$	150	175 <sup>1)</sup>	220 <sup>1)</sup>	$^{\circ}\text{C}$		P_8.8.7
Over voltage protection	$V_{S(AZ)}$	42	50	60	V	$I_{VS} = 10\text{ mA}$ Sleep mode	P_8.8.8
<b>Reverse Polarity</b>							
Drain Source diode during reverse polarity	$V_{DS(REV)}$	-	800	-	mV	<sup>1)</sup> $I_L = -10\text{ mA}$ $T_J = 25\text{ °C}$ Sleep mode	P_8.8.9
Drain Source diode during reverse polarity	$V_{DS(REV)}$	-	650	-	mV	$I_L = -10\text{ mA}$ $T_J = 150\text{ °C}$ Sleep mode	P_8.8.10
<b>Timings</b>							
Restart time in Limp Home mode	$t_{RETRY0(LH)}$	7	10	13	ms	<sup>1)</sup>	P_8.8.13
Restart time in Limp Home mode	$t_{RETRY1(LH)}$	14	20	26	ms	<sup>1)</sup>	P_8.8.14
Restart time in Limp Home mode	$t_{RETRY2(LH)}$	28	40	52	ms	<sup>1)</sup>	P_8.8.15
Restart time in Limp Home mode	$t_{RETRY3(LH)}$	56	80	104	ms	<sup>1)</sup>	P_8.8.16

1) Not subject to production test - specified by design

Diagnosis

## 9 Diagnosis

The SPI of TLE75004-EPD provides diagnosis information about the device and the load status. Each channel diagnosis information is independent from other channels. An error condition on one channel has no influence on the diagnostic of other channels in the device (unless configured to work in parallel, see [Chapter 7.2](#) for more details).

### 9.1 Over Load and Over Temperature

When either an Over Load or an Over Temperature occurs on one channel, the diagnosis bit **ERRn** is set accordingly. As described in [Chapter 8.1](#) and [Chapter 8.2](#), the channel latches OFF and must be reactivated setting corresponding **HWCR\_OCL.OUTn** bit to “1”.

### 9.2 Output Status Monitor

The device compares each channel  $V_{DS}$  with  $V_{DS(OL)}$  and sets the corresponding **DIAG\_OSM.OUTn** bits accordingly. The bits are updated every time **DIAG\_OSM** register is read.

- $V_{DS} < V_{DS(OL)} \rightarrow \text{DIAG\_OSM\_OUTn} = \text{“1”}$

A diagnosis current  $I_{OL}$  in parallel to the power switch can be enabled by programming the **DIAG\_IOL.OUTn** bit, which can be used for Open Load at OFF detection. Each channel has its dedicated diagnosis current source. If the diagnosis current  $I_{OL}$  is enabled or if the channel changes state (ON  $\rightarrow$  OFF or OFF  $\rightarrow$  ON) it is necessary to wait a time  $t_{OSM}$  for a reliable diagnosis. Enabling  $I_{OL}$  current sources increases the current consumption of the device. Even if an Open Load is detected, the channel is not latched OFF.

See [Figure 21](#) for a timing overview (the values of **DIAG\_IOL.OUTn** refer to a channel in normal operation properly connected to the load).

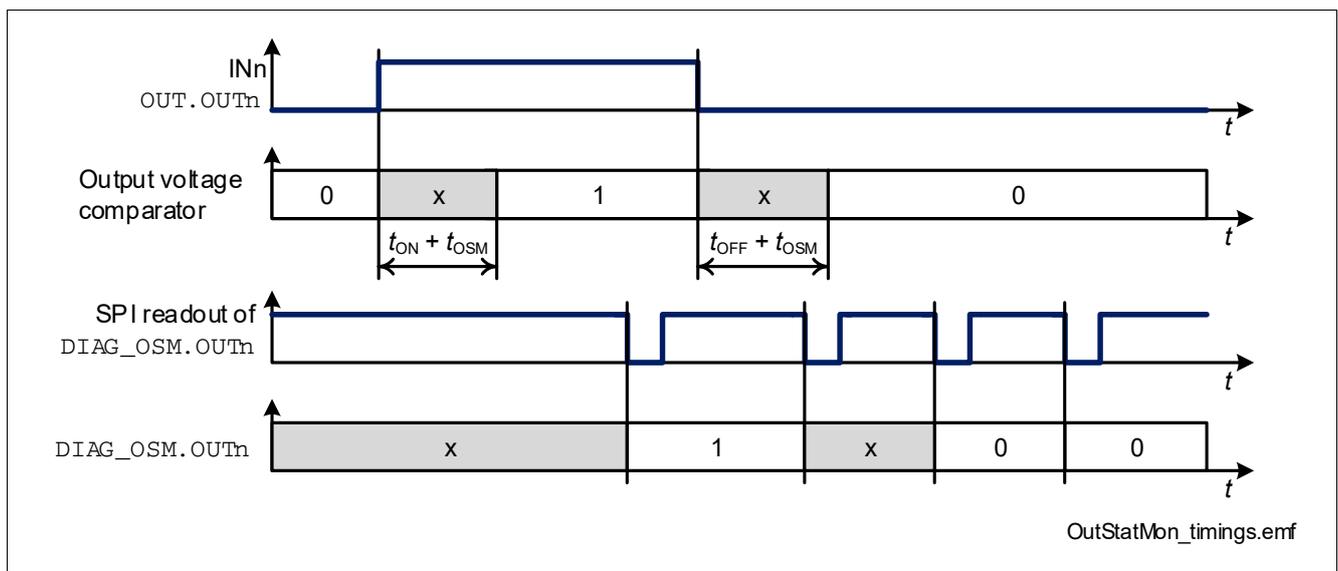


Figure 21 Output Status Monitor timing

Output Status Monitor diagnostic is available when  $V_S = V_{S(NOR)}$  and  $V_{DD} \geq V_{DD(UV)}$ .

Due to the fact that Output Status Monitor checks the voltage level at the outputs in real time, for Open Load in OFF diagnostic it is necessary to synchronize the reading of **DIAG\_OSM** register with the OFF state of the channels.

Diagnosis

Figure 22 shows how Output Status Monitor is implemented at concept level.

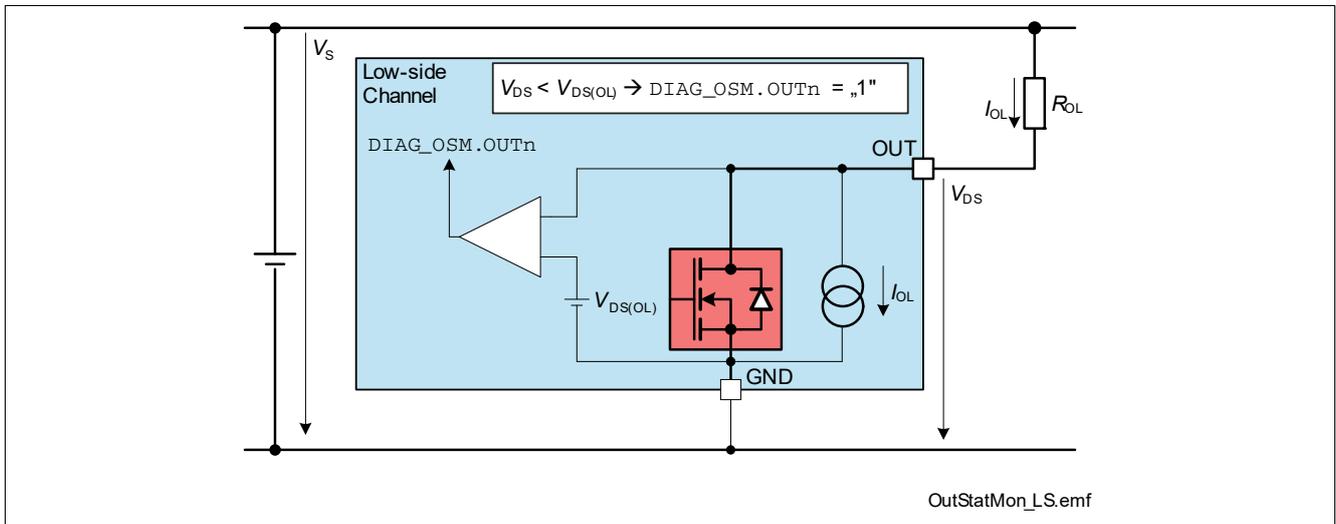


Figure 22 Output Status Monitor - concept

In Standard Diagnosis the bit **OLOFF** represents the OR combination of all **DIAG\_OSM.OUTn** bits for all channels in OFF state which have the corresponding current source  $I_{OL}$  activated.

**Diagnosis**

**9.3 Electrical Characteristics Diagnosis**

**Table 11 Electrical Characteristics Diagnosis**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$  (unless otherwise specified)  
 Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

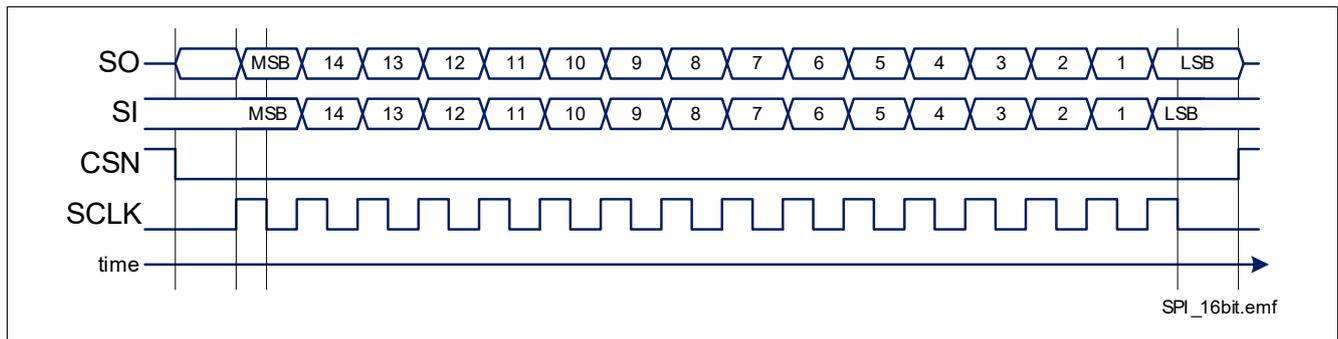
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Output Status Monitor</b>							
Output Status Monitor comparator settling time	$t_{OSM}$	–	–	20	$\mu\text{s}$	<sup>1)</sup>	P_9.5.1
Output Status Monitor threshold voltage	$V_{DS(OL)}$	3	3.3	3.6	V		P_9.5.2
Output diagnosis current	$I_{OL}$	70	85	100	$\mu\text{A}$	$V_{DS} = 3.3\text{ V}$	P_9.5.5
Open Load equivalent resistance	$R_{OL}$	30	–	300	$\text{k}\Omega$	<sup>1)</sup>	P_9.5.6

1) Not subject to production test - specified by design

**Serial Peripheral Interface (SPI)**

## 10 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a full duplex synchronous serial slave interface, which uses four lines: SO, SI, SCLK and CSN. Data is transferred by the lines SI and SO at the rate given by SCLK. The falling edge of CSN indicates the beginning of an access. Data is sampled in on line SI at the falling edge of SCLK and shifted out on line SO at the rising edge of SCLK. Each access must be terminated by a rising edge of CSN. A modulo 8/16 counter ensures that data is taken only when a multiple of 8 bit has been transferred after the first 16 bits. Otherwise a TER bit is asserted. In this way the interface provides daisy chain capability with 16 bit as well as with 8 bit SPI devices.



**Figure 23 Serial Peripheral Interface**

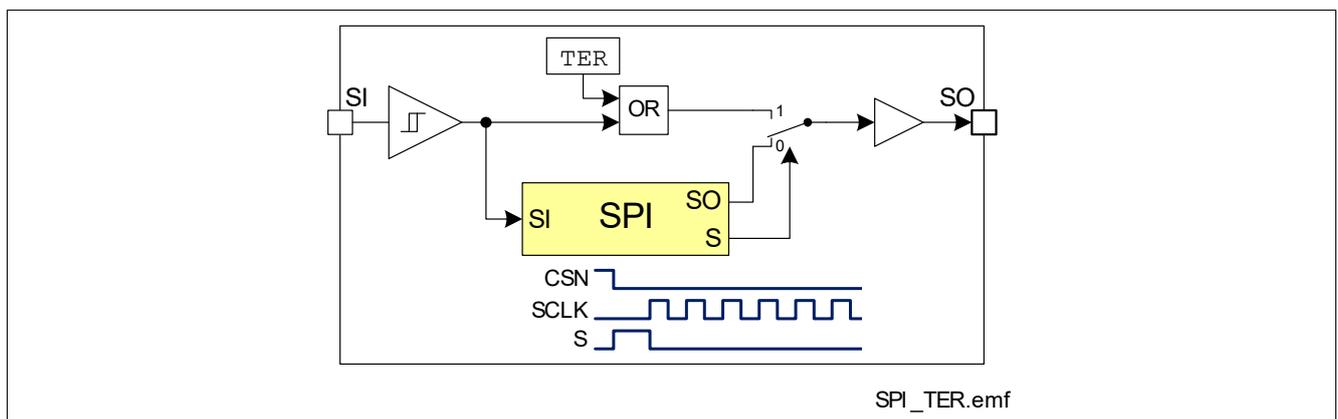
### 10.1 SPI Signal Description

#### CSN - Chip Select

The system microcontroller selects the TLE75004-EPD by means of the CSN pin. Whenever the pin is in “low” state, data transfer can take place. When CSN is in "high" state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state.

#### CSN “high” to “low” Transition

- The requested information is transferred into the shift register.
- SO changes from high impedance state to "high" or “low” state depending on the logic OR combination between the transmission error flag (TER) and the signal level at pin SI. This allows to detect a faulty transmission even in daisy chain configuration.
- If the device is in Sleep mode, SO pin remains in high impedance state and no SPI transmission occurs.



**Figure 24 Combinatorial Logic for TER bit**

**Serial Peripheral Interface (SPI)**

**CSN “low” to “high” Transition**

- Command decoding is only done, when after the falling edge of CSN exactly a multiple (1, 2, 3, ...) of eight SCLK signals have been detected after the first 16 SCLK pulses. In case of faulty transmission, the transmission error bit (**TER**) is set and the command is ignored.
- Data from shift register is transferred into the addressed register.

**SCLK - Serial Clock**

This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts diagnostic information out on the rising edge of the serial clock. It is essential that the SCLK pin is in “low” state whenever chip select CSN makes any transition, otherwise the command may be not accepted.

**SI - Serial Input**

Serial input data bits are shift-in at this pin, the most significant bit first. SI information is read on the falling edge of SCLK. The input data consists of two parts, control bits followed by data bits. Please refer to [Chapter 10.5](#) for further information.

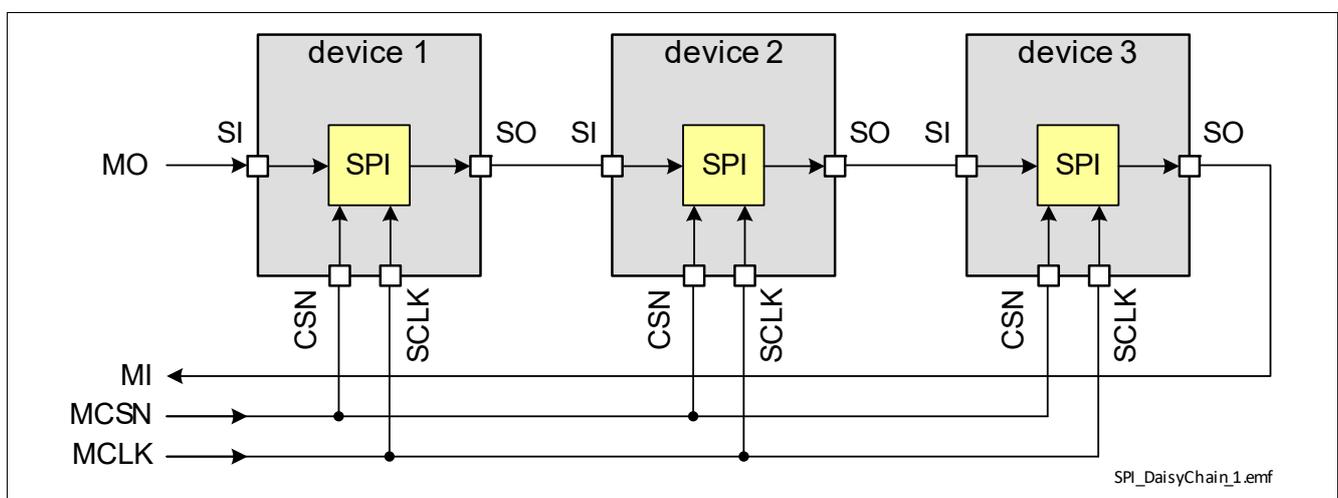
**SO Serial Output**

Data is shifted out serially at this pin, the most significant bit first. SO is in high impedance state until the CSN pin goes to “low” state. New data appears at the SO pin following the rising edge of SCLK.

Please refer to [Chapter 10.5](#) for further information.

**10.2 Daisy Chain Capability**

The SPI of TLE75004-EPD provides daisy chain capability. In this configuration several devices are activated by the same CSN signal MCSN. The SI line of one device is connected with the SO line of another device (see [Figure 25](#)), in order to build a chain. The end of the chain is connected to the output and input of the master device, MO and MI respectively. The master device provides the master clock MCLK which is connected to the SCLK line of each device in the chain.

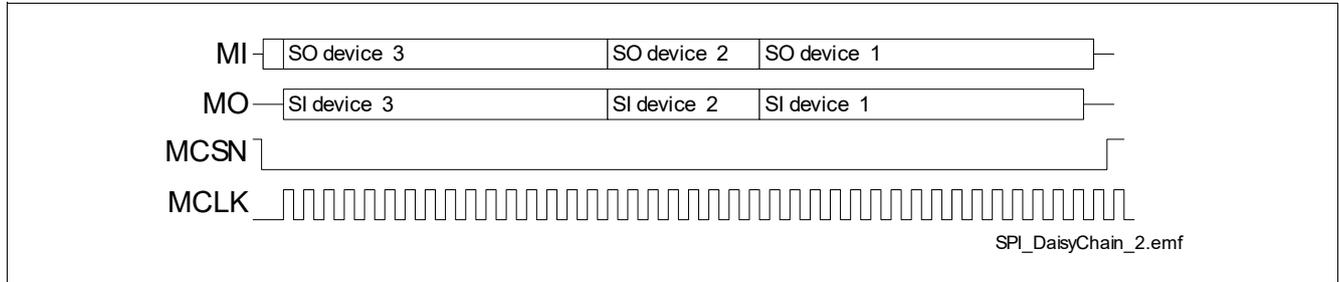


**Figure 25 Daisy Chain Configuration**

In the SPI block of each device, there is one shift register where each bit from SI line is shifted in each SCLK. The bit shifted out occurs at the SO pin. After sixteen SCLK cycles, the data transfer for one device is finished.

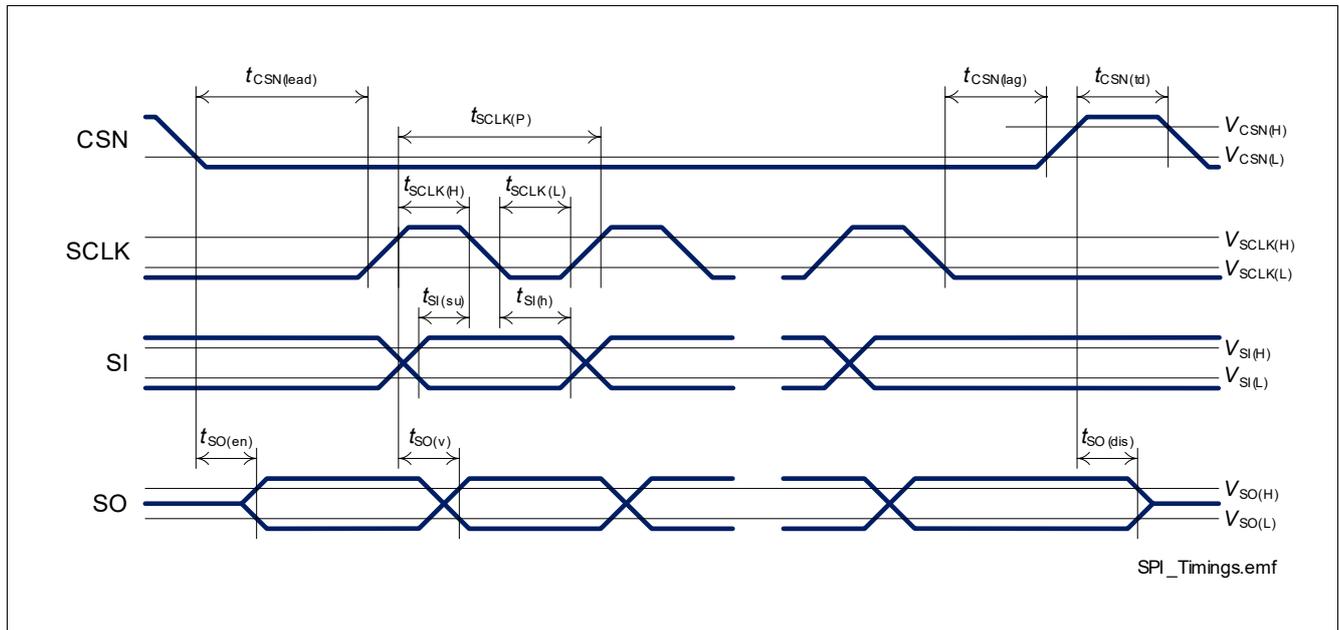
**Serial Peripheral Interface (SPI)**

In single chip configuration, the CSN line must turn “high” to make the device acknowledge the transferred data. In daisy chain configuration, the data shifted out at device 1 has been shifted in to device 2. When using three devices in daisy chain, several multiples of 8 bits have to be shifted through the devices (depending on how many devices with 8 bit SPI and how many with 16 bit SPI). After that, the MCSN line must turn “high” (see [Figure 26](#)).



**Figure 26 Data Transfer in Daisy Chain Configuration**

**10.3 Timing Diagrams**



**Figure 27 Timing Diagram SPI Access**

**Serial Peripheral Interface (SPI)**

**10.4 Electrical Characteristics**

$V_{DD} = 3\text{ V to }5.5\text{ V}$ ,  $V_S = 7\text{ V to }18\text{ V}$ ,  $T_J = -40\text{ °C to }+150\text{ °C}$  (unless otherwise specified)

Typical values:  $V_{DD} = 5\text{ V}$ ,  $V_S = 13.5\text{ V}$ ,  $T_J = 25\text{ °C}$

**Table 12 Electrical Characteristics Serial Peripheral Interface (SPI)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input Characteristics (CSN, SCLK, SI) - “low” level of pin</b>							
CSN	$V_{CSN(L)}$	0	–	0.8	V	–	P_10.4.1
SCLK	$V_{SCLK(L)}$	0	–	0.8	V	–	P_10.4.2
SI	$V_{SI(L)}$	0	–	0.8	V	–	P_10.4.3
<b>Input Characteristics (CSN, SCLK, SI) - “high” level of pin</b>							
CSN	$V_{CSN(H)}$	2	–	$V_{DD}$	V	–	P_10.4.4
SCLK	$V_{SCLK(H)}$	2	–	$V_{DD}$	V	–	P_10.4.5
SI	$V_{SI(H)}$	2	–	$V_{DD}$	V	–	P_10.4.6
<b>Input Pull-Up Current at Pin CSN</b>							
L-input pull-up current at CSN pin	$-I_{CSN(L)}$	30	60	90	$\mu\text{A}$	$V_{DD} = 5\text{ V}$ $V_{CSN} = 0.8\text{ V}$	P_10.4.7
H-input pull-up current at CSN pin	$-I_{CSN(H)}$	20	40	65	$\mu\text{A}$	$V_{DD} = 5\text{ V}$ $V_{CSN} = 2\text{ V}$	P_10.4.8
<b>L-Input Pull-Down Current at Pin</b>							
SCLK	$I_{SCLK(L)}$	5	12	20	$\mu\text{A}$	$V_{SCLK} = 0.8\text{ V}$	P_10.4.9
SI	$I_{SI(L)}$	5	12	20	$\mu\text{A}$	$V_{SI} = 0.8\text{ V}$	P_10.4.10
<b>H-Input Pull-Down Current at Pin</b>							
SCLK	$I_{SCLK(H)}$	14	28	45	$\mu\text{A}$	$V_{SCLK} = 2\text{ V}$	P_10.4.11
SI	$I_{SI(H)}$	14	28	45	$\mu\text{A}$	$V_{SI} = 2\text{ V}$	P_10.4.12
<b>Output Characteristics (SO)</b>							
L level output voltage	$V_{SO(L)}$	0	–	0.4	V	$I_{SO} = -1.5\text{ mA}$	P_10.4.13
H level output voltage	$V_{SO(H)}$	$V_{DD} - 0.4$	–	$V_{DD}$	V	$I_{SO} = 1.5\text{ mA}$	P_10.4.14
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	$\mu\text{A}$	$V_{CSN} = V_{DD}$ $V_{SO} = 0\text{ V}$	P_10.4.15
Output tristate leakage current	$I_{SO(OFF)}$	-1	–	1	$\mu\text{A}$	$V_{CSN} = V_{DD}$ $V_{SO} = V_{DD}$	P_10.4.16
<b>Timings</b>							
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(lead)}$	200	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.17
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(lag)}$	200	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.18

**Serial Peripheral Interface (SPI)**

**Table 12 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(td)}$	250	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.19
Output enable time (falling CSN to SO valid)	$t_{SO(en)}$	–	–	200	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$ $C_L = 20\text{ pF at SO pin}$	P_10.4.20
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	200	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$ $C_L = 20\text{ pF at SO pin}$	P_10.4.21
Serial clock frequency	$f_{SCLK}$	–	–	5	MHz	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.22
Serial clock period	$t_{SCLK(P)}$	200	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.23
Serial clock “high” time	$t_{SCLK(H)}$	75	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.24
Serial clock “low” time	$t_{SCLK(L)}$	75	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.25
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	20	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.26
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	20	–	–	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$	P_10.4.27
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	100	ns	<sup>1)</sup> $V_{DD} = 4.5\text{ V or }V_S > 7\text{ V}$ $C_L = 20\text{ pF at SO pin}$	P_10.4.28
Enable lead time (falling CSN to rising SCLK)	$t_{CSN(lead)}$	1	–	–	$\mu\text{s}$	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.29
Enable lag time (falling SCLK to rising CSN)	$t_{CSN(lag)}$	1	–	–	$\mu\text{s}$	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.30
Transfer delay time (rising CSN to falling CSN)	$t_{CSN(td)}$	1.25	–	–	$\mu\text{s}$	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.31

**Serial Peripheral Interface (SPI)**

**Table 12 Electrical Characteristics Serial Peripheral Interface (SPI) (cont'd)**

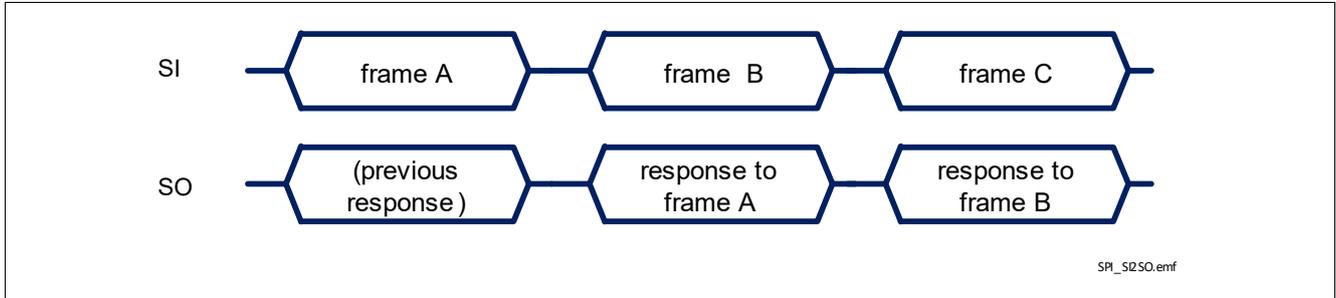
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output enable time (falling CSN to SO valid)	$t_{SO(en)}$	–	–	1	$\mu\text{s}$	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$ $C_L = 20\text{ pF}$ at SO pin	P_10.4.32
Output disable time (rising CSN to SO tristate)	$t_{SO(dis)}$	–	–	1	$\mu\text{s}$	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$ $C_L = 20\text{ pF}$ at SO pin	P_10.4.33
Serial clock frequency	$f_{SCLK}$	–	–	1	MHz	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.34
Serial clock period	$t_{SCLK(P)}$	1	–	–	$\mu\text{s}$	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.35
Serial clock “high” time	$t_{SCLK(H)}$	375	–	–	ns	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.36
Serial clock “low” time	$t_{SCLK(L)}$	375	–	–	ns	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.37
Data setup time (required time SI to falling SCLK)	$t_{SI(su)}$	100	–	–	ns	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.38
Data hold time (falling SCLK to SI)	$t_{SI(h)}$	100	–	–	ns	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$	P_10.4.39
Output data valid time with capacitive load	$t_{SO(v)}$	–	–	500	ns	<sup>1)</sup> $V_{DD} = V_S = 3.0\text{ V}$ $C_L = 20\text{ pF}$ at SO pin	P_10.4.40

1) Not subject to production test, specified by design

**Serial Peripheral Interface (SPI)**

**10.5 SPI Protocol**

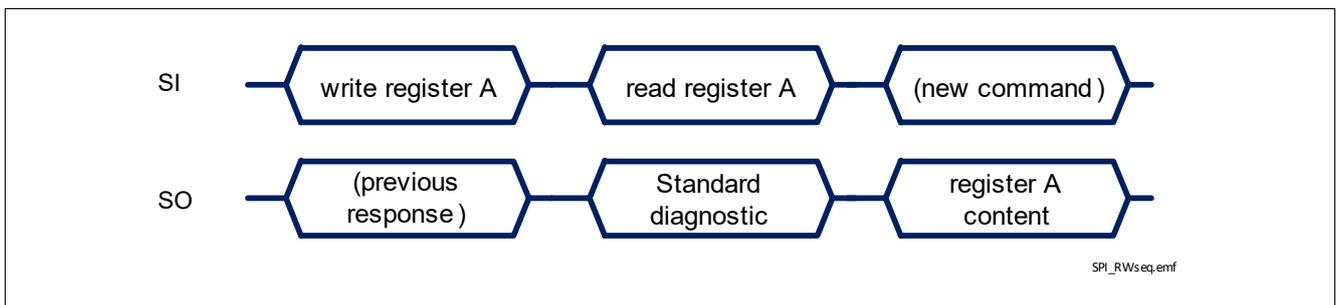
The relationship between SI and SO content during SPI communication is shown in **Figure 28**. SI line represents the frame sent from the  $\mu\text{C}$  and SO line is the answer provided by TLE75004-EPD.



**Figure 28 Relationship between SI and SO during SPI communication**

The SPI protocol provides the answer to a command frame only with the next transmission triggered by the  $\mu\text{C}$ . Although the biggest majority of commands and frames implemented in TLE75004-EPD can be decoded without the knowledge of what happened before, it is advisable to consider what the  $\mu\text{C}$  sent in the previous transmission to decode TLE75004-EPD response frame completely.

More in detail, the sequence of commands to “read” and “write” the content of a register looks as follows:



**Figure 29 Register content sent back to  $\mu\text{C}$**

There are 3 special situations where the frame sent back to the  $\mu\text{C}$  is not related directly to the previous received frame:

- in case an error in transmission happened during the previous frame (for instance, the clock pulses were not multiple of 8 with a minimum of 16 bits), shown in **Figure 30**
- when TLE75004-EPD logic supply comes out of Power-On reset condition or after a Software Reset, as shown in **Figure 31**
- in case of command syntax errors
  - “write” command starting with “11” instead of “10”
  - “read” command starting with “00” instead of “01”
  - “read” or “write” commands on registers which are “reserved” or “not used”

Serial Peripheral Interface (SPI)

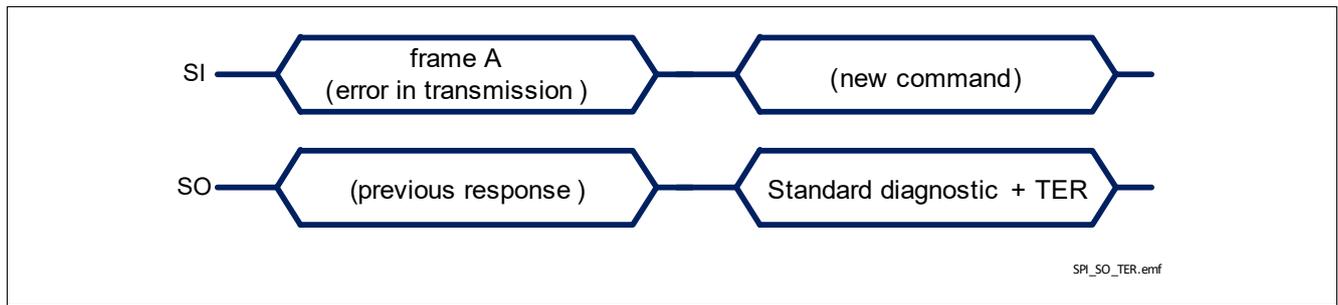


Figure 30 TLE75004-EPD response after a error in transmission

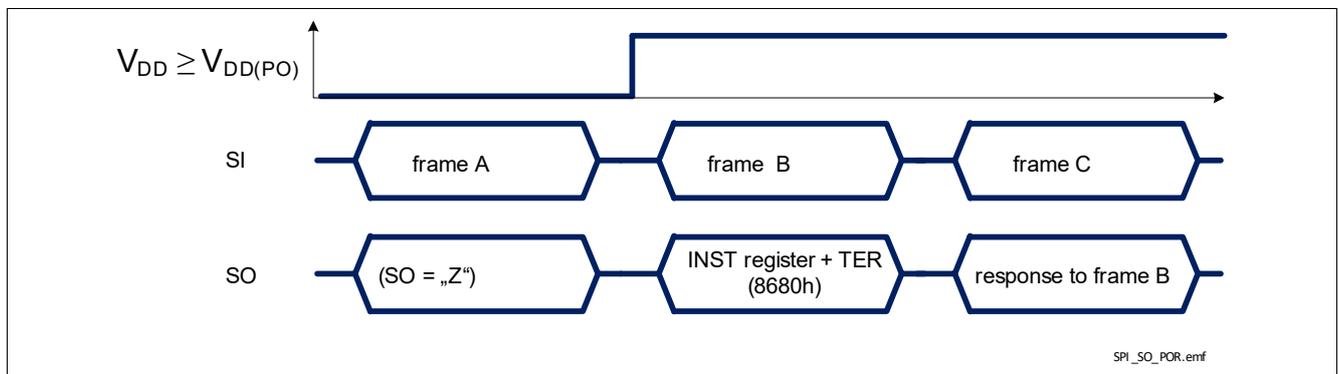


Figure 31 TLE75004-EPD response after coming out of Power-On reset at  $V_{DD}$

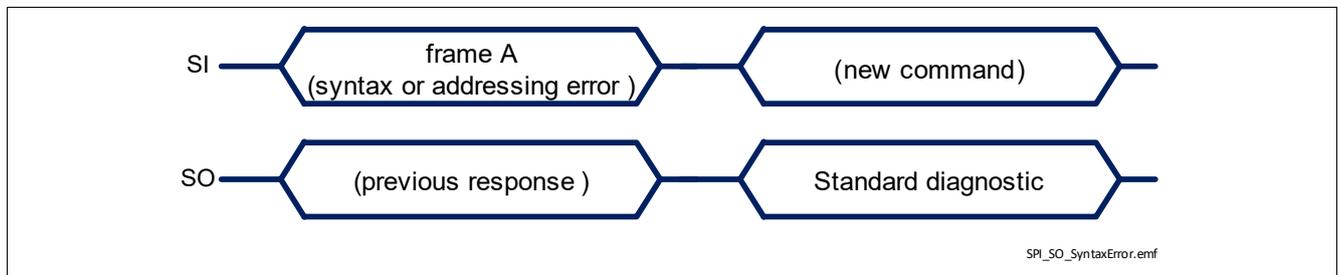


Figure 32 TLE75004-EPD response after a command syntax error

A summary of all possible SPI commands is presented in [Table 13](#), including the answer that TLE75004-EPD sends back at the next transmission.

**Serial Peripheral Interface (SPI)**

**Table 13 SPI Command summary<sup>1)</sup>**

<b>Requested Operation</b>	<b>Frame sent to SPIDER+ (SI pin)</b>	<b>Frame received from SPIDER+ (SO pin) with the next command</b>
Read Standard Diagnosis	0xxxxxxxxxxxxxxxxx01 <sub>B</sub> ("xxxxxxxxxxxxxxxx <sub>B</sub> " = don't care)	0ddddddddddddddd <sub>B</sub> (Standard Diagnosis)
Write 8 bit register	10aaaabbcccccccc <sub>B</sub> where: "aaaa <sub>B</sub> " = register address ADDR0 "bb <sub>B</sub> " = register address ADDR1 "cccccccc <sub>B</sub> " = new register content	0ddddddddddddddd <sub>B</sub> (Standard Diagnosis)
Read 8 bit registers	01aaaabbxxxxxxxx10 <sub>B</sub> where: "aaaa <sub>B</sub> " = register address ADDR0 "bb <sub>B</sub> " = register address ADDR1 "xxxxxxxx <sub>B</sub> " = don't care	10aaaabbcccccccc <sub>B</sub> where: "aaaa <sub>B</sub> " = register address ADDR0 "bb <sub>B</sub> " = register address ADDR1 "cccccccc <sub>B</sub> " = register content

1) "a" = address bits for ADDR0 field, "b" = address bit for ADDR1 field, "c" = register content, "d" = diagnostic bit

Serial Peripheral Interface (SPI)

## 10.6 SPI Registers Overview

### 10.6.1 Standard Diagnosis

**Table 14 Standard Diagnosis**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---	---------

0	UVR VS	LOP VDD	MODE	TER	0	OL OFF	0	0	0	0	0	ERR				7800 <sub>H</sub>
---	-----------	------------	------	-----	---	-----------	---	---	---	---	---	-----	--	--	--	-------------------

Field	Bits	Type	Description
UVRVS	14	r	<b>V<sub>S</sub> Undervoltage Monitor</b> 0 <sub>B</sub> No undervoltage condition on V <sub>S</sub> detected (see <a href="#">Chapter 6.2.1</a> for more details) 1 <sub>B</sub> (default) There was at least one V <sub>S</sub> Undervoltage condition since last Standard Diagnosis readout
LOPVDD	13	r	<b>V<sub>DD</sub> Lower Operating Range Monitor</b> 0 <sub>B</sub> V <sub>DD</sub> is above V <sub>DD(LOP)</sub> 1 <sub>B</sub> (default) There was at least one “V <sub>DD</sub> = V <sub>DD(LOP)</sub> ” condition since last Standard Diagnosis readout
MODE	12:11	r	<b>Operative Mode Monitor</b> 00 <sub>B</sub> (reserved) 01 <sub>B</sub> Limp Home Mode 10 <sub>B</sub> Active Mode 11 <sub>B</sub> (default) Idle Mode
TER	10	r	<b>Transmission Error</b> 0 <sub>B</sub> Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1 <sub>B</sub> (default) Previous transmission failed The first frame after a reset is <b>TER</b> set to “high” and the <b>INST</b> register. The second frame is the Standard Diagnosis with <b>TER</b> set to “low” (if there was no fail in the previous transmission).
OLOFF	8	r	<b>Open Load in OFF Diagnosis</b> 0 <sub>B</sub> (default) All channels in OFF state (which have <b>DIAG_IOL.OUTn</b> bit set to “1”) have V <sub>DS</sub> > V <sub>DS(OL)</sub> 1 <sub>B</sub> At least one channel in OFF state (with <b>DIAG_IOL.OUTn</b> bit set to “1”) has V <sub>DS</sub> < V <sub>DS(OL)</sub> Channels in ON state are not considered
ERRn n = 3 to 0	n:0	r	<b>Over Load / Over Temperature Diagnosis of channel n</b> 0 <sub>B</sub> (default) No failure detected 1 <sub>B</sub> Over Temperature or Over Load bits 7:4 - reserved (default: 0 <sub>B</sub> )

Serial Peripheral Interface (SPI)

10.6.2 Register structure

The register banks the digital part have following structure:

**Table 15 Register structure - all registers**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
r = 0 w = 1	r = 1 w = 0	ADDR0				ADDR1			DATA							XXXX <sub>H</sub>

**Table 16** summarizes the available registers with their addressing space and size

**Table 16 Register addressing space**

Register name	ADDR0	ADDR1	Size	Type	Purpose
<b>OUT</b>  n = 3 to 0	0000 <sub>B</sub>	00 <sub>B</sub>	n	r/w	<b>Power output control register</b> bits OUT . OUTn 0 <sub>B</sub> (default) Output is OFF 1 <sub>B</sub> Output is ON bits 7:4 - reserved (read default: 0 <sub>B</sub> , write ignored)
<b>MAPIN0</b>  n = 3 to 0	0001 <sub>B</sub>	00 <sub>B</sub>	n	r/w	<b>Input Mapping (Input Pin 0)</b> bits MAPIN0 . OUTn 0 <sub>B</sub> (default) The output is not connected to the input pin 1 <sub>B</sub> The output is connected to the input pin Note: Channel 2 has the corresponding bit set to “1” by default bits 7:4 - reserved (read default: 0 <sub>B</sub> , write ignored)
<b>MAPIN1</b>  n = 3 to 0	0001 <sub>B</sub>	01 <sub>B</sub>	n	r/w	<b>Input Mapping (Input Pin 1)</b> bits MAPIN1 . OUTn 0 <sub>B</sub> (default) The output is not connected to the input pin 1 <sub>B</sub> The output is connected to the input pin Note: Channel 3 has the corresponding bit set to “1” by default bits 7:4 - reserved (read default: 0 <sub>B</sub> , write ignored)
<b>INST</b>	0001 <sub>B</sub>	10 <sub>B</sub>	8	r	<b>Input Status Monitor</b> bit TER 0 <sub>B</sub> Previous transmission was successful (modulo 16 + n*8 clocks received, where n = 0, 1, 2...) 1 <sub>B</sub> (default) Previous transmission failed bits INST . RES (6:2) - reserved bits INST . INn (1:0) 0 <sub>B</sub> (default) The input pin is set to “low” 1 <sub>B</sub> The input pin is set to “high” First register transmitted after a reset of the logic

Serial Peripheral Interface (SPI)

**Table 16 Register addressing space (cont'd)**

Register name	ADDR0	ADDR1	Size	Type	Purpose
<b>DIAG_IOL</b>  n = 3 to 0	0010 <sub>B</sub>	00 <sub>B</sub>	n	r/w	<b>Open Load diagnostic current control</b> bits DIAG_IOL . OUTn 0 <sub>B</sub> (default) Diagnosis current not enabled 1 <sub>B</sub> Diagnosis current enabled bits 7:4 - reserved (read default: 0 <sub>B</sub> , write ignored)
<b>DIAG_OSM</b>  n = 3 to 0	0010 <sub>B</sub>	01 <sub>B</sub>	n	r	<b>Output Status Monitor</b> bits DIAG_OSM . OUTn 0 <sub>B</sub> (default) $V_{DS} > V_{DS(OL)}$ 1 <sub>B</sub> $V_{DS} < V_{DS(OL)}$ bits 7:4 - reserved (default: 0 <sub>B</sub> )
<b>HWCR</b>	0011 <sub>B</sub>	00 <sub>B</sub>	8	r/w	<b>Hardware Configuration Register</b> bit HWCR . ACT (7) (Active Mode) 0 <sub>B</sub> (default) Normal operation or device leaves Active Mode 1 <sub>B</sub> Device enters Active Mode (see <a href="#">Chapter 6.1</a> for a description of the possible operative mode transitions) bit HWCR . RST (6) (Reset) 0 <sub>B</sub> (default) Normal operation 1 <sub>B</sub> Execute Reset command (self clearing) bits HWCR . PAR (1:0) (channels operating in parallel) 0 <sub>B</sub> (default) Normal operation 1 <sub>B</sub> two neighbour channels have Over Load and Over Temperature synchronized (see <a href="#">Chapter 7.2</a> for more details)  bits 5:2 - reserved (read default: 0 <sub>B</sub> , write ignored)
<b>HWCR_OCL</b>  n = 3 to 0	0011 <sub>B</sub>	01 <sub>B</sub>	n	w	<b>Output Clear Latch</b> bits HWCR_OCL . OUTn 0 <sub>B</sub> (default) Normal operation 1 <sub>B</sub> Clear the error latch for the selected output bits 7:4 - reserved (default: 0 <sub>B</sub> , write ignored)

**10.6.3 Register summary**

All registers with addresses not mentioned in [Table 17](#) have to be considered as “reserved”. “Read” operations performed on those registers return the Standard Diagnosis. The column “Default” indicates the content of the register (8 bits) after a reset.

**Table 17 Addressable registers**

15	14	13-10	9	8	7	6	5	4	3	2	1	0	Default
r = 0 w = 1	r = 1 w = 0	0000	00		(reserved)								<b>OUT.OUTn</b>  00 <sub>H</sub>
r = 0 w = 1	r = 1 w = 0	0001	00		(reserved)								<b>MAPIN0.OUTn</b>  04 <sub>H</sub>

Serial Peripheral Interface (SPI)

**Table 17** Addressable registers

15	14	13-10	9	8	7	6	5	4	3	2	1	0	Default
r = 0 w = 1	r = 1 w = 0	0001	01		(reserved)				MAPIN1.OUTn			08 <sub>H</sub>	
0	1	0001	10		TER	(reserved)				INST.INn		00 <sub>H</sub>	
r = 0 w = 1	r = 1 w = 0	0010	00		(reserved)				DIAG_IOL.OUTn			00 <sub>H</sub>	
0	1	0010	01		(reserved)				DIAG_OSM.OUTn			00 <sub>H</sub>	
r = 0 w = 1	r = 1 w = 0	0011	00		HWC R.ACT	HWC R.RST	(reserved)				HWCR.PAR		00 <sub>H</sub>
r = 0 w = 1	r = 1 w = 0	0011	01		(reserved)				HWCR_OCL.OUTn			00 <sub>H</sub>	

**10.6.4 SPI command quick list**

A summary of the most used SPI commands (read and write operations on all registers) is shown in **Table 18**

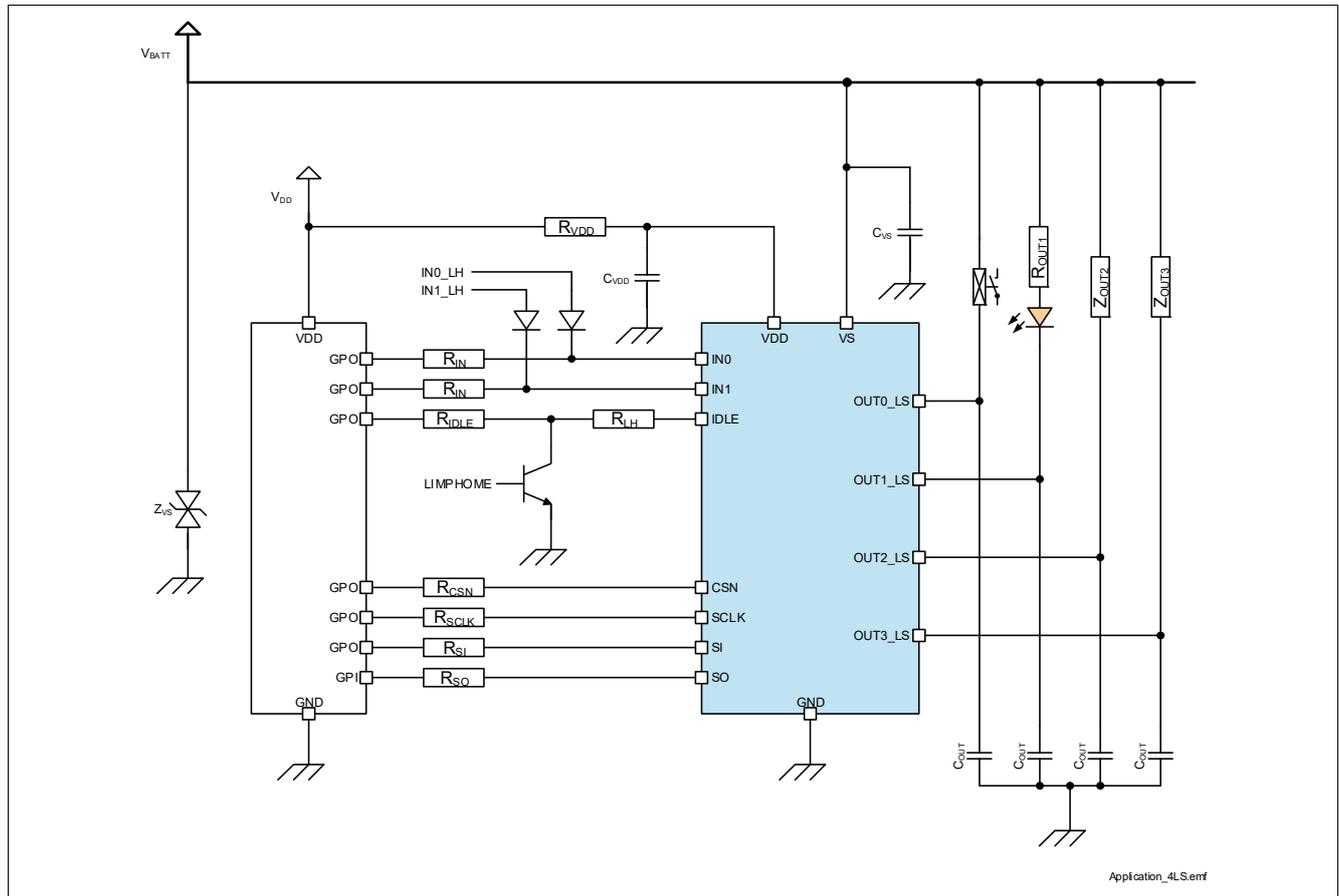
**Table 18** SPI command quick list

Register	“read” command”	“write” command	content written
<b>OUT</b>	4002 <sub>H</sub>	80XX <sub>H</sub>	XX <sub>H</sub> = xxxxxxxx <sub>B</sub>
<b>MAPIN0</b>	4402 <sub>H</sub>	84XX <sub>H</sub>	XX <sub>H</sub> = xxxxxxxx <sub>B</sub>
<b>MAPIN1</b>	4502 <sub>H</sub>	85XX <sub>H</sub>	XX <sub>H</sub> = xxxxxxxx <sub>B</sub>
<b>INST</b>	4602 <sub>H</sub>	n.a. (read-only)	–
<b>DIAG_IOL</b>	4802 <sub>H</sub>	88XX <sub>H</sub>	XX <sub>H</sub> = xxxxxxxx <sub>B</sub>
<b>DIAG_OSM</b>	4902 <sub>H</sub>	n.a. (read-only)	–
<b>HWCR</b>	4C02 <sub>H</sub>	8CXX <sub>H</sub>	XX <sub>H</sub> = xxxxxxxx <sub>B</sub>
<b>HWCR_OCL</b>	4D02 <sub>H</sub>	8DXX <sub>H</sub>	XX <sub>H</sub> = xxxxxxxx <sub>B</sub>

**Application Information**

**11 Application Information**

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*



**Figure 33 TLE75004-EPD Application Diagram**

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

**Table 19 Suggested Component values**

Reference	Value	Purpose
$R_{IN}$	4.7 k $\Omega$	Protection of the micro-controller during Over Voltage and Reverse Polarity Guarantee TLE75004-EPD channels OFF during Loss of Ground
$R_{IDLE}$	4.7 k $\Omega$	Protection of the micro-controller during Over Voltage and Reverse Polarity Guarantee TLE75004-EPD channels OFF during Loss of Ground
$R_{CSN}$	500 $\Omega$	Protection of the micro-controller during Over Voltage and Reverse Polarity
$R_{SCLK}$	500 $\Omega$	Protection of the micro-controller during Over Voltage and Reverse Polarity
$R_{SI}$	500 $\Omega$	Protection of the micro-controller during Over Voltage and Reverse Polarity
$R_{SO}$	500 $\Omega$	Protection of the micro-controller during Over Voltage and Reverse Polarity
$R_{VDD}$	100 $\Omega$	Logic supply voltage spikes filtering

---

**Application Information**

**Table 19 Suggested Component values** (cont'd)

<b>Reference</b>	<b>Value</b>	<b>Purpose</b>
$C_{VDD}$	100 nF	Logic supply voltage spikes filtering
$C_{VS}$	68 nF	Analog supply voltage spikes filtering
$Z_{VS}$	P6SMB30	Protection of device during Over Voltage. Zener diode
$C_{OUT}$	10 nF	Protection of TLE75004-EPD against ESD and BCI

**11.1 Further Application Information**

- Please contact us for information regarding the Pin FMEA
- For further information you may contact <http://www.infineon.com/>

## 12 Package Outlines

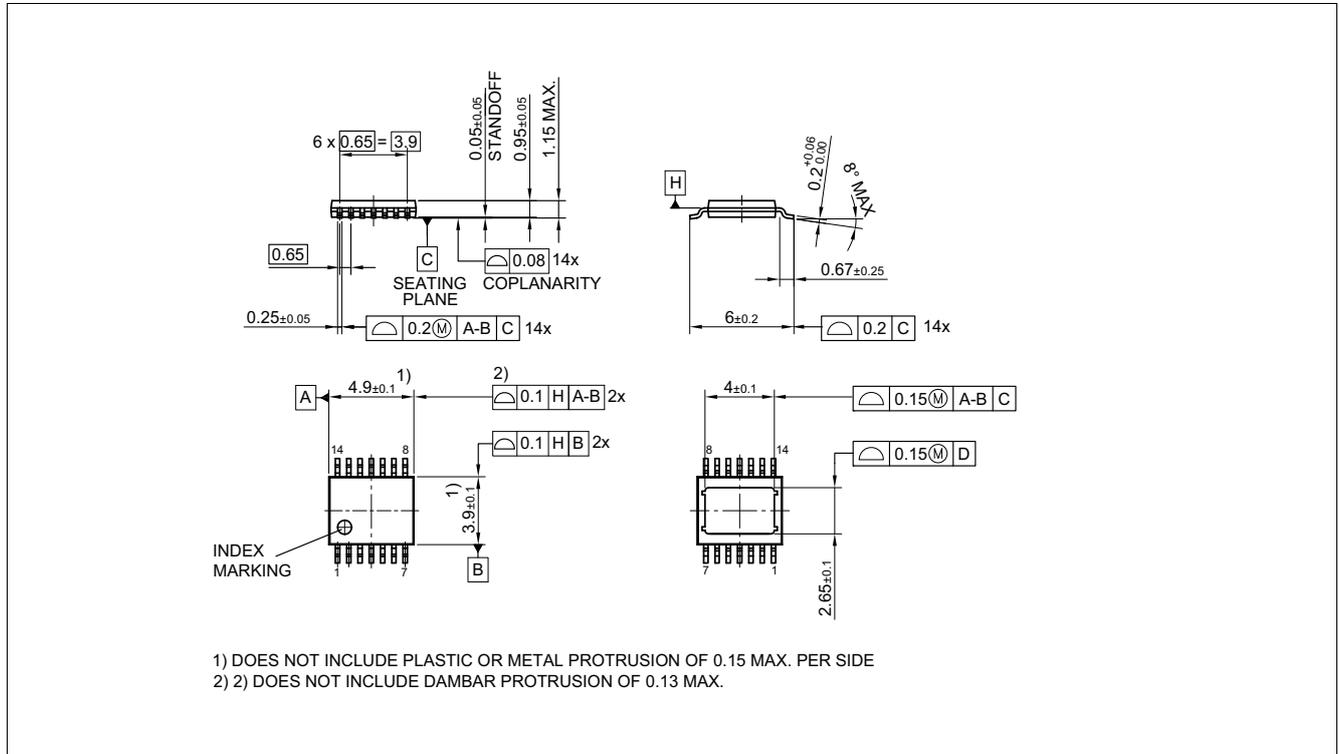


Figure 34 PG-TSDSO-14 Package drawing

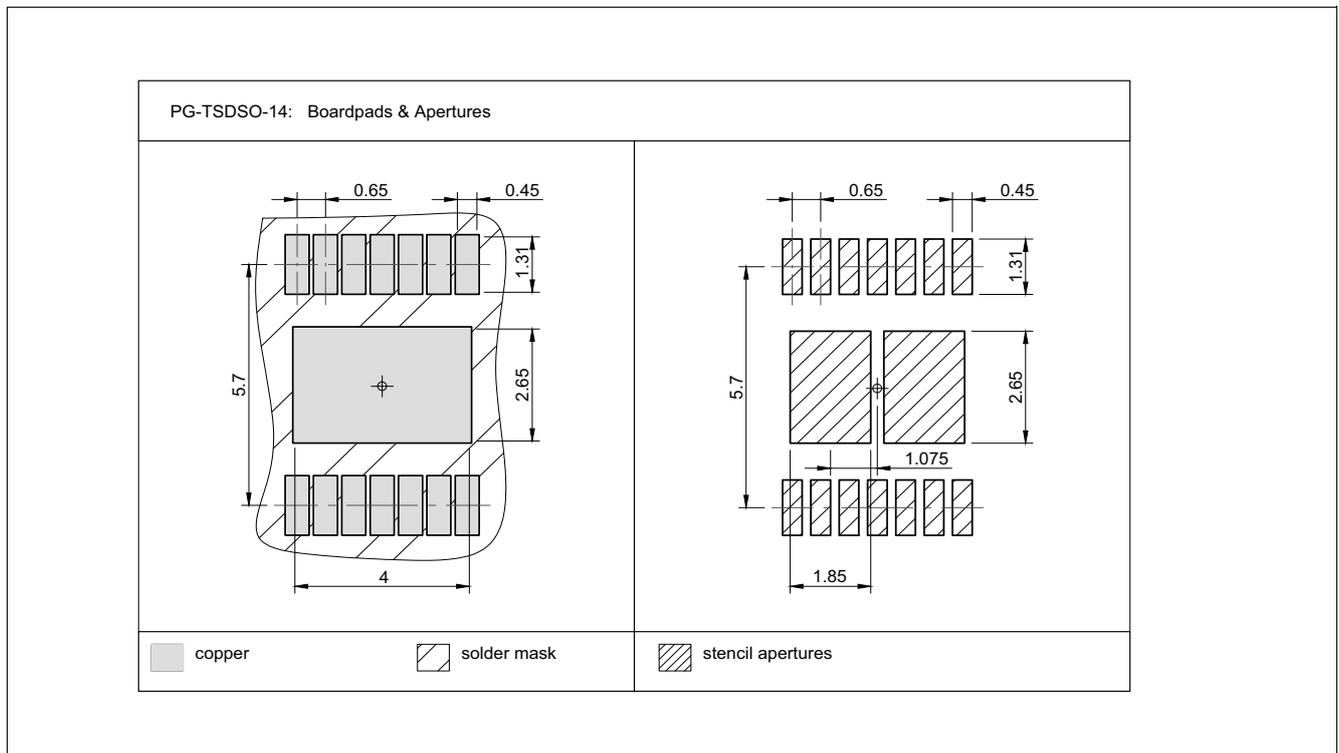


Figure 35 TLE75004-EPD Package pads and stencil

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**Package Outlines**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Revision History

### 13 Revision History

Page or Item	Changes since previous revision
<b>Rev. 1.10, 2020-09-02</b>	
All	Package name updated
<b>Table 2</b>	Updated ESD susceptibility footnotes for HBM and CDM
	Updated backcover
<b>Rev.1.00, 2017-11-23</b>	
All	Datasheet released
TLE75004-EPD	

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**Email: [erratum@infineon.com](mailto:erratum@infineon.com)**

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