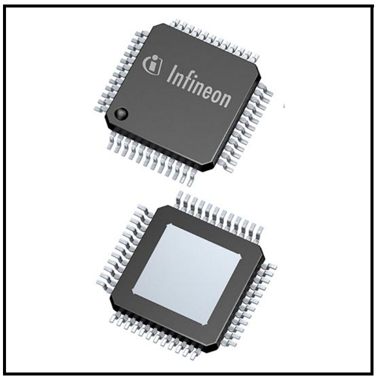
TLE9012AQU

Li-Ion Battery Monitoring and Balancing IC



Features

- General
  - Monitors up to 12 cells connected in series
  - Supports communication of up to 20 devices
  - Supports hot plugging
- Voltage measurement
  - 16 bit high resolution ADC measurement for each cell
  - High accuracy measurement for SoC (State-of-Charge) and SoH (State-of-Health) calculation
  - Temperature compensated measurements
  - Built-in noise filtering
  - Selectable measurement bit length
- Temperature measurement
  - 5 temperature measurement channels for connection to external NTC
  - Internal temperature measurement
- Balancing
  - Integrated balancing switch allowing up to 150 mA balancing current
- Communication Bus (iso UART)
  - Differential robust serial interface for communication between battery blocks
  - High speed communication with 2 Mbps
  - Power balanced communication scheme
- Additional 4 GPIO pins to e.g. connect an external EEPROM
- Green product (RoHS-compliant)
- ISO-26262 ready, supporting ASIL-C BMS safety applications[1)]

Safety features

- Two independent internal voltage references
- Block voltage measurement based on different ADCs
- Configurable analog OV/UV comparators
- End-to-end CRC secured communication
- CRC secured configuration registers
- Internal open load detection

1) according to ISO 26262-8 clause 13 first edition

- Emergency mode signaling using iso UART lines

Potential applications

- Multi-cell battery monitoring and balancing system IC designed for Li-Ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as in 12 V Lithium-Ion batteries

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE9012AQU provides the main function of monitoring the temperature of the battery and voltage of each cell as well as the communication to the host controller.

Type	Package	Marking
TLE9012AQU	PG-TQFP-48	TLE9012AQU

Table of Contents

1 Block diagram

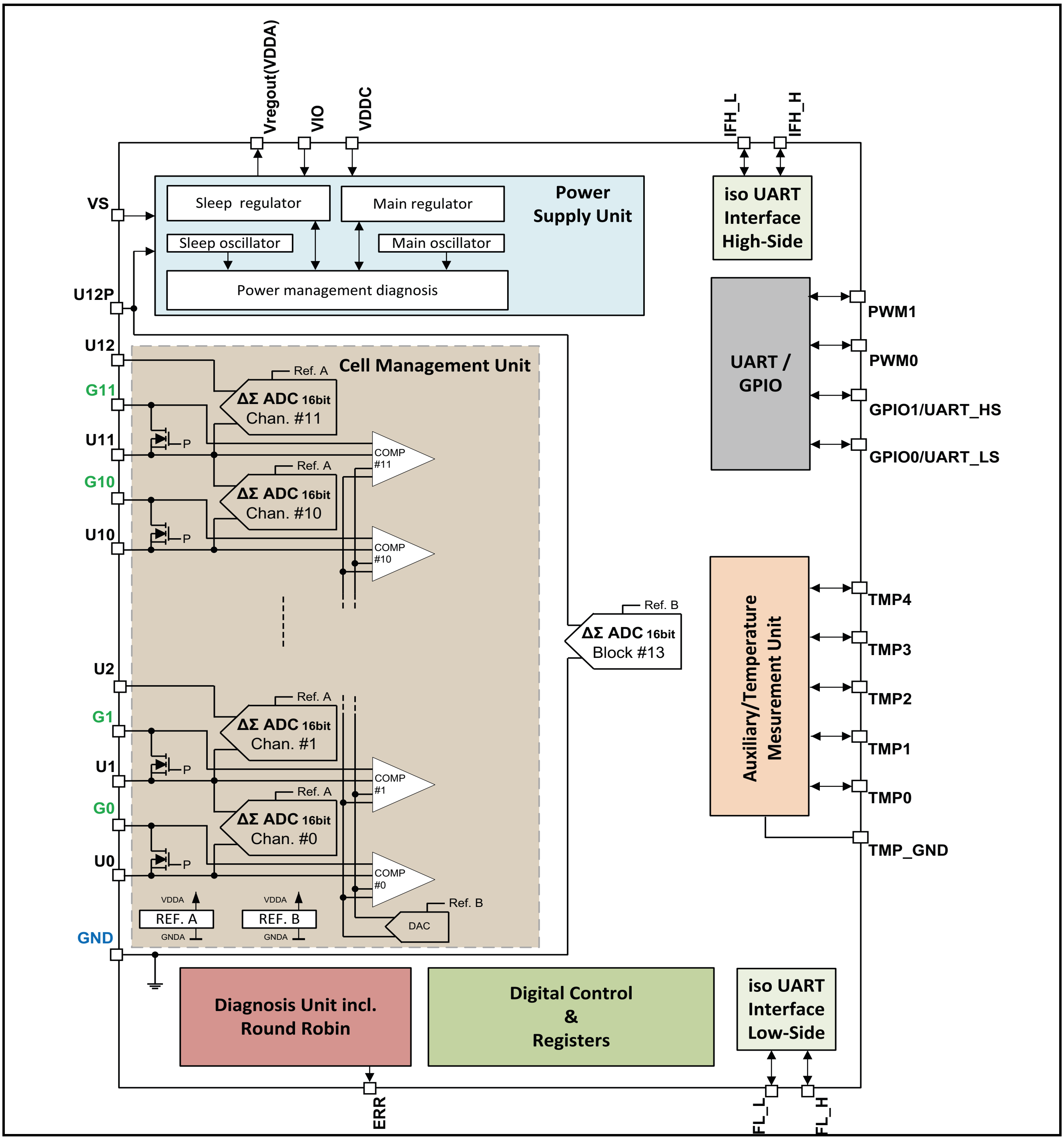


Figure 1 TLE9012AQU block diagram

2 Pin configuration

2.1 Pin assignment

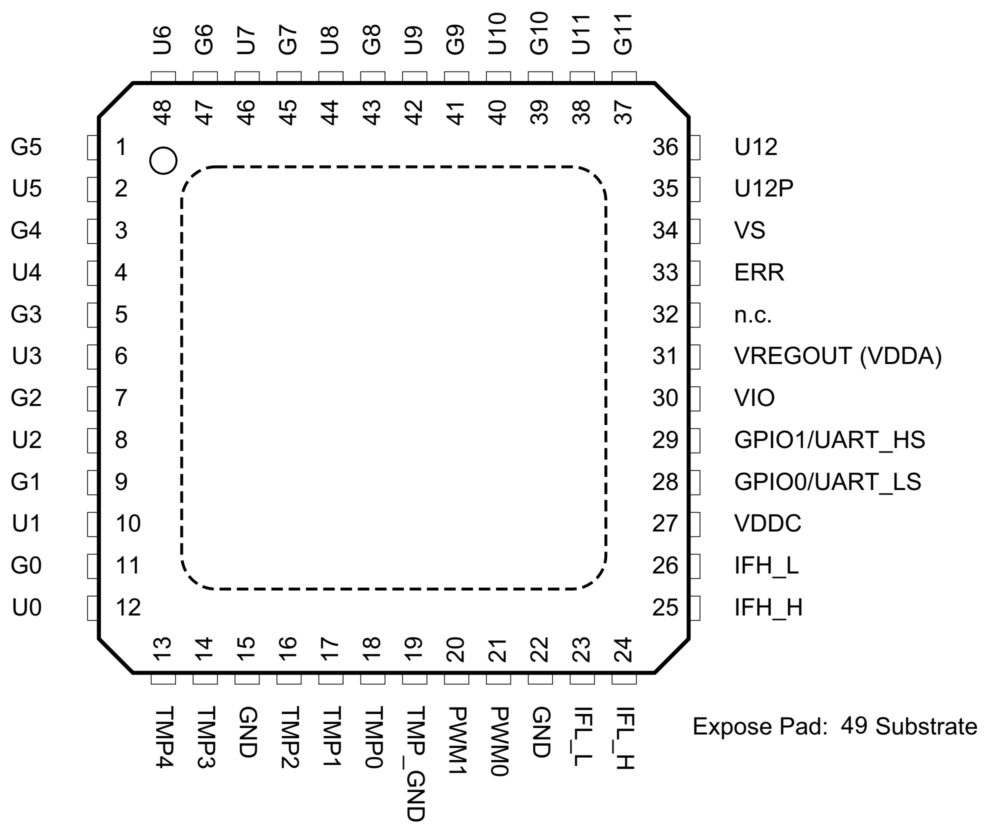


Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin assignment

Pin	Symbol	Function
1	G5	Cell balance control channel 5, input of SCVS
2	U5	Cell voltage measurement channel 5 negative terminal (positive terminal of cell 4)
3	G4	Cell balance control channel 4, input of SCVC
4	U4	Cell voltage measurement channel 4 negative terminal (positive terminal of cell 3)
5	G3	Cell balance control channel 3, input of SCVC
6	U3	Cell voltage measurement channel 3 negative terminal (positive terminal of cell 2)
7	G2	Cell balance control channel 2, input of SCVC
8	U2	Cell voltage measurement channel 2 negative terminal (positive terminal of cell 1)
9	G1	Cell balance control channel 1, input of SCVC
10	U1	Cell voltage measurement channel 1 negative terminal (positive terminal of cell 0)
11	G0	Cell balance control channel 0, input of SCVC
12	U0	Cell voltage measurement channel 0 negative terminal (same potential as local GND)
13	TMP4	Temperature sensor 4; If not used, please connect pin to GND. If TMP4 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin.
14	TMP3	Temperature sensor 3; If not used, please connect pin to GND. If TMP3 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin.
15	GND	Local GND of CSC (Cell Supervision Circuit) device
16	TMP2	Temperature sensor 2; If not used, please connect pin to GND. If TMP2 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin.
17	TMP1	Temperature sensor 1; If not used, please connect pin to GND. If TMP1 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin.
18	TMP0	Temperature sensor 0; If not used, please connect pin to GND. If TMP0 is disabled, the pin can be used as 0 .. 2 V auxiliary ADC miscellaneous pin.
19	TMP_GND	Temperature sensor reference. This pin can be connected to local GND.
20	PWM1	PWM output channel 1; This pin has also a general purpose input/output function; If not used, please connect pin to GND.
21	PWM0	PWM output channel 0; This pin has also a general purpose input/output function; If not used, please connect pin to GND.
22	GND	Local GND of CSC device (Cell Supervision Circuit)
23	IFL_L	Lower Communication Bus (iso UART) L pin
24	IFL_H	Lower Communication Bus (iso UART) H pin
25	IFH_H	Upper Communication Bus (iso UART) H pin
26	IFH_L	Upper Communication Bus (iso UART) L pin
27	VDDC	Buffer capacitor pin for internal Communication Bus (iso UART) supply
28	GPIO0/ UART_LS	General purpose input/output channel 0. This pin has also the function of UART_LS; If not used, please connect pin to GND.

Table 1 Pin assignment

Pin	Symbol	Function
29	GPIO1/ UART_HS	General purpose input/output channel 1. This pin has also the function of UART_HS; if not used, please connect pin to GND.
30	VIO	Supply for GPIO interface.
31	Vregout	Output pin of the internal regulator.
32	n.c.	Not connected; this pin shall be connected to GND.
33	ERR	Erroroutput to microcontroller; open drain PMOS connected to VS. If not used, please leave pin open.
34	VS	Supply pin of internal regulator Vregout.
35	U12P	Positive supply pin; connect to positive terminal of topmost cell in block; supply of the sleep regulator.
36	U12	Cell voltage measurement channel 11 positive terminal (most upper cell in the block)
37	G11	Cell balance control channel 11, input of SCVC
38	U11	Cell voltage measurement channel 11 negative terminal (positive terminal of cell 10)
39	G10	Cell balance control channel 10, input of SCVC
40	U10	Cell voltage measurement channel 10 negative terminal (positive terminal of cell 9)
41	G9	Cell balance control channel 9, input of SCVC
42	U9	Cell voltage measurement channel 9 negative terminal (positive terminal of cell 8)
43	G8	Cell balance control channel 8, input of SCVC
44	U8	Cell voltage measurement channel 8 negative terminal (positive terminal of cell 7)
45	G7	Cell balance control channel 7, input of SCVC
46	U7	Cell voltage measurement channel 7 negative terminal (positive terminal of cell 6)
47	G6	Cell balance control channel 6, input of SCVC
48	U6	Cell voltage measurement channel 6 negative terminal (positive terminal of cell 5)
49	EPAD	Cooling tab; should be connected to GND externally.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS	V_{VS}	-0.3	–	75	V	–	
Supply voltage U12P	V_{U12P}	-0.3	–	75	V	–	
Supply voltage VIO	V_{VIO}	-0.3	–	5.5	V	–	
Supply voltage VS rel.	V_{VS}	V_{regout}- 0.3	–	–	–	–	
Regulator output VREGOUT	V_{regout}	-0.3	–	3.6	V	–	
Regulator output VDDC	V_{VDDC}	-0.3	–	3.6	V	–	
Communication Bus (iso UART) interface IFH_x	V_{IFH_L} V_{IFH_H}	-3	–	5.5	V	[2)]BCI test max. 300 mA injected via twisted pair cable onto iso UART interface (max. pin current 150 mA)	
Communication Bus (iso UART) interface IFL_x	V_{IFL_L} V_{IFL_H}	-3	–	5.5	V		
Cell sense input voltage abs. Un	V_{Un}	-0.3	–	75	V	0 ≤ n ≤ 12	
Cell balancing pin abs. Gn	V_{Gn}	-0.3	–	75	V	0 ≤ n ≤ 11	
Cell sense input voltages rel. Un	V_{Un}	V_{Un-1}- x	–	V_{Un-1}+ 5.5	V	1 ≤ n ≤ 12; x= -0.0016*T_j + 0.54; e.g.: x=0.5@T_j =25°C	
Cell balancing pins rel. Gn	V_{Gn}	V_{Un}- 0.3	–	V_{Un+1}+ 0.3	V	0 ≤ n ≤ 11	
Temperature sensor input voltages abs. TMPn	V_{TMPn}	-0.3	–	2.75	V	0 ≤ n ≤ 4	
Temperature sensor input voltages rel. TMPn	V_{TMPn}	-0.3	–	V_{regout}+0.3	V		
Temperature sensor input voltages abs. TMP_GND	V_{TMP_GND}	-0.3	–	2.75	V	–	
Temperature sensor input voltages rel. TMP_GND	V_{TMP_GND}	-0.3	–	V_{regout}+0.3	V	–	

Table 2 Absolute maximum ratings[1] (cont'd)

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
General purpose I/O voltages abs. GPIOn	V_{GPIOn}	-0.3	–	5.5	V	0 ≤ n ≤ 1	
General purpose I/O voltages rel. GPIOn	V_{GPIOn}	-0.3	–	V_{VIO}+ 0.3	V		
Pulse width modulation I/O voltages abs. PWMn	V_{PWMn}	-0.3	–	5.5	V	0 ≤ n ≤ 1	
Pulse width modulation I/O voltages rel. PWMn	V_{PWMn}	-0.3	–	V_{VIO}+ 0.3	V		
Open drain output pin abs. ERR	V_{ERR}	-0.3	–	75	V	–	
Open drain output pin rel. ERR	V_{ERR}	-0.3	–	V_{VS}+ 0.3	V	–	
Ground pin GND	V_{GND}	0	–	0	V	Absolute GND	
Temperatures							
Junction temperature Tj	T_j	-40	–	150	°C	–	
Storage temperature Tstg	T_{stg}	-55	–	150	°C	–	
ESD robustness							
ESD robustness 2 kV	V_{ESD}	-2	–	2	kV	HBM[3]; all pins	
ESD robustness 4 kV	V_{ESD}	-4	–	4	kV	HBM[3]; Robustness vs. GND for pins: VS, U12P, Un, TMPn, TMP_GND, AUX_MISn, IFH_x, IFL_x, Gn	
ESD robustness CDM 500 V	V_{ESD}	-500	–	500	V	CDM[4]; all pins	
ESD robustness CDM 750 V	V_{ESD_Corner}	-750	–	750	V	CDM[4]; corner pins	

1) Not subject to production test, specified by design.
2) Positive and negative transients with a maximum duration of 100ns allowed between +/- 8 V; This should simulate ESD events; however, during normal and steady state condition voltage on these pins must stay inside the maximum ratings specified.
3) ESD robustness, according to Human Body Model "HBM" ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)
4) ESD robustness, according to Charged Device Model "CDM" JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical characteristics table.

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage VS	V_{VS}	4.75	–	60	V	when using the internal regulator	
Supply voltage U12P	V_{U12P}	4.75	–	60	V	–	
Supply voltage VIO	V_{VIO}	3	–	5.5	V	–	

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case RthJC	R_{thJC}	–	6	-	K/W	[1]	
Junction to ambient RthJA	R_{thJA}	–	30	-	K/W	[1][2]	

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.
Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org.

4 Power supply

4.1 Functional description

The TLE9012AQU has an internal power supply to be able to work completely independent by using the power stored in the cells which it monitors.

4.2 Power supply description

The following table contains a description of the power supply pins of the TLE9012AQU.

Table 5 Power supply pins

Pin name	Function
VS	VS is the main supply pin. This pin is the input for the internal regulator that is intended to supply the device in normal mode. It should be connected to the highest voltage in the module (usually the positive pole of the top cell). Supplying this pin is necessary to function the device.
U12P	U12P is the sense pin for the block voltage measurement (BVM); additionally this pin is the input supply pin for the sleep regulator which supplies the wake-up structures. The built-in sleep regulator powers the detection of incoming iso UART and UART wake-up signals in sleep mode which will then trigger the start-up procedure. It should be connected to the highest voltage in the module. Supplying this pin is necessary to function the device.
Vregout (VDDA)	This pin is the output of the internal regulator. Usually this voltage can be used to drive the GPIOs for communication with other devices on board. Please connect this pin to a buffer capacitor.
VIO	This pin is the supply for the GPIOs. It can be connected either to Vregout or to the output of an external voltage regulator. The voltage available on this pin, will define the GPIO logic output levels as well as the thresholds of the GPIO logic inputs.
VDDC	VDDC is the output of the internal regulator used for the iso UART communication interface. This pin is used for buffering of the regulator. Please connect this pin to a buffer capacitor to ensure proper and robust communication.
GND	This is the main reference for the TLE9012AQU on the board.

The cell partitioning can be configured in the **PART_CONFIG** register with the given constraint of starting from the most upper cell (CELL_11). Please note: Only cells activated in **PART_CONFIG** are being measured and checked in the round robin scheme (see also **Chapter 8.3.1**).

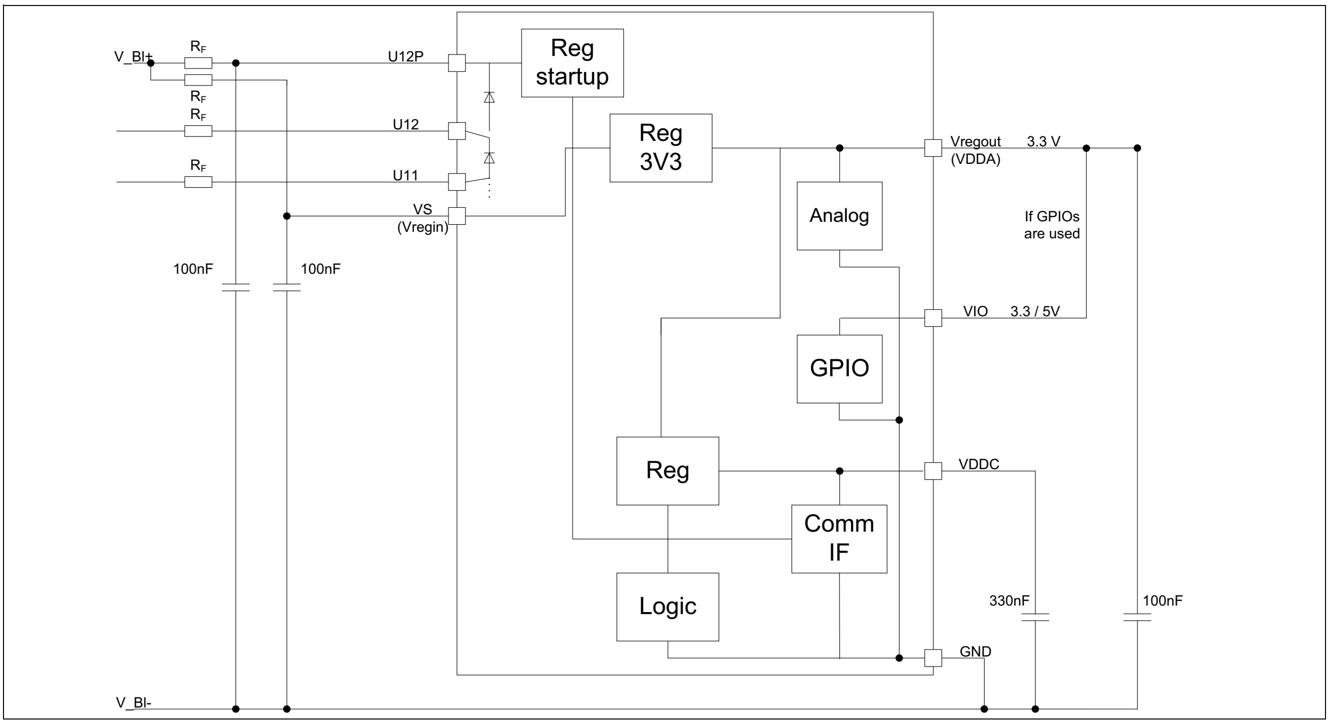


Figure 3 Typical power supply configuration using the internal voltage regulator

4.3 Using an external voltage regulator for the UART/GPIO unit

It is also possible to use an external voltage regulator. This might be desired to have common I/O voltage levels with the host controller in case of systems where no transceiver IC is used and communication is happening directly via UART/GPIO (non-HV application like 12 V/48 V).

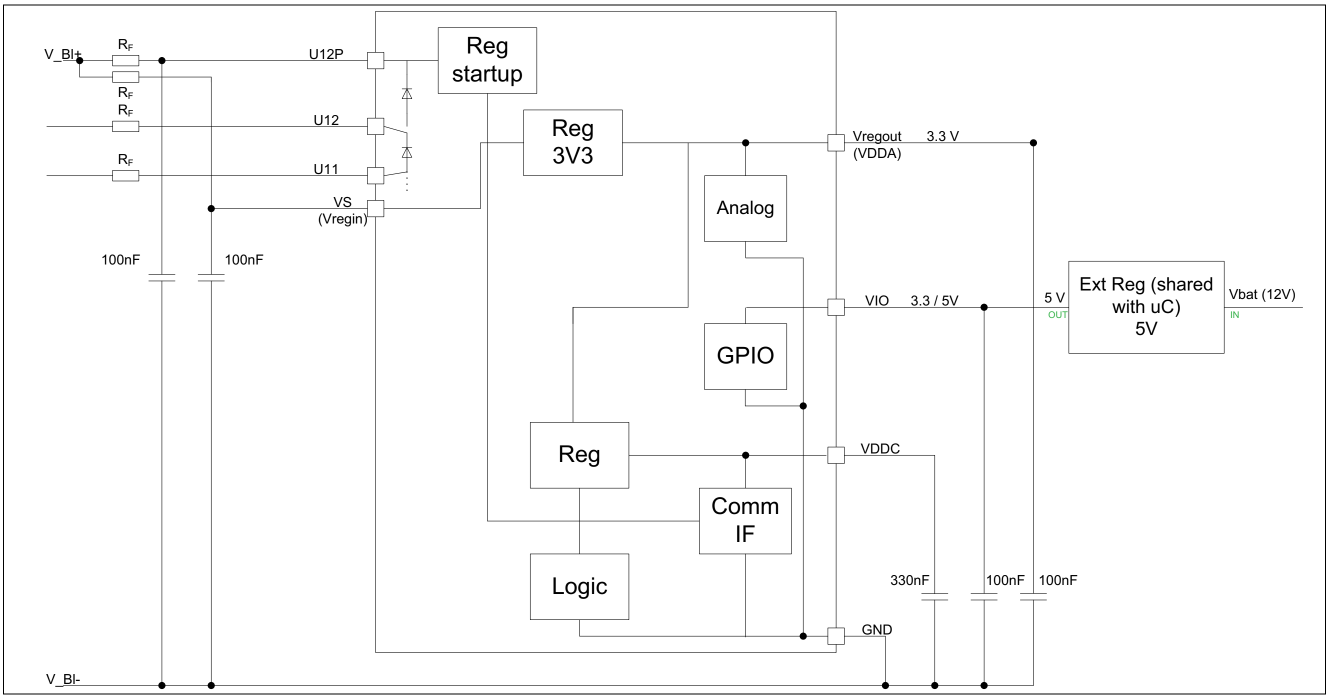


Figure 4 System using an external voltage regulator (non-transceiver application)

4.4 Wake-up and sleep mode

The TLE9012AQU is designed to be continuously connected to a battery. Therefore, the physical connection to the cells which powers the device is expected to happen only once in a lifetime. After receiving power on U12P and VS, the part will go into sleep mode and will be monitoring the communication interfaces for a wake-up sequence.

In order to activate the TLE9012AQU a wake-up sequence as described in **Chapter 8.2.2** has to be sent via either the iso UART port or the UART interface.

A watchdog is implemented that has to be triggered by regular iso UART/UART communication in order to keep the TLE9012AQU in normal mode. The watchdog timer is programmable (register **WDOG_CNT**). The device will revert to sleep mode automatically as soon as the watchdog has timed out.

Additionally the TLE9012AQU includes the option to send the device directly to sleep mode, this can be performed by setting the PD bit-field in the **OP_MODE** register.

4.5 Power supply monitoring

To ensure the correct function of the TLE9012AQU, the device is equipped with an internal monitoring unit for the different internal voltages as well as other supply functions. If important supplies go below levels to ensure correct functionality, the IC will enter sleep mode. The fault bit UV_SLEEP in the **GEN_DIAG** register indicates sleep mode due to a supply level outside the limits.

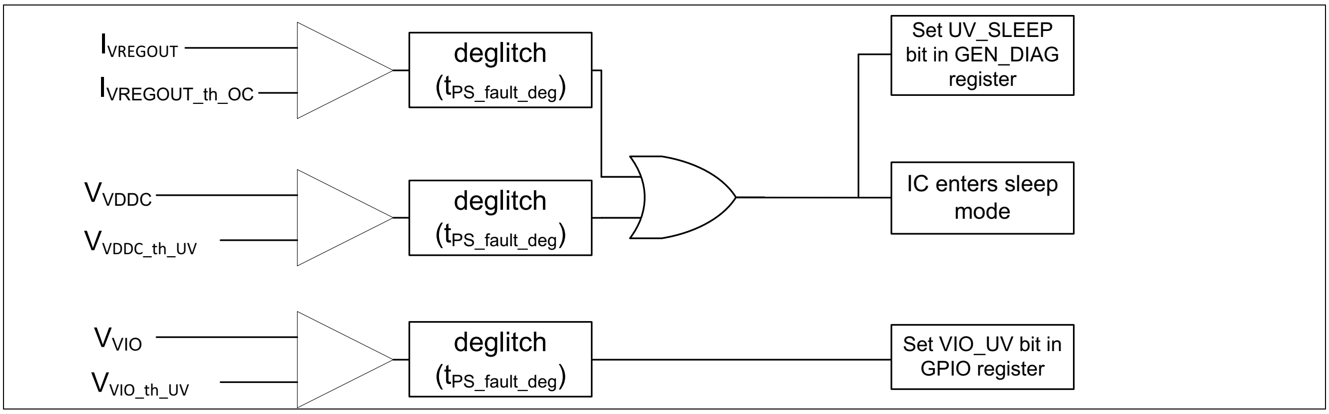


Figure 5 HW monitoring unit

4.6 Electrical characteristics power supply

Table 6 Electrical characteristics power supply

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal regulators							
internal regulator output voltage VREGOUT	$V_{Vregout}$	3	3.45	3.6	V	–	
Overcurrent threshold VREGOUT	$I_{VREGOUT\_th\_OC}$	31	40	60	mA	–	
Undervoltage threshold falling VIO	$V_{VIO\_th\_UV\_fall}$	2.2	–	2.76	V	–	
Undervoltage threshold rising VIO	$V_{VIO\_th\_UV\_rise}$	2.24	–	2.8	V	–	
VIO undervoltage hysteresis VIO	$V_{VIO\_th\_UV\_hys}$	40	100	160	mV	–	
Output voltage VDDC	V_{VDDC}	2.42	2.5	2.75	V	–	
Undervoltage threshold VDDC	$V_{VDDC\_th\_UV}$	2.15	–	2.42	V	–	
Undervoltage threshold hysteresis VDDC	$V_{VDDC\_th\_UV\_hys}$	80	100	140	mV	–	
Power supply fault deglitch time	$t_{PS\_fault\_deg}$	8	15	24	µs	1)	
Supply currents							
Sleep mode current U12P	I_{U12P_sleep}	0	3	4.9	µA	T_j = 25°C;	
Sleep mode leakage current VS	I_{VS_sleep}	-1	–	1	µA	-40°C ≤ T_j ≤ 85°C	
Idle current U12P	I_{U12P_idle}	–	2.5	10	µA	IC in idle mode (no sleep mode), but no measurement or communication. VIO connected to Vregout	
Idle current VS	I_{VS_idle}	–	4.7	9.2	mA		
Current consumption during GPIO communication VIO	I_{VIO_comm}	–	–	5	mA	depending on load on GPIO	
Current consumption during CVM & BVM VS	I_{VS_meas}	–	21	25	mA	Parallel measurement of all cells + block voltage measurement. VIO connected to Vregout. Incl. idle consumption I_{VS_idle}	

Table 6 Electrical characteristics power supply (cont'd)

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption during round robin scheme running VS	I_{VS_RR}	–	9	26	mA	Only during round robin scheme is running. VIO connected to Vregout. Incl. idle consumption I_{VS_idle}	
Current consumption during communication VS	I_{VS_comm}	–	6.5	10.8	mA	Valid for GPIO or iso UART communication. Current to charge-up external interface components not included. Incl. idle consumption I_{VS_idle}	
Current consumption during communication only for external iso UART interface components VS	$I_{VS\_comm\_ext}$	–	–	6	mA	[1] $C_{isoUART\_ser}$ = 1 nF $BR_{isoUART}$ = 2 MBits $R_{isoUART\_ser}$ = 39 Ω This consumption needs to be added to I_{VS_comm}.	

1) Not subject to production test, specified by design.

5 Cell management unit

5.1 Overview

The TLE9012AQU provides the tools required for managing up to 12 cells stacked in series. It provides the following functions:

- Accurate voltage measurement
- Configurable OV/UV comparators
- Passive cell balancing
- Cell diagnosis

Additionally, other central functions take care of providing the tools to manage the module as a whole. More information can be found in **Chapter 8**.

Each cell has the same structure as shown in **Figure 6**. Additionally **Figure 6** shows how the unit is connected to the external structure. The cell voltage measurement unit contains a 16-Bit SD-ADC. It is recommend to use similar filter characteristics for the Ux+1 - Ux and Gx - Ux input filters to support a synchronous OV/UV check with both units (comparator & SD-ADC).

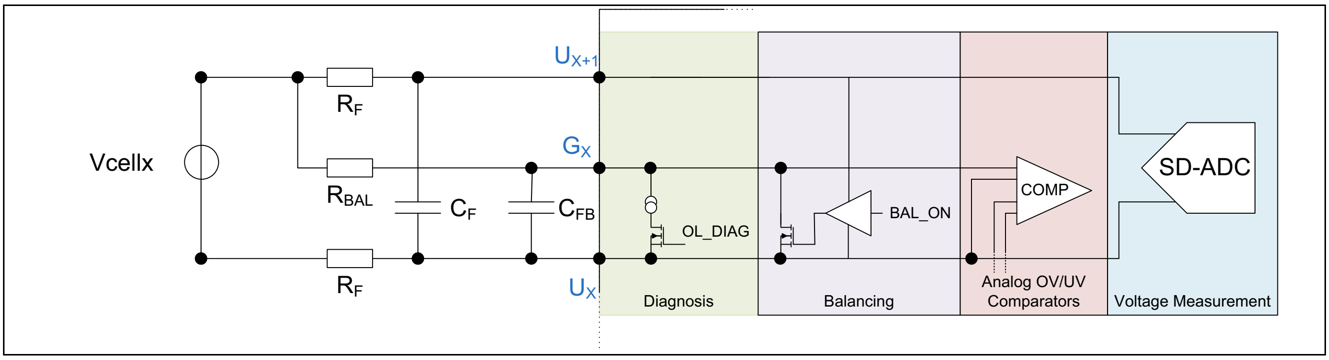


Figure 6 Example of internal structure for 1 cell monitoring hardware

5.2 Accurate cell voltage measurement

The exact voltage of each cell is necessary to estimate parameters like state of charge of the battery. The TLE9012AQU provides the necessary ADCs to accurately measure the voltage of each cell.

The voltage measurement path consists of 12 individual 16 bit delta sigma analog to digital converters, one for each cell. The use of separate ADC units enables the conversion of all 12 cell voltages simultaneously. The offset and gain errors of the converters are trimmed individually.

The AD conversion for all cells are initiated by writing the CVM_START bit-field in the **MEAS_CTRL** register. The IC has the option to enable a programmable timer t_{CVM_del}. After receiving a command, which initiates the start of a cell voltage measurement, this timer delays the start of the cell voltage measurement. The IC's cell voltage measurement ADC samples with f_s and averages the cell voltage measurement result of each cell for the duration of t_{CVM}. If CVM is started, during the t_{CVM}, the measurement result is reset. At the end of the conversion, the CVM_START bit-field is automatically cleared and the RESULT is available. This bit-field can be monitored by reading the respective register. The result registers can be accessed by reading the RESULT bit-field in the **CVM_0** – **CVM_11** registers.

Different measurement modes can be selected (this mode will affect all channels at once):

Table 7 Voltage measurement modes

Mode (CVM_BIT_WIDTH [2:0])	Result resolution	Measuring time (t_{CVM})	ADC bandwidth (cut-off frequency)[1]	FSR
110	16 Bit	~4.68 ms	70 Hz	5 V
101	15 Bit	~2.34 ms	140 Hz	
100	14 Bit	~1.17 ms	280 Hz	
011	13 Bit	~585.1 µs	560 Hz	
010	12 Bit	~292.6 µs	1.12 kHz	
001	11 Bit	~146.3 µs	2.24 kHz	
000	10 Bit	~73.1 µs	4.48 kHz	

1) The given cut-off frequencies are only theoretical calculations assuming 1st order averaging filter and should be used only for orientation purposes. They will neither be tested nor guaranteed.

The result is always an unsigned value. In case the result is less than 16 bits, the remaining LSBs will be set to “0”.The equation to convert the value read from the RESULT bit-fields in the **CVM_0** – **CVM_11** registers to the cell voltage is:

Cell voltage [mV] = (FSR*1000 [mV] / (2^16)) * RESULT (5.1)

The voltage measurement unit averages the signal automatically over the entire measurement time. So the voltage measurement unit of each cell provides a built-in digital filtering for the cell voltage measurement. The reference for the primary cell voltage measurement ADCs is the internal voltage reference A.

Please note: As soon as a cell voltage measurement start command is received, any ongoing round robin schedule will be cancelled and the measurement will start after t_{CVM_del}. After the measurement is finished, the RR task will be restarted. For more information please refer to **Chapter 8.3**.

5.2.1 Electrical characteristics

Table 8 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Cell sense inputs							
CVM differential input current Un	I_{Un_CVM}	18	25	32	µA	during CVM V_{CVM}=5 V 0 ≤ n ≤ 12 typ. value I_{Un_CVM} = V_{CVM} / 200 kΩ	
Input leakage current Un	I_{Un_leak}	-1.0	0	1.0	µA	0 ≤ n ≤ 12 in sleep mode & in idle mode	
Timing							
CVM propagation delay within IC	t_{CVM_prop}	0	–	10	µs	[1]Propagation delay between complete arrival of CVM start message and the actual start of the CVM	
CVM start delay timer resolution	$t_{CVM\_del\_LSB}$	35.1	36.6	38.1	µs	[1]	
CVM start delay timer maximum interval	$t_{CVM\_del\_max}$	1.09	1.13	1.18	ms	[1]	
Primary voltage measurement							
CVM input range	V_{CVM}	0	–	5	V	[1] Measuring V_{cell} = V_{Un+1} - V_{Un}; 0 ≤ n ≤ 11	
CVM resolution	V_{CVM_LSB}	–	FSR/2^m	–	V	[1]10 ≤ m ≤ 16; FSR = 5 V	
CVM ADC sampling frequency	$f_{s\_CVM\_ADC}$	13.44	14	14.56	MHz	[1]	
CVM time	t_{CVM}	–	2^m/ $f_{s\_CVM\_ADC}$	–	s	[1] 10 ≤ m ≤ 16	
Maximum CVM time deviation between channels within IC	Dev_{CVM_IC}	-0.5	–	0.5	%	[1]deviation between CVM time t_{CVM} within one IC	
Maximum CVM time deviation across ICs	Dev_{CVM_chain}	-4	–	4	%	[1]deviation between CVM time t_{CVM} over all ICs	

Table 8 Electrical characteristics (cont'd)

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CVM relative accuracy - initial[2)4)]	$CVM_{ERR\_relative}$	-0.9	–	0.9	mV	16 bit mode V_{cell} = 4.3 V T_j = 25°C ±3 sigma distribution within abs. min/max limits	
CVM accuracy - initial[2)4)]	CVM_{ERR}	-2	–	2	mV	14 - 16 bit mode 2.7 V ≤ V_{cell} ≤ 4.3 V T_j = 25°C ±3 sigma distribution within abs. min/max limits Accuracy at tester in backend	
CVM accuracy EOL[3)4)]	CVM_{ERR_EOL}	-5.8	–	5.8	mV	14 -16 bit mode 2.7 V ≤ V_{cell} ≤ 4.3 V -40°C ≤ T_j ≤ 125°C ±3 sigma distribution within abs. min/max limits	
CVM accuracy EoL - 10 Bit mode[1)3)4)]	$CVM_{ERR\_EoL\_10Bit}$	-25	–	25	mV	10 bit mode 0.05 V ≤ V_{cell} ≤ 4.8 V -40°C ≤ T_j ≤ 150°C ±3 sigma distribution within abs. min/max limits	

1) Not subject to production test, specified by design.
2) Initial accuracy verified by Infineon backend.
3) End-of-Life; according to AEC-Q100 Grade 1 Rev. H automotive qualification.
4) Parameters are verified during the following conditions: no NTC measurement; no iso UART communication; no AUX measurement

5.3 Configurable analog overvoltage/undervoltage (OV/UV) comparators

Additionally to the primary measurement path with the SD-ADC the TLE9012AQU includes also a separate analog OV/UV check (see also **Figure 6**) via comparators and a Digital-Analog-Converter (DAC). The threshold values of the comparators are configurable. Furthermore the comparator logic is averaging its checks over a time period of t_{comp}. Similar to the digital comparators used in the round robin scheme to check for OV/UV based on the primary measurement, the analog comparators check the voltage at Gx-Ux against the OV/UV thresholds stored in register **OL_OV_THR** and **OL_UV_THR** as secondary redundant OV/UV path.

This analog unit is connected to the Gx pin which also means the external filter structure is different from the primary path. The approach of the different pins avoids having potential faults violating both OV/UV check paths in the same way.

The analog OV/UV check against the thresholds happens synchronously to the digital check in every round robin scheme. Please see also round robin scheme description in **Chapter 8.3.1**.

5.3.1 Electrical characteristics

Table 9 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Cell Gx sense inputs							
Comparator differential input current Gn	I_{Gn_comp}	–	7	10	µA	$0 \le n \le 11$ during comparator check in round robin[1)]	
Analog overvoltage/undervoltage comparators							
Comparator input range	V_{Comp}	0	–	5	V	[1)] Measuring $V_{cell} = V_{Gn} - V_{Un}$ $0 \le n \le 11$	
Comparator resolution	V_{Comp_LSB}	–	FSR/2^{10}	–	V	[1)]FSR = 5 V	
Comparator accuracy	$COMP_{ERR}$	-50	–	50	mV	1 V < V_{cell} < 4.7 V -40°C ≤ T_j ≤ 150°C ±3 sigma distribution within abs. min/max limits	
Relative comparator accuracy	$COMP_{ERR\_limited}$	-30	–	30	mV	V_{cell} = 3.6 V -40°C ≤ T_j ≤ 25°C ±3 sigma distribution within abs. min/max limits	
Comparator sampling frequency	f_{COMP}	1	–	–	MHz	[1)]	
Comparator checking time	t_{comp}	–	$2^{10}/ f_{s\_CVM\_ADC}$	–	µs	[1)]	

1) Not subject to production test, specified by design.

5.4 Cell balancing

The TLE9012AQU IC supports passive balancing of up to 12 cells connected in series. The device contains 12 built-in MOSFET switches which can be used together with external resistors to dissipate each cell's energy, see **Figure 7**.

Balancing can be activated for each cell independently and in any combination, including all 12 channels simultaneously. The internal switches can support balancing currents of I_{BAL}. For balancing currents higher than I_{BAL}, external P channel MOSFET transistors can be used as shown in **Figure 9**.

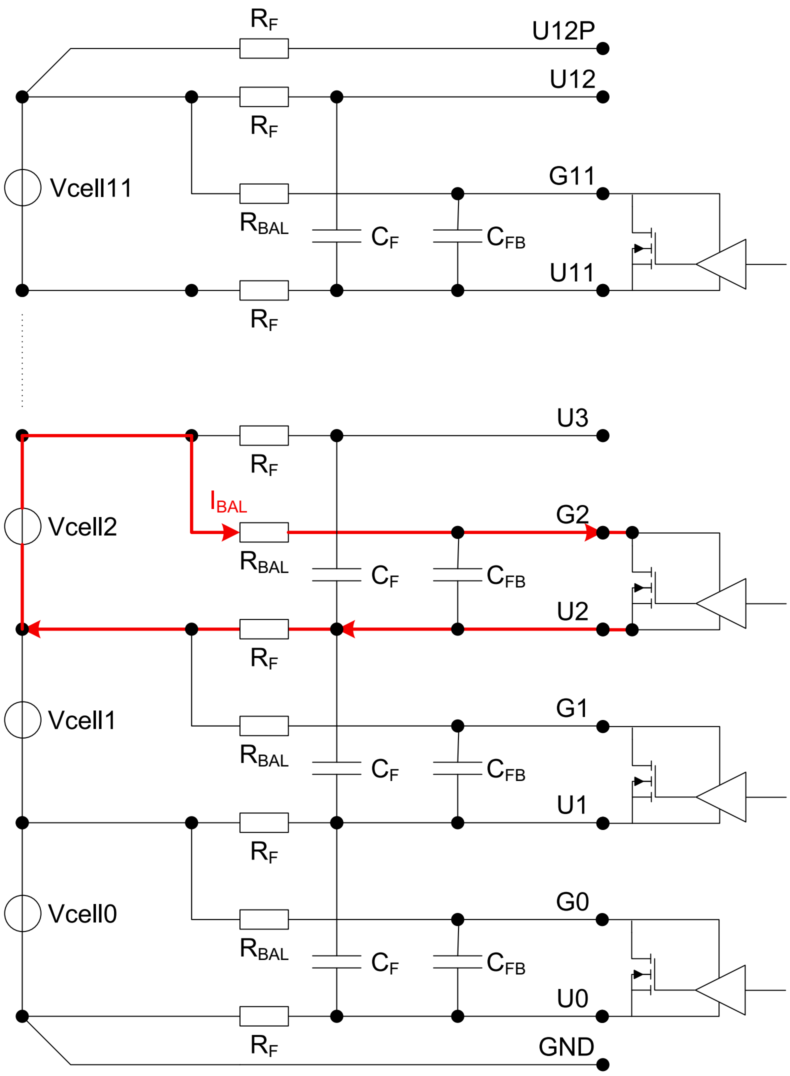


Figure 7 Passive balancing example of Cell2

Passive balancing is initiated by the host microcontroller by writing to the **BAL_SETTINGS** register via the UART or the iso UART interface. Writing a "1" to the ON_1 bit-field, for instance, will turn on the passive balancing switch connected to the G1 pin and the current will start flowing. The switch remains on until a "0" is written to the ON_1 bit-field, the IC enters the sleep state or a failure occurs (see **Chapter 8.4**).

To avoid measurement errors due to passive balancing current, the passive balancing switches can be deactivated automatically during the conversion by setting the PBOFF bit-field in the **MEAS_CTRL** register.

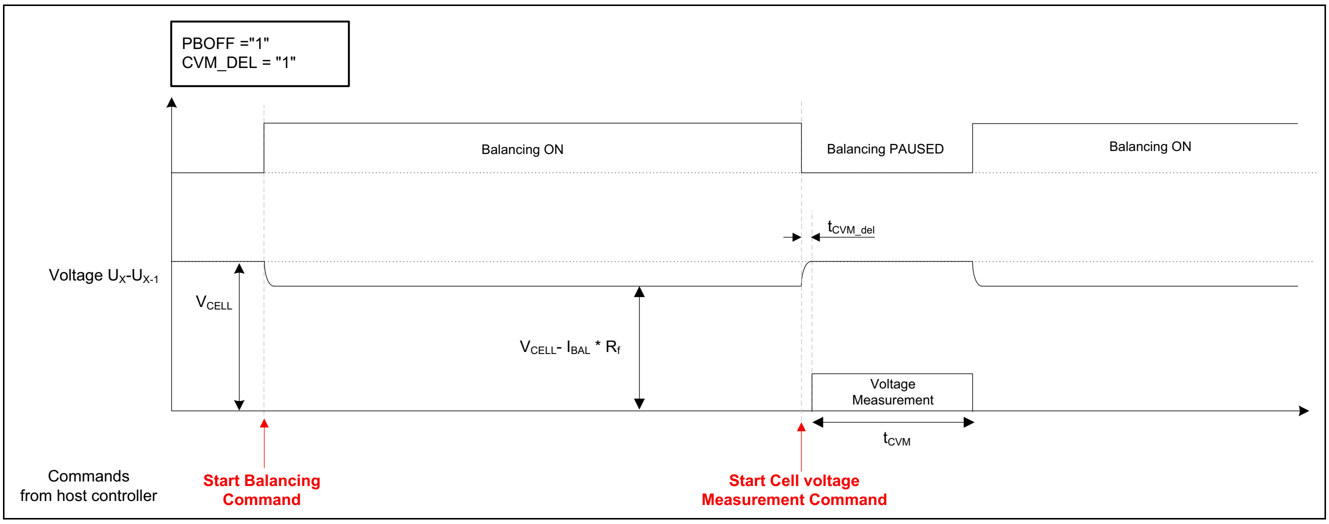


Figure 8 Timing diagram for balancing & cell voltage measurement with t_{CVM_del} (PBOFF Bit = 1)

A programmable settling time t_{CVM_del} (bit-field CVM_DEL) can be programmed in the **MEAS_CTRL** register; this delays the start of the measurement after the passive balancing transistors are disabled. Please note that for a global synchronization the start of the measurement is always delayed by t_{CVM_del} no matter whether balancing was happening or not. Please see **Figure 8** for more details.

The TLE9012AQU includes an extended watchdog mode. In this mode, the watchdog LSB step interval changes to $t_{WD\_EXT\_LSB}$. With this extended timing, there is a maximum watchdog duration of $t_{WD\_EXT\_max}$.

During the round robin (RR) measurements, the passive balancing switches will be deactivated to avoid false detections during the round robin checks. After the RR scheme is done, the balancing will continue automatically (this is true independent of the PBOFF state). If balancing was activated before the RR starts, the RR will perform a balancing over- and undercurrent check. The balancing fault flag (one for OC and one for UC) is set in the **GEN_DIAG** register if an overcurrent or undercurrent occurs on any cell.

The balancing function will be deactivated if one of the following errors is detected. The errors are indicated in **GEN_DIAG**.

- Balancing error overcurrent, bit-field: BAL_ERR_OC. Balancing only for affected cell(s) deactivated.
- Balancing error undercurrent, bit-field: BAL_ERR_UC. Balancing only for affected cell(s) deactivated.
- Overvoltage error, bit-field: CELL_OV. Balancing only for affected cell(s) deactivated.
- Undervoltage error, bit-field: CELL_UV. Balancing only for affected cell(s) deactivated.
- Internal temperature sensor over temperature error, bit-field: INT_OT. Balancing for all cells deactivated.
- External temperature sensor measurement error, bit-field: EXT_OT. Balancing for all cells deactivated.
- Configuration register CRC error, bit-field: REG_CRC_ERR. Balancing for all cells deactivated.
- Internal IC error, bit-field: INT_IC_ERR. Balancing for all cells deactivated.
- Open load error, bit-field: OL_ERR. Balancing for all cells deactivated.
- ADC error, bit-field: ADC_ERR. Balancing for all cells deactivated.

5.4.1 Using external balancing switches

If the necessary current is higher than the maximum allowed internal balancing current, an external P-MOS can be used to increase the balancing current further. Assuming a proper dimensioning of the external components, all the functions remain unchanged. Please see **Figure 9** for more details. The Roc/uc resistor is needed to support the balancing overcurrent and undercurrent diagnosis also for the external switch (see also **Chapter 5.5.2**).

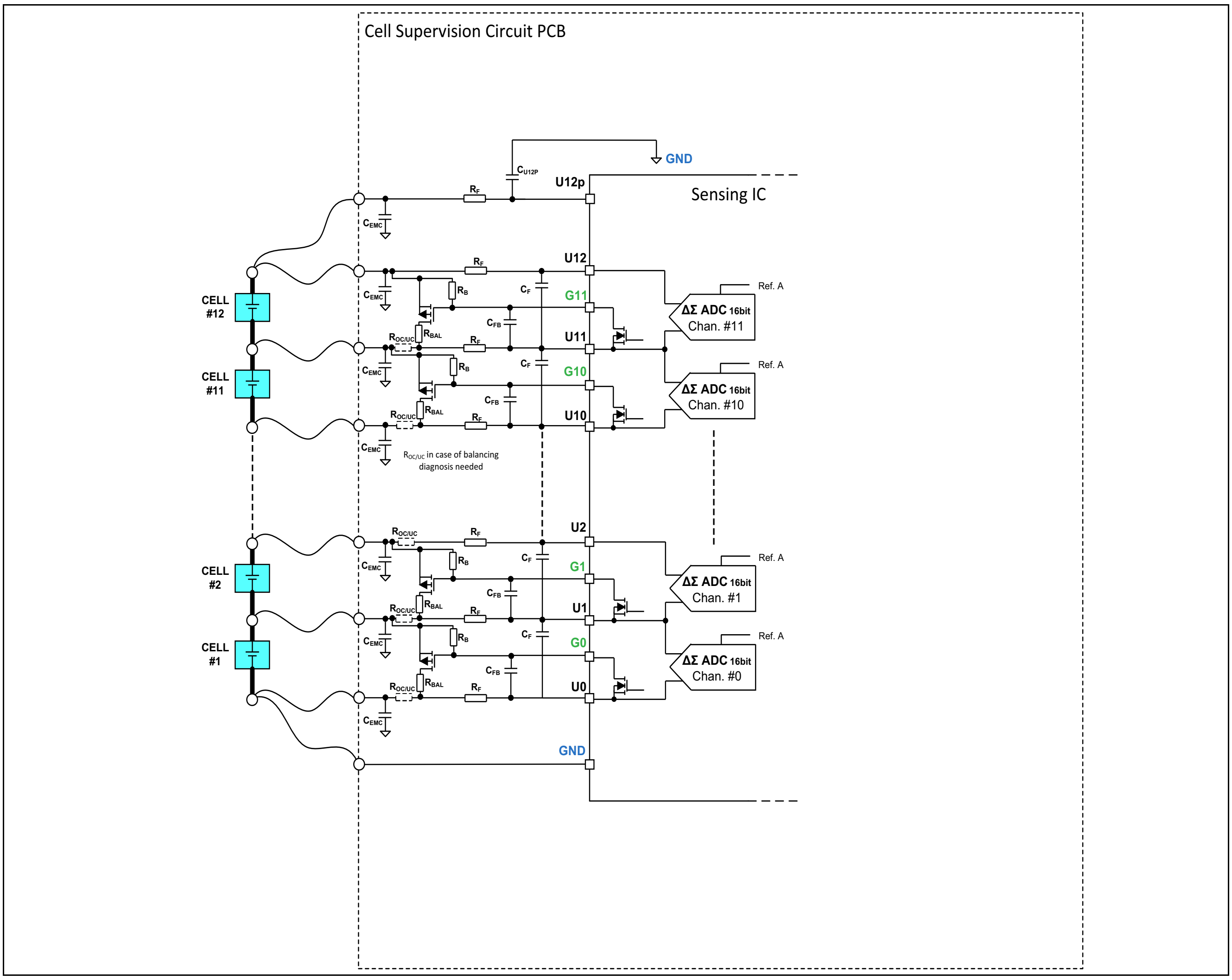


Figure 9 Diagram of the cell unit using external balancing switches

5.4.2 Electrical characteristics

Table 10 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input leakage current Gn	I_{Gn_leak}	-1.0	0	1.0	µA	$0 \leq n \leq 11$ in sleep & idle mode	
Balancing switch on-state resistance	R_{BAL_DSON}	1.5	2.7	5.3	Ω	$1.5V \leq V_{Cell}$	

Table 10 Electrical characteristics (cont'd)

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Balancing current	I_{BAL}	–	–	150	mA	1.5V ≤ V_{Cell}	
Balancing overcurrent detection time	$t_{BAL\_OC\_DET}$	–	–	t_{RR_max}	ms	[1]Time till a balancing over current must be detected. Equivalent to max. round robin cycle time (when the error counter is disabled which is the default value, M_NR_ERR_BAL_OC = 1)	

1) Not subject to production test, specified by design.

5.5 Cell diagnosis

The cell diagnosis are part of the round robin (see **Chapter 8.3**). The TLE9012AQU provides the necessary tools to detect a possible open load/wire of the different cell connections.

In order to help the diagnosis, the following hardware is available:

- 12x cell-specific Sigma-Delta ADC (CVM)
- 1x block measurement ADC (BVM)
- 12x diagnosis current sink (1x for each cell)

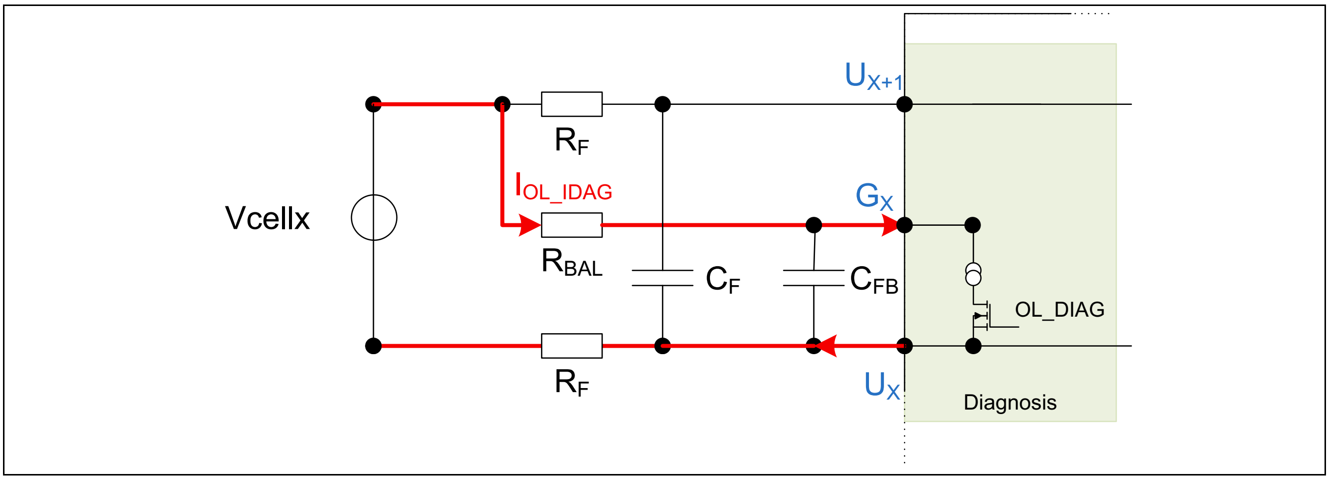


Figure 10 Current path for open load detection

5.5.1 Automatic open load detection

The TLE9012AQU offers the possibility to automatically detect open wires in the following pins: Ux, Gx, VS/U12P and GND.

The following steps are executed in the automatic open load detection:

- Turn off diagnosis current sinks and balancing switches (just to be sure that they are off).
- Wait for the duration set in the CVM_DEL (register **MEAS_CTRL**).
- Voltage measurement with all CVM in fast acquisition mode (10 bits in 75 µs).
- Measure block voltage with BVM. This step is done simultaneously with the previous one.
- Store all 13 intermediate values (12x CVM + 1x BVM) and perform ADC check.
- Turn ON all ODD diagnosis current sinks.
- Wait for the duration set in the CVM_DEL (register **MEAS_CTRL**).
- Voltage measurement with all ODD SD-ADC.
- Turn OFF all ODD diagnosis current sinks.
- Compare ODD results.
- Turn ON all EVEN diagnosis current sinks.
- Wait for the duration set in the CVM_DEL (register **MEAS_CTRL**).
- Voltage measurement with all EVEN SD-ADC.
- Turn OFF all EVEN diagnosis current sinks.
- Store all 12 intermediate values (6x odd cell specific values + 6x even cell specific values).
- Compare EVEN results.

This test will detect an open wire in the path marked in red on **Figure 10**. The sequence above happens automatically within every RR (see also **Chapter 8**). Once the results are available the following conclusions can be derived:

- If the wire is intact, the voltage measurements before turning on the diagnosis current sinks and after turning off again shall have only a small difference (by I_{OL_DIAG}* R_F). If the OL thresholds are set properly to the voltage difference, no OL fault will be indicated.
- If the wire is not connected at the cell (so an open connection between cell + / cell - and the respective R_F or the R_F itself at U_x is broken as open), the measurement comparison will result in a higher delta voltage and an OL fault will be indicated if the OL_max threshold exceeded.
- if R_F at U_x is broken as a short or R_{BAL} is broken open, the result will be a lower delta voltage and an OL fault will be indicated if OL_min threshold exceeded.

Furthermore in order to detect an open wire on the corner wire connecting pins U12P/U12/VS or GND/U0 (or the lowest Ux if less than 12 cells are connected) with the respective cell, all CVM values retrieved during the first CVM measurement need to be added up and the sum should be compared to the BVM (ADC check). This happens automatically in RR in the CVM vs BVM check:

- If the wire connecting U12P/U12/VS or GND/U0 is open, a CVM vs BVM check fault will occur.
- Further distinction between U12P/U12/VS and GND/U0 happens via a cell voltage check (similar to UV but with hard programmed 50 mV threshold). If the lowest cell voltage result is close to zero, the fault happened at GND/U0, and if the highest cell voltage result is close to zero, the fault happened at U12P/U12/VS.
- If both errors which are described above occur (CVM vs. BVM & V_cell < 50 mV) at the same time, the TLE9012AQU also increments the respective OL error counter.

The following diagram shows the full process and the expected voltage variations:

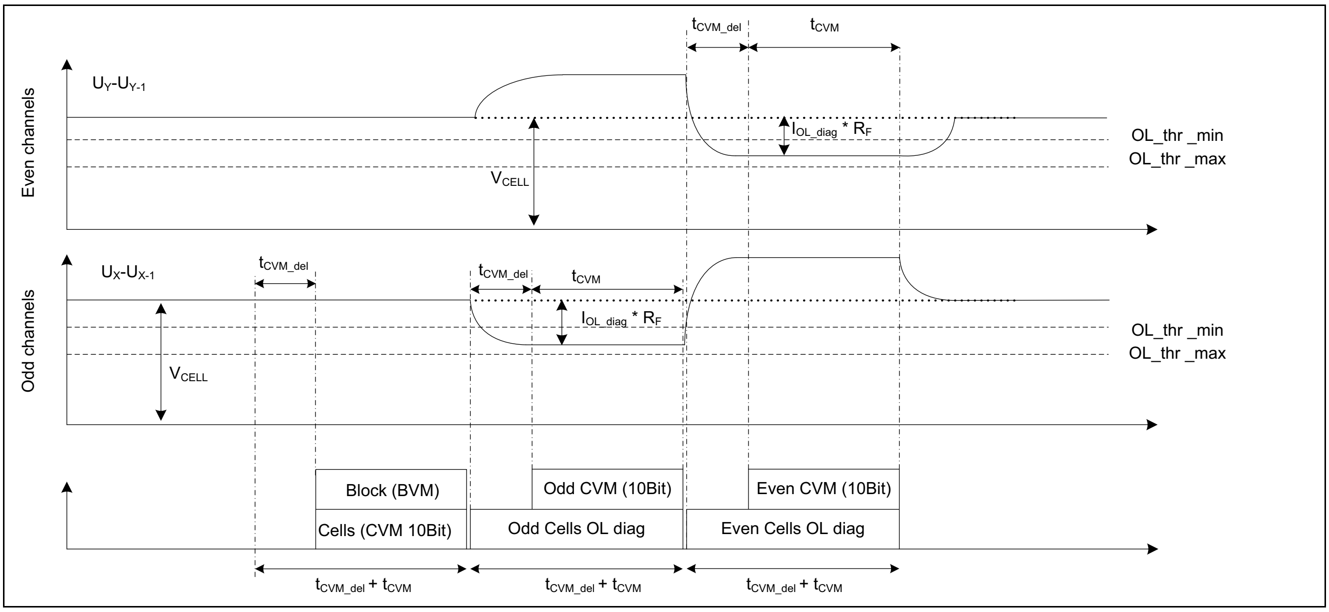


Figure 11 Open load detection timing diagram (no faults)

5.5.2 Overcurrent and undercurrent

The TLE9012AQU offers the possibility to detect over- and undercurrent during balancing. This check will be done during the round robin diagnosis for each cell were balancing was active at the start of the round robin. The check principle is similar to the open load check described in the chapter above.

During balancing, the round robin function will read the cell voltage and compare the value to the expected value (voltage difference = I_{BAL} *R_F):

- If the difference is lower than the threshold UC_THR (register **BAL_CURR_THR**), the undercurrent error counter will be incremented.
- If the difference is higher than the threshold OC_THR (register **BAL_CURR_THR**), the overcurrent error counter will be incremented.

As soon as a balancing error is set in **GEN_DIAG**, the balancing function will be disabled for the given channel. If an external PMOS is used see chapter 5.4.1.

5.5.3 Electrical characteristics

Table 11 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Sink current for open load diagnosis	I_{OL_DIAG}	10	15	18.3	mA	0.75 V ≤ V_{cell}	
Open load							
Open load threshold maximum value	OL_{thr_range}	–	307.6	–	mV	[1]bit-field with 6 bits	
Open load threshold resolution	OL_{thr_res}	–	FSR/2^{10}	–	mV	[1]FSR = 5 V	
Balancing overcurrent & undercurrent							
Balancing overcurrent error threshold maximum value	OC_{thr_range}	–	1.245	–	V	[1]bit-field with 8 bits. I_{OC_thr} = OC_THR [V] / Rf	
Balancing undercurrent error threshold maximum value	UC_{thr_range}	–	1.245	–	V	[1]bit-field with 8 bits. I_{UC_thr} = UC_THR [V] / Rf	
Balancing overcurrent error threshold resolution	OC_{thr_res}	–	FSR/2^{10}	–	mV	[1]FSR = 5 V	
Balancing undercurrent error threshold resolution	UC_{thr_res}	–	FSR/2^{10}	–	mV	[1]FSR = 5 V	

1) Not subject to production test, specified by design.

6 Cell block voltage and auxiliary measurements

Additionally to the 12 dedicated cell voltage measurement ADCs (CVM), a 13th ADC is available to perform different auxiliary voltage measurements including a block voltage measurement (BVM) from U12P to GND. This ADC has a different reference (Reference B) than the CVM ADCs (Reference A). **Figure 12** shows how the 13th ADC is connected within the device.

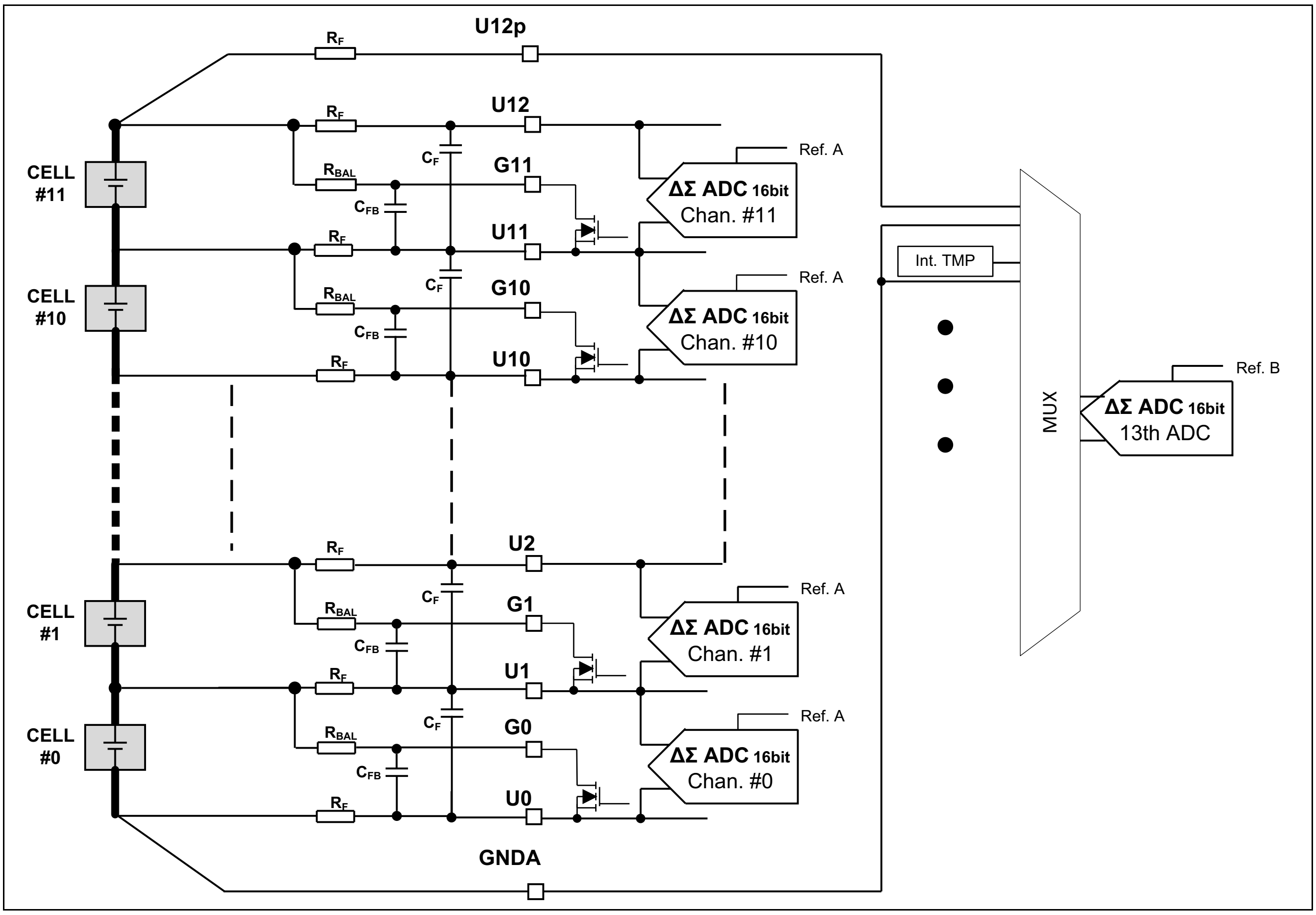


Figure 12 BVM/AVM block diagram

6.1 Cell block voltage measurement (BVM) description

The 13th ADC can perform a block voltage measurement (BVM). This measurement can be used as ADC check of the 12 cell specific voltage measurements by comparing the sum with the BVM result. The block measurement is initiated by setting the BVM_START bit-field in the **MEAS_CTRL** register and starts after t_{BVM_prop}. During the conversion time the BVM_START bit is set ("1") and the RESULT bit-field in the **BVM** register is cleared ("0").

Please note: As soon as a block voltage measurement start command is received, any ongoing round robin schedule will be cancelled and the measurement will start immediately after t_{BVM_prop}. After the measurement is finished, the RR task will be restarted. For more information please refer to **Chapter 8.3**.

By setting the bit-fields BVM_START and CVM_START (register **MEAS_CTRL**) with the same write command, both measurements will happen simultaneously which can be useful for a plausibility comparison in the microcontroller. The conversion time can be selected similar to the CVM:

Table 12 BVM modes

Mode (BVM_BIT_WIDTH [2:0])	Result resolution	Measuring time (t_{BVM})	ADC bandwidth (cut-off frequency)[1)]	FSR
110	16 Bit	~4.68 ms	70 Hz	60 V
101	15 Bit	~2.34 ms	140 Hz	
100	14 Bit	~1.17 ms	280 Hz	
011	13 Bit	~585.1 µs	560 Hz	
010	12 Bit	~292.6 µs	1.12 kHz	
001	11 Bit	~146.3 µs	2.24 kHz	
000	10 Bit	~73.1 µs	4.48 kHz	

1) The given cut-off frequencies are only theoretical calculations assuming 1st order averaging filter and should be used only for orientation purposes. They will neither be tested nor guaranteed.

When the conversion is complete, the result can be read out via RESULT bit-field in the **BVM** register. The result is always an unsigned value. In case the result is less than 16 bits, only the MSBs are useful. The remaining LSBs will be set to "0" automatically.

The equation to convert the value read from the RESULT bit-field in the **BVM** register to the cell voltage is:

Block voltage [mV] = (FSR*1000 [mV] / (2^16)) * RESULT (6.1)

6.2 Auxiliary voltage measurement (AVM) description

The 13th SD-ADC can also be used to measure other internal and external voltages as shown in **Figure 12**. The following AVMs are available:

- external temperature measurement of TMP 0
- external temperature measurement of TMP 1
- external temperature measurement of TMP 2
- external temperature measurement of TMP 3
- external temperature measurement of TMP 4
- miscellaneous auxiliary measurement via TMP0 pin if TMP 0 is inactive in **TEMP_CONF**
- miscellaneous auxiliary measurement via TMP1 pin if TMP 1 is inactive in **TEMP_CONF**
- miscellaneous auxiliary measurement via TMP2 pin if TMP 2 is inactive in **TEMP_CONF**
- miscellaneous auxiliary measurement via TMP3 pin if TMP 3 is inactive in **TEMP_CONF**
- miscellaneous auxiliary measurement via TMP4 pin if TMP 4 is inactive in **TEMP_CONF**
- diagnosis resistor R_{DIAG} of external measurement unit

The TMP measurements happen on a cyclical basis within the round robin scheduler (see also **Chapter 8.3** and **Chapter 7**). So the measurement data will be periodically refreshed and is accessible in the corresponding result registers. Furthermore, the miscellaneous auxiliary measurements (in case the corresponding TMP is inactive) as well as the diagnosis resistor measurement must be triggered manually.

The measurement start of a manual triggered AVM happens by setting AVM_START in the **MEAS_CTRL** register. Which of the AVM measurements are performed can be set by the bit-field AVM_xxxx_MASK or R_DIAG bit-field (register **AVM_CONFIG**).

6.3 Electrical characteristics

Table 13 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Cell sense inputs							
BVM input current U12P	I_{U12P_BVM}	–	280	400	µA	[1]during BVM	
Synchronization timing							
BVM propagation delay within IC	t_{BVM_prop}	0	–	10	µs	[1]Propagation delay between complete arrival of BVM start message and the actual start of the BVM	
Block voltage measurement							
BVM input range	V_{BVM}	4.75	–	60	V	[1]$V_{BVM} = V_{U12P} - V_{GND}$	
BVM resolution	V_{BVM_LSB}	–	FSR/2^m	–	V	[1] $10 \le m \le 16$; FSR = 60 V	
BVM ADC sampling frequency	$f_{s\_BVM\_ADC}$	13.44	14	14.56	MHz	[1]	
BVM time	t_{BVM}	–	2^m/ $f_{s\_BVM\_ADC}$	–	s	[1] m bits $10 \le m \le 16$	
Maximum BVM to CVM time deviation within IC	$Dev_{BVM\_CVM\_IC}$	-0.5	–	0.5	%	[1] deviation between BVM time t_{BVM} and CVM time t_{CVM} within one IC	
Maximum BVM time deviation across ICs	Dev_{BVM_chain}	-4	–	4	%	[1] deviation between BVM time t_{BVM} over all ICs	
BVM accuracy EoL[2]	BVM_{ERR}	-70	–	70	mV	[3]14 - 16 Bit mode $4.75\text{ V} \le V_{BVM} \le 60\text{ V}$ $-40°C \le T_j \le 150°C$ ±3 sigma distribution within abs. min/max limits	

Table 13 Electrical characteristics (cont'd)

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
BVM accuracy EoL[2] - 10Bit	BVM_{ERR_10Bit}	-250	–	110	mV	[1][3] 10 Bit mode 4.75 V ≤ V_{BVM} ≤ 60 V -40°C ≤ T_j ≤ 150°C ±3 sigma distribution within abs. min/max limits	
Auxiliary voltage measurement							
AUX input range	V_{AUXn}- V_{TMP_GND}	0	–	2	V	0 ≤ n ≤ 4	
AUX resolution	V_{AUX_LSB}	–	FSR/2^{10}	–	V	[1] FSR = 2 V	
AUX measurement time	t_{AUX}	–	2^{10}/ $f_{s\_BVM\_ADC}$	–	s	[1]	
AUX ADC accuracy EoL[2]	AUX_{ERR}	-45	–	45	mV	10 Bit mode 0.05V ≤ V_{AUX} ≤ 1.95 V -40°C ≤ T_j ≤ 150°C	

1) Not subject to production test, specified by design.
2) End-of-Life; according to AEC-Q100 Grade 1 Rev. H automotive qualification.
3) Parameters are verified during the following conditions: no NTC measurement; no iso UART communication; no AUX measurement

7 Temperature measurement

The TLE9012AQU has 5 inputs for measuring external temperature sensors (NTC's). To measure the resistance a current is forced through the NTC, the resulting voltage drop is measured by the 13th ADC (see **Chapter 6**).

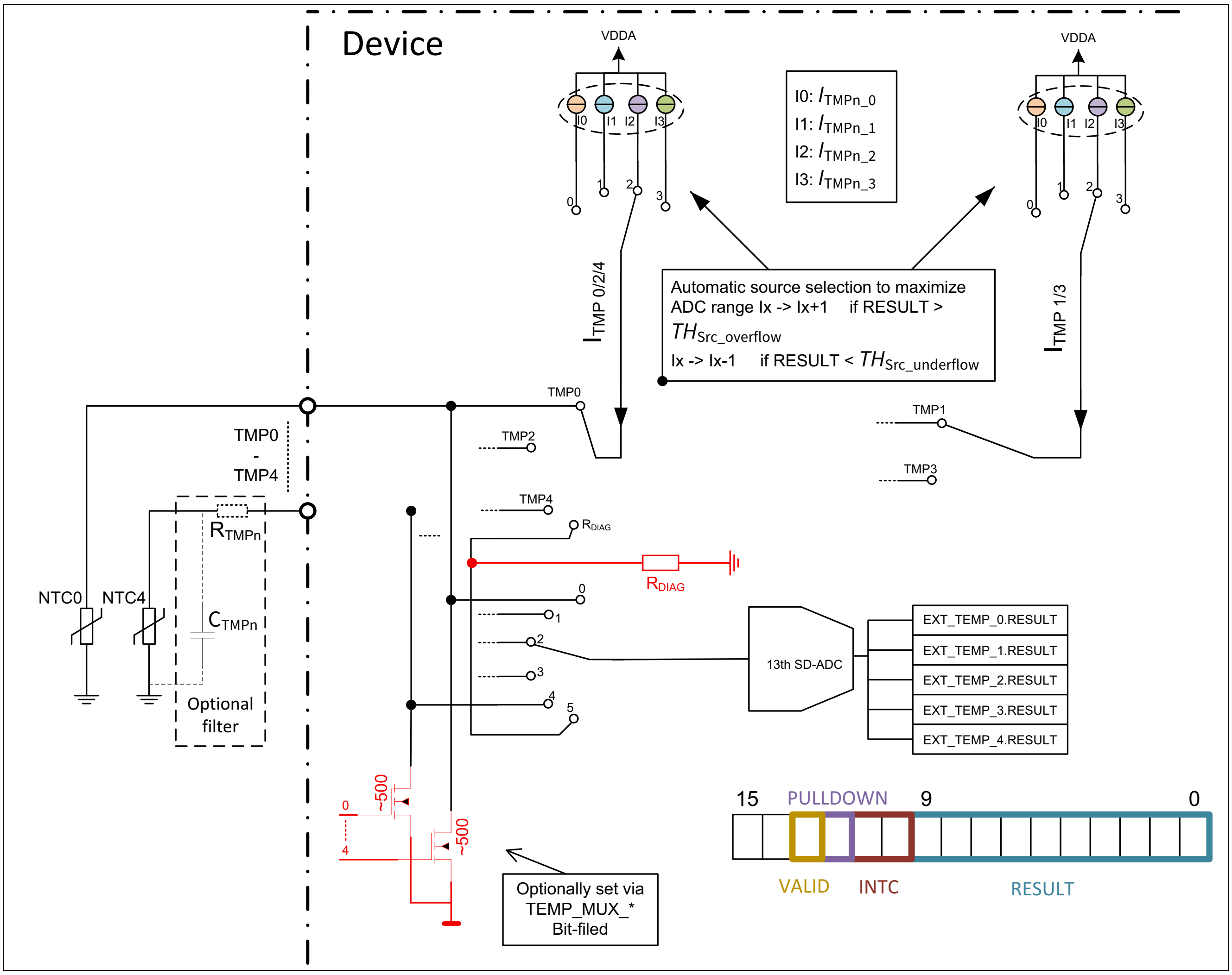


Figure 13 External temperature measurement overview

In order to get a sufficient resistance measurement resolution independent of the resistance range, the TLE9012AQU will – as part of the round robin scheme – automatically identify which one of the four sources is the best one to use.

The measurement will be performed as part of the round robin scheme. Up to two temperature measurements can be performed in every round robin scheme. It is recommended to use the RR_SYNC feature to trigger the round robin manually (see **Chapter 8.3.2**) in case the NTC measurement is actively used as part of it. Goal is to avoid a clash of the round robin and the CVM/BVM/AVM which would delay the round robin execution (see **Chapter 8.3.4**). Reason is that the current sources which power the NTCs are deactivated in case the round robin gets delayed due to a clash with CVM/BVM/AVM.

Results are stored in the respective registers including the information of which current source was chosen for this particular measurement. Based on this information the NTC resistance can be calculated as follows:

R NTC [Ohm] = (RESULT [LSB10]* FSR [V] * 4^{INTC})/(2^{10} * 320 µA) - R_{TMP}; INTC= 0 .. 3 (used current source)

For testing the correct functionality of the temperature sensor multiplexer, pull down switches are implemented to pull each TMP input to ground. These switches can be activated by setting

TEMP_MUX_DIAG_SEL bit-fields (register **AVM_CONFIG**). If the pull down was active during the measurement, this will be shown by setting the respective pull-down_x bit-field in the result register. The VALID_x bit-fields in the same register indicate a valid (new) measurement. They are cleared after readout.

External temperature sensor diagnostics

Overtemperature, shorted NTC, and open NTC faults are detected automatically as part of the round robin scheme of the TLE9012AQU. The short and open detection works in the following manner:

- open detected: RESULT ≥ 1023 [LSB10] & I_{TMPn_3} used
- short detected: RESULT ≤ 64 [LSB10] & I_{TMPn_0} used

The faults are indicated by the fault flag bits in the **EXT_TEMP_DIAG** register. An overtemperature, short, or open fault on any of the NTC inputs will set the EXT_OT fault bit-field in the **GEN_DIAG** register. The EXT_OT fault bit-field is cleared by writing a "0" to this bit-field, which will also trigger a reset of the value of the **EXT_TEMP_DIAG** register to the reset value. The overtemperature threshold and the NTC bias current used for the overtemperature measurement can be selected in the **TEMP_CONF** register.

Furthermore the correct functionality of the measurement unit can be checked by measuring against an internal diagnosis resistor as part of the manual AVM. The diagnosis resistor measurement will be done only via current I_{TMP0_2}.

Internal chip temperature

An on-chip temperature sensor provides information about the internal temperature of the TLE9012AQU near the bandgap references. The value is stored in the **INT_TEMP** register. The junction temperature T_j can be calculated using the formula:

$$\text{Temperature [°C]} = -T_{int\_LSB} * \text{RESULT} + 547.3 \qquad (7.1)$$

7.1 Electrical characteristics

Table 14 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal temperature sensors							
internal temperature resolution	T_{int_LSB}	-	0.66 24	-	K	[1]	
External temperature sensors							
External NTC resistor measurement accuracy	NTC_{ERR}	-2	–	2	%	Accuracy of measured NTC resistance value in the range of 1.22 kΩ to 390 kΩ	
External NTC resistor measurement accuracy	NTC_{ERR}	-3	–	3	%	Accuracy of measured NTC resistance value in the range of 1.22 kΩ to 610 Ω	

Temperature measurement

Table 14 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External NTC resistor measurement accuracy	NTC_{ERR}	-4.8	–	4.8	%	Accuracy of measured NTC resistance value in the range of 610 Ω to 400 Ω	
Temperature ADC voltage input range	V_{TMPn} - V_{TMP_GND}	0	–	2	V	[1] $0 \le n \le 4$	
Measurement current	I_{TMPn_0}	307.2	320	332.8	µA	$0 \le n \le 4$	
Measurement current	I_{TMPn_1}	76.8	80	83.2	µA	$0 \le n \le 4$	
Measurement current	I_{TMPn_2}	19.2	20	20.8	µA	$0 \le n \le 4$	
Measurement current	I_{TMPn_3}	4.5	5	5.5	µA	$0 \le n \le 4$	
Internal TMP diagnosis resistor RDIAG	R_{DIAG}	19.9	–	31.9	kΩ		
Pull-down switch on-state resistance	R_{PD_DSON}	–	–	400	Ω		
Source selection overflow threshold	$TH_{Src\_overflow}$		1000			[1]	
Source selection underflow threshold	$TH_{Src\_underflow}$		200			[1]	
External components							
NTC filter capacitor	C_{TMPn}	–	–	10	nF	[1] $0 \le n \le 4$	

1) Not subject to production test, specified by design.

8 Housekeeping functions

8.1 Functional description

This chapter describes several functions required to function the TLE9012AQU.

These functions are:

- watchdog and wake-up function
- round robin scheme triggering diagnosis checks cyclically
- Emergency Mode (EMM) & ERR pin function

8.2 Watchdog and wake-up function

The TLE9012AQU has a watchdog implemented that if not triggered correctly will transfer the part to sleep mode. If the device is in sleep mode, it needs to receive a wake-up signal in order to trigger the wake-up procedure to enter normal operation.

In the following these two functions will be detailed.

8.2.1 Watchdog counter

A watchdog counter is implemented that must be exercised by regular iso UART or UART communication in order to keep the TLE9012AQU in normal mode. If the watchdog expires, the device will enter sleep mode. The watchdog counter is a 7 bit unsigned down counter. The value of the counter (WD_CNT, register **WDOG_CNT**) after a reset is 0x7Fh. The counter is decremented with a clock of either t_{WD} or t_{EXT_WD} depending on the setting of the EXT_WD bit-field (register **OP_MODE**) (see **Chapter 5.4**).

The WD_CNT value must be written to a value > 0 by either the UART or iso UART interface before the watchdog counter reaches 0. Otherwise the device will revert to sleep mode which includes disabling balancing as soon as the watchdog has timed out.

Additionally the **WDOG_CNT** register contains a main counter (MAIN_CNT) which is a free-running 9 bit up counter clocked with a t_{MAIN_CNT}. This signal is derived from the main oscillator of the TLE9012AQU. The content of this counter can be checked by the host microcontroller in order to verify the value of the main oscillator frequency.

8.2.2 Sleep mode and wake-up function

In sleep mode the power dissipation of the receiver logic is very low. However, the TLE9012AQU will continue to monitor all the communication interfaces (iso UART and UART) waiting for a wake-up sequence. Please note that a wake-up via UART/GPIO is possible if voltage at VIO pin > $V_{VIO\_th\_UV\_rise}$.

The wake-up sequence is a alternating sequence (with frequency f_{WAKEUP}) to be sent by the bus master's iso UART/UART interface.

After n_{WAKE_det} complete periods are detected, the device will trigger a wake-up and will require a wake-up time t_{WAKE} before standard datagrams can be processed. The default direction of the interface where the wake-up signal was detected will be configured as RX (receive) until the device enters sleep mode again. The default direction of the other interface will be configured as TX (transmit) until the device enters sleep mode again.

After t_{WAKE} the device will start generating a wake-up signal at the TX interface to wake up the next device.

Please keep in mind that the wake-up signal will be propagated through the entire network.

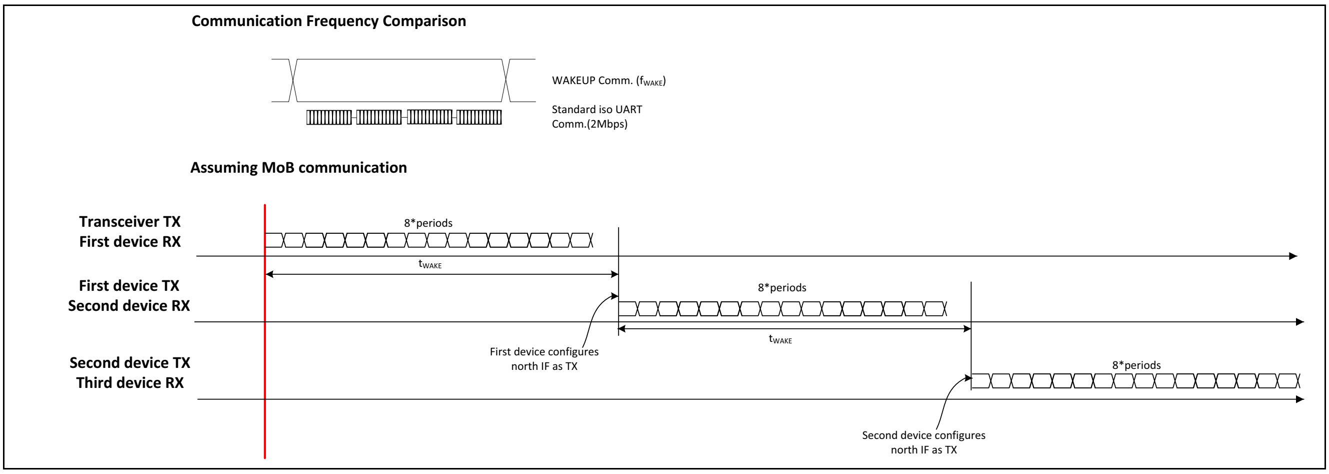


Figure 14 Wake-up signals

Approximately 1 ms after the cells are being connected to the device it will be able to detect a wake-up signal and trigger a wake-up.

8.2.3 Wake-up procedure

After the wake up following default settings will be used:

- The watchdog counter will be set to the max. value: 0x7F.
- The iso UART node ID will be set to 0.
- The internal checks will be started to be ready for measurements.
- Depending what triggered the wake-up:
  - Round robin sleep time-out: Round robin will be restarted. After RR is finished, the part will go immediately into sleep mode.
  - EMM signal received: Signal will also be generated. After the signal has been sent, the part will go immediately into sleep mode.
  - Wake-up signal received: Signal will also be generated.

If the wake-up reason is a wake-up signal, the device will stay awake and wait for enumeration.

The enumeration procedure is started by the microcontroller. After a wake-up signal has been sent through the chain, all the devices are numbered as “#0”, and in this status the devices will not forward any iso UART messages except for EMM signals.

The microcontroller will send (from either the IFH or IFL interfaces) a write command to device ID#0 changing the ID from #0 to #1. With this, the first device in the chain is already numbered as #1. Since it is no longer #0, the first device in the chain will forward the messages further in the chain; therefore the microcontroller can again send a write command to device ID#0 changing the ID from #0 to #2. Now the second device is already numbered as #2. This task must be continued until the message is received by the opposite interface on the microcontroller side (Ring mode: if the first message was sent from IFL that will be IFH or vice versa). The last device in the chain must be marked as final node.

Please note that the numbering in the chain must always be consecutive, starting with the lowest number next to the master of the chain. Otherwise there is a potential risk of clash in the communication bus.

8.2.4 Electrical characteristics

Table 15 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up function							
Wake-up signal frequency	f_{WAKEUP}	48	50	1040	kHz	–	
Device wake-up time	t_{WAKE}	200	370	500	µs	48 kHz wake-up frequency from first falling edge of the input pattern to the first edge of the propagated wake-up sequence.	
Wake-up - number of detected periods	n_{WAKE_det}	4	–	8	periods	–	
Wake-up - length in periods	n_{WAKE}	8	–	8	periods	–	
Watchdog counter							
Watchdog interval step	t_{WD_LSB}	14.5	16	17.8	ms	[1)] EXT_WD = 0	
Watchdog interval step - extended	$t_{WD\_EXT\_LSB}$	13.5	15.07	17	min	[1)] EXT_WD = 1	
Watchdog maximum interval	t_{WD_max}	1.8	2.03	2.3	s	[1)] EXT_WD = 0	
Watchdog maximum interval - extended	$t_{WD\_EXT\_max}$	28.9	31.9	35.5	h	[1)] EXT_WD = 1	
Main counter							
Main counter interval step	t_{count_LSB}	281	292.5 7	305	µs	[1)]	
Main counter maximum interval	t_{count_max}	144.03	149.8	156.03	ms	[1)]	

1) Not subject to production test, specified by design.

8.3 Round robin

The TLE9012AQU provides the necessary logic to perform a round robin scheduling scheme to trigger internal diagnostics to check for possible faults. Furthermore the round robin (RR) scheduling triggers the external (via connected NTC) and internal temperature measurement.

In normal mode the device will run the round robin schedule cyclically. The next chapters discussing the RR scheduler and its tasks. During sleep mode, the device has the possibility to wake-up periodically for a short time to apply one RR scheme. RR during sleep mode is described in **Chapter 8.3.3**.

8.3.1 Round robin tasks

The round robin performs the following tasks:

- Internal temperature measurement & overtemperature check

- Compensation calculations
- Check of block voltage (BVM) vs. sum of all cell voltages (CVM) including needed measurements
- Check of all cells overvoltage
- Check of all cells undervoltage
- Open load detection
- External NTC resistance measurement (2 channels at each RR)
- Balancing diagnosis via over- & undercurrent check (if balancing was activated at start of RR scheme)

The **Figure 15** shows the different tasks and the timing of the round robin in more detail.

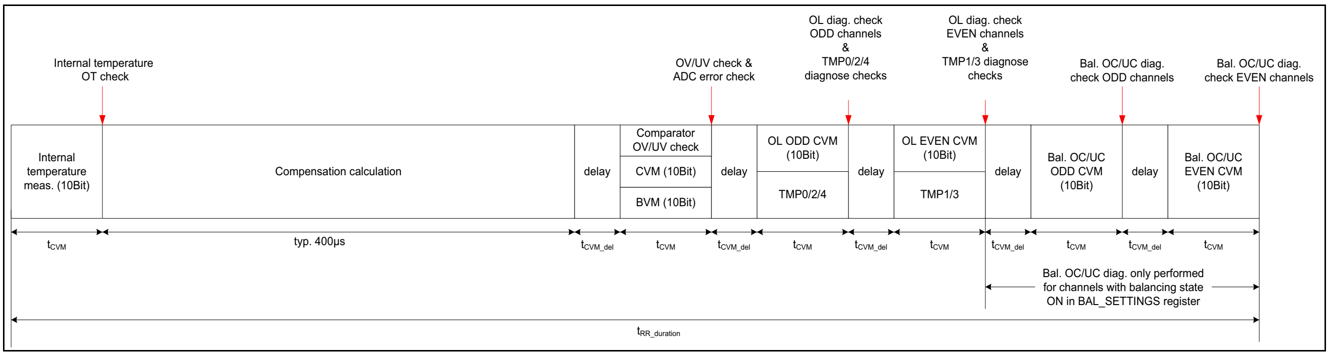


Figure 15 RR task timing diagram

The following sections will describe the tasks in more detail:

Internal temperature measurement

During this check, the internal temperature will be measured with the 13th ADC (10 bit mode), and the result will be compared to the configured threshold (INT_OT_THR, register **INT_OT_WARN_CONF**). Furthermore, the result will be copied into the related **INT_TEMP** register.

Compensation calculation

During this phase the necessary compensation measurements for the compensation are performed and the compensation is calculated.

ADC error check

A cell voltage measurement will be performed for each cell. Furthermore a block voltage measurement will be performed with the 13th ADC simultaneously to the cell voltage measurement. Both results will be compared for a plausibility check. If the comparison fails, the fault counter for the ADC error will be incremented. After NR_ERR (register **RR_ERR_CNT**) consecutively fails, the ADC_ERR bit will be set in the **GEN_DIAG** register. Please note: The results of the measurements are not stored in the CVM and BVM results register to avoid overriding valid and more precise (e.g. 16 bit measured) results.

Cell overvoltage and undervoltage check

The results from above (measured as part of the ADC error check) will also be used to check for over- and undervoltage with a digital comparator. Simultaneously also the analog comparators (described in **Chapter 5.3**) will check the voltage from Gx - Ux for over- and undervoltage. If the voltage of any cell is above the programmed threshold on the **OL_OV_THR** register, identified either by the digital or the analog comparator, the fault counter will be incremented. Consecutive errors > NR_ERR (register **RR_ERR_CNT**) will set the fault bit in the **GEN_DIAG** register and the affected cell will be displayed in the corresponding **CELL_OV** register. The same applies for any detected undervoltage (measurement result lower than programmed threshold on **OL_UV_THR** register).

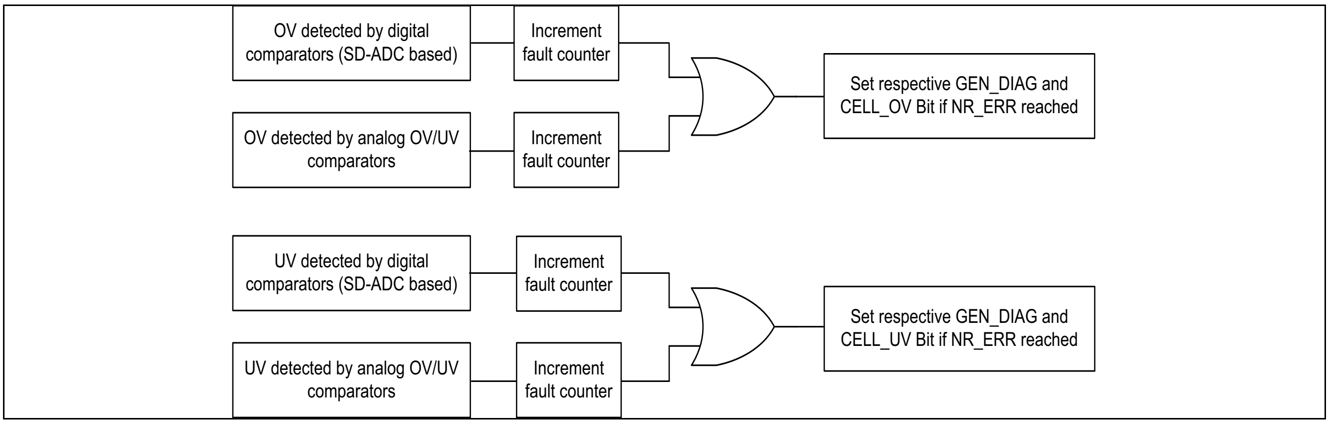


Figure 16 OR function of over- & undervoltage detection check

Pin fine open load diagnosis

The open load detection check is also part of the round robin scheme, please see **Chapter 5.5.1** for more details. If the check fails, the fault counter for the individual open load diagnosis will be incremented. After NR_ERR (register **RR_ERR_CNT**) consecutively fails, the respective open load error bit will be set in the **GEN_DIAG** register.

External resistance measurement via NTC

During this check, the external resistance will be measured with the 13th ADC (10 bit mode) and the result will be compared to the configured threshold (EXT_OT_THR, register **TEMP_CONF**). Furthermore the result will be copied into the related **EXT_TEMP_0** – **EXT_TEMP_4** registers and the valid bit will be set to “1” after a new result is available.

Balancing diagnosis via overcurrent and undercurrent check

The TLE9012AQU performs also a balancing overcurrent and undercurrent check as part of the round robin for each cell were the balancing function was active at the start of OV/UV check. Please see **Chapter 5.5** for more details. If the checks fails, the fault counter for the individual balancing diagnosis will be incremented. After NR_ERR (register **RR_ERR_CNT**) consecutively fails, the respective balancing error bit will be set in the **GEN_DIAG** register.

Please note: It is recommend to mask the fault counter for the balancing overcurrent diagnosis in the **RR_CONFIG** register, so that a balancing diagnosis error gets triggered after the first detection. Reason is the potentially high current in case of an balancing overcurrent. If the fault counter is active (not masked) the individual balancing error counters will be reset as soon as balancing of the corresponding cell gets deactivated. But if balancing gets deactivated for all channels and an individual balancing error counter was already up-counted (but >= NR_ERR) the up-counted error counter value will be kept.

8.3.2 Round robin schedule (during normal operation)

The round robin schedule will be executed during normal operation. The task will be executed always directly after the wake-up procedure. **Figure 17** shows the RR timing and usual duration after wake-up. After the wake-up the RR is executed cyclically. RR_CNT (register **RR_CONFIG**) is available to define the wait time between the RR cycles. The **RR_CONFIG** can be written by the external microcontroller. The RR_CNT counter (register **RR_CONFIG**) has to be between given limits to ensure that internal diagnostics are triggered in a reasonable time frame. The RR_CNT counter will be set back to the value RR_CNT (register **RR_CONFIG**) as soon as the RR started.

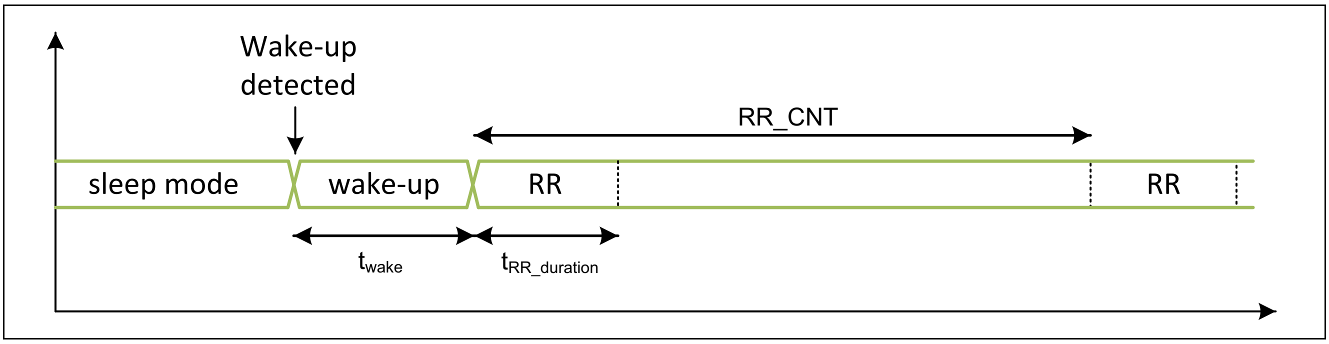


Figure 17 RR wake-up timing

In order to allow a user configurable filter function before a fault in the **GEN_DIAG** register is set, certain consecutive number of faults can be allowed by setting the threshold n_{ERROR} (bit-field: NR_ERR, register **RR_ERR_CNT**). Each possible fault has a counter cnt_{ERROR_x} which is pre-configured to 0. Every time a fault is detected, the counter of the corresponding fault will be incremented. The corresponding fault will be set in the **GEN_DIAG** register if the counter of that fault is > n_{ERROR} (bit-field: NR_ERR). Furthermore if the fault is not masked out in the **FAULT_MASK** register, the device will go into emergency mode (and trigger an EMM signal). If no fault is detected during a RR cycle, the corresponding counter will be set back to 0. Alternatively the corresponding counter will also be set back as soon as the corresponding fault bit in the **GEN_DIAG** register is reset by the host controller.

The counters (cnt_{ERROR_x}) will keep their status while going into sleep mode or coming out of it and will only be reset like described above in normal mode.

In order to reduce power consumption and since the external temperature measurement takes quite a long time, an additional counter cnt_{ET} is implemented. The counter is preset to n_{ET} (bit-field: NR_EXT_TEMP_START). The counter is decremented with each RR. If the counter reaches zero, an external temperature measurement will be triggered for two channels and the counter will be set to n_{ET} again. The time to charge the NTC and its capacitor (optional) is called Tsettle. **Figure 18** shows the round robin timing including Tsettle for the external temperature measurement.

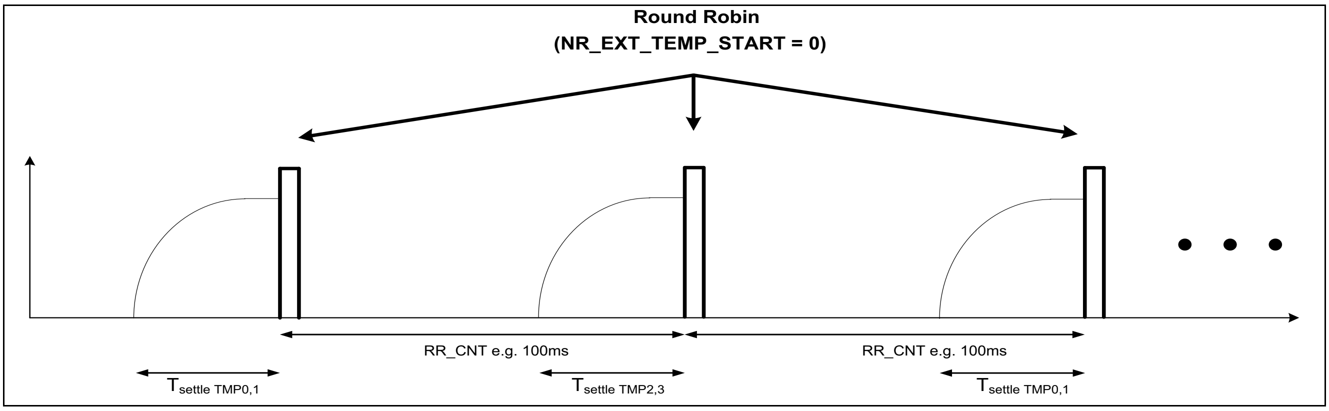


Figure 18 RR timing (assuming 4 active external temperature sensors)

In order to re-synchronize the RR tasks of all the devices in the system and with other sub-tasks like cell voltage measurement, a RR_SYNC bit-field (register **RR_CONFIG**) is available. If this bit-field is set, the round robin scheme will be executed every time the watchdog is reloaded with a write command into the WD_CNT bit-field; in addition, the internal RR counter will also be set back to RR_CNT. It is recommended - especially if the

NTC resistance measurement is used - to use that function to synchronize all temperature measurements. The following **Figure 19** shows how to make sure that the NTCs are charged up correctly when using this function.

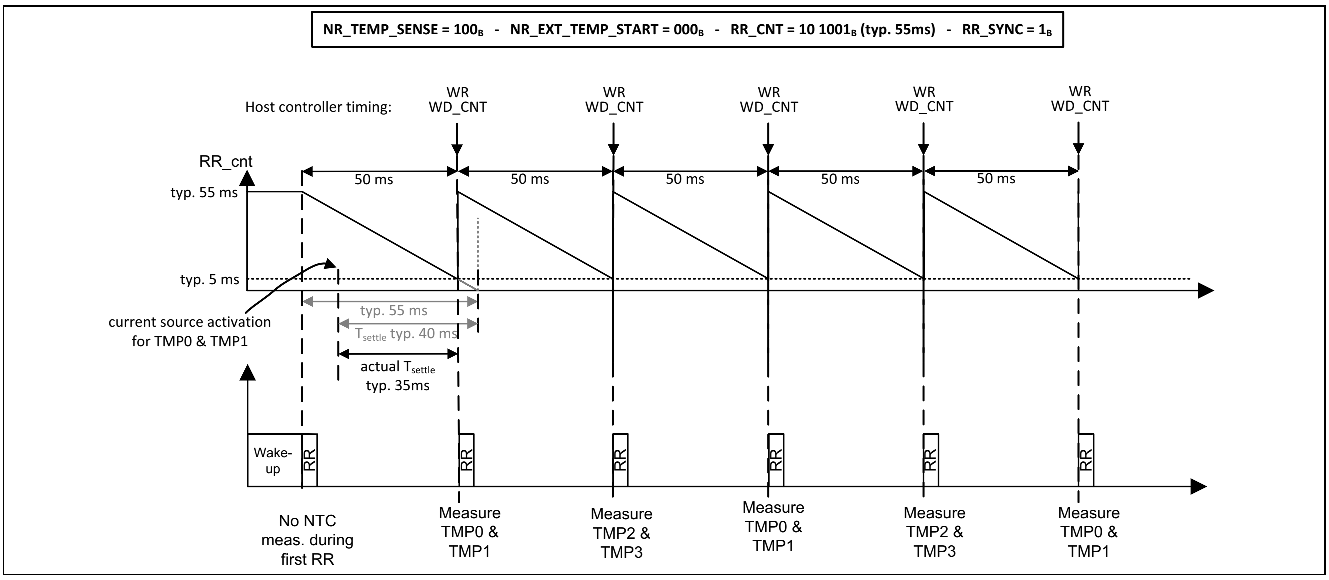


Figure 19 RR_SYNC in conjunction with T_{settle} (assuming 4 active external NTC sensor channels)

The following diagram shows an extract of the typical RR flow to give a better understanding of the fault checking and EMM generation:

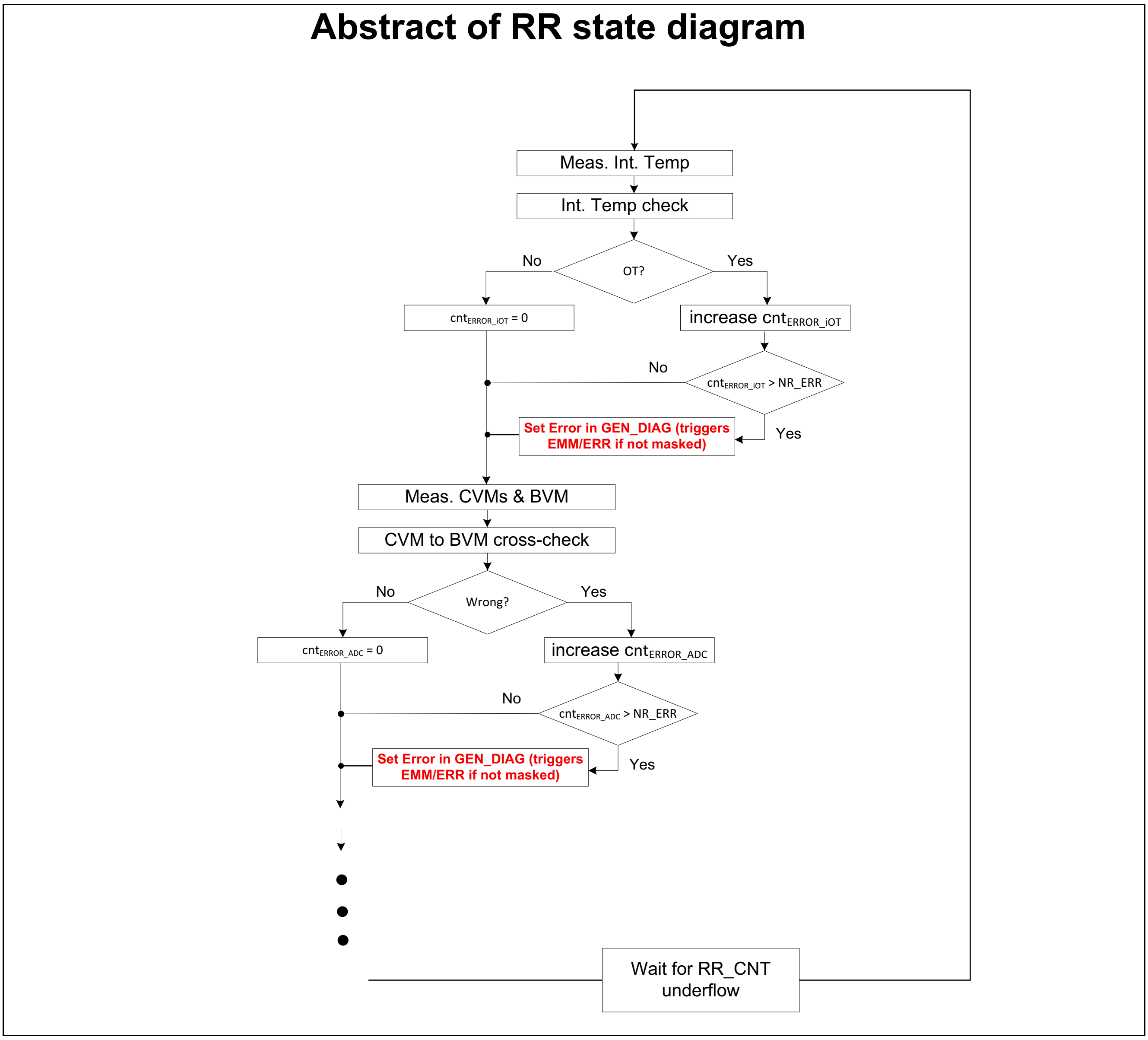


Figure 20 Extract of RR flow to show GEN_DIAG setting and EMM generation

8.3.3 Round robin schedule (during sleep mode)

During sleep mode no internal or external checks are performed but the device includes a feature to wake-up periodically from sleep mode to perform one RR scheme. After the RR scheme is performed and no error in the **GEN_DIAG** is set the device will go back to sleep mode immediately. The function is off by default and can be switched on by setting the RR_SLEEP_CNT bit-field (register **RR_ERR_CNT**). This bit-field defines the time between two wake-up cycles. If a wake-up signal arrives during the periodical wake-up in sleep mode, the part will go immediately to into normal mode.

Figure 21 shows the typical timing in sleep mode. Please note: After the RR scheme is performed and an error in the **GEN_DIAG** is set the device will either send an EMM signal and will go back to sleep mode after the EMM was transmitted or set the ERR pin signal active and go back to sleep mode after t_{WD_max}

Please note as the RR is the first RR after the wake up no external temperature measurement is performed see Figure 24.

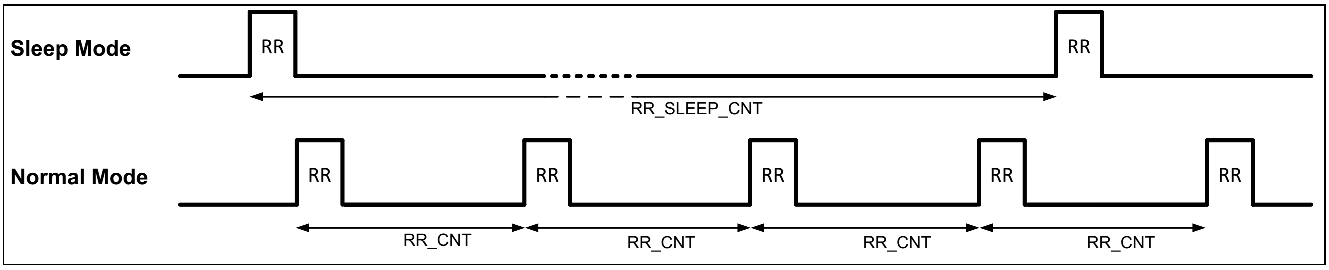


Figure 21 Round robin timing

8.3.4 Prioritization of round robin and manual measurement triggering

The manual triggering of a measurement and the measurements which happen cyclically via the round robin scheduler need to be aligned/prioritized since they are partly using the same physical units.

The timing of manually triggered measurements can be critical, especially for the CVM and BVM measurement. The better the measurements are synchronized globally within a battery system, the more accurate are the SoC/SoH models in the microcontroller. Furthermore the synchronization of the CVM and BVM within a device guarantees an accurate measurement comparison. Therefore the manually triggered measurements of CVM and BVM have priority over the RR scheduler and start immediately (see also **Chapter 5.2**, **Chapter 6.1** and **Chapter 8.3**). **Figure 22** illustrates the various scenarios for the CVM and BVM measurements and how these are processed. Please note that the RR scheduler duration $t_{RR\_duration}$ depends on the chosen CVM_DEL configuration.

The manually triggered AVM measurement and the cyclically triggered RR work with the same principle as the CVM/BVM. So the AVM has priority over the RR. The only difference is that the AVM does not include a CVM_DEL. The AVM measurements are happening sequentially in the same order as defined in the **AVM_CONFIG** register from LSB to MSB. If BVM and AVM started at the same time only BVM is executed.

As shown in the figures, the lock measurement bit-field (LOCK_MEAS, register **GEN_DIAG**) is introduced to prevent multiple triggers by the microcontroller while a measurement is happening and to prevent overriding the RR continuously.

If the temperature measurement within the round robin is used it is recommended to use the RR_SYNC feature to trigger the round robin manually (see **Chapter 8.3.2**). Goal is to avoid a clash of the round robin and the CVM/BVM/AVM which would delay the round robin execution. Reason is that the current sources which power the NTCs are deactivated in case the round robin gets delayed due to a clash with CVM/BVM/AVM.

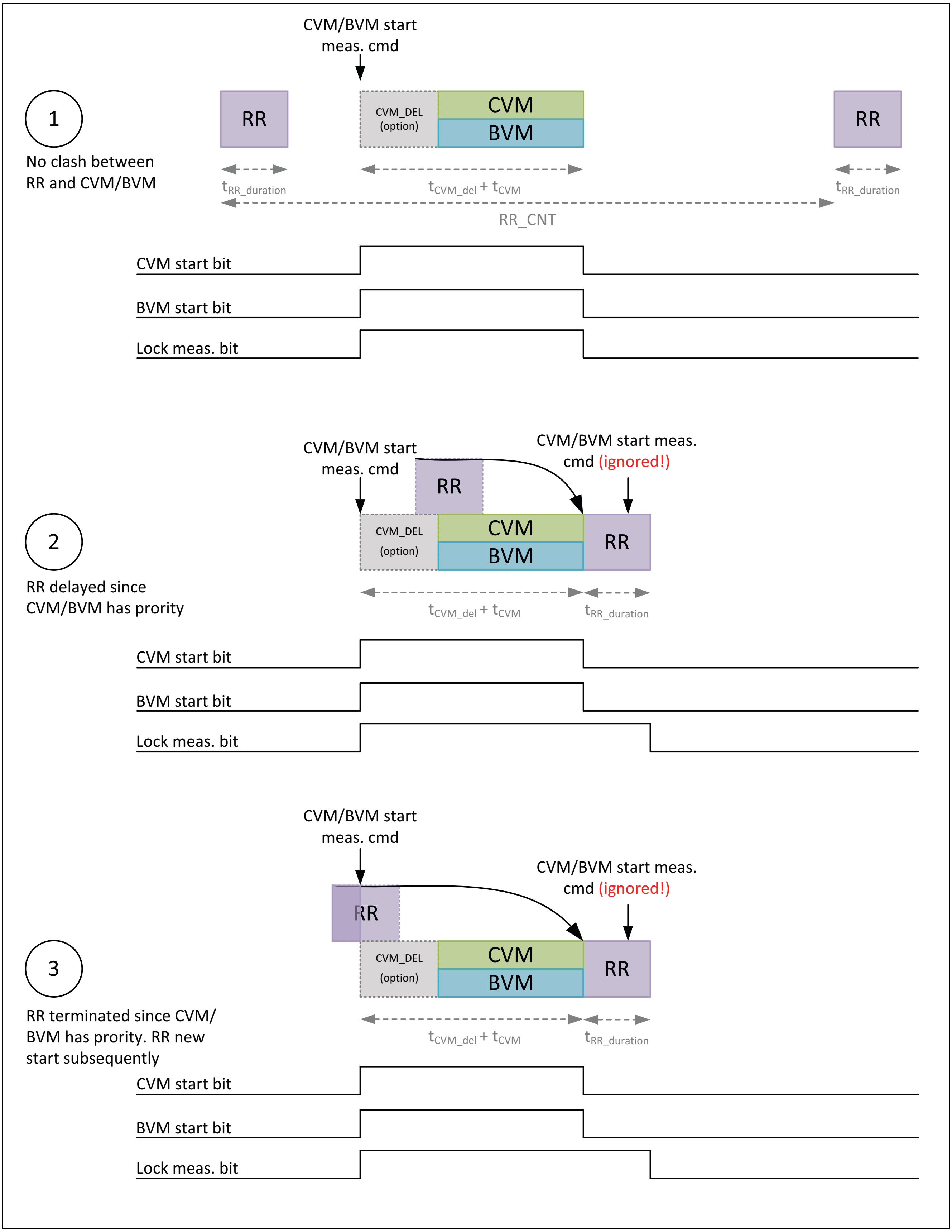


Figure 22 Timing and priority of CVM/BVM and RR measurements

8.3.5 Electrical characteristics

Table 16 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
OV/UV detection							
OV/UV threshold resolution	$V_{OVUV\_thr\_res}$	–	FSR/2^{10}	–	V	[1]10 bit, FSR =5 V	
OV/UV threshold range	$V_{OVUV\_thr\_range}$	0	–	5	V	[1]Cell 0 to Cell 11	
Round robin counter							
RR minimum interval	t_{RR_min}	6.7	7.1	7.4	ms	[1]	
RR maximum interval	t_{RR_max}	149	155.7	163	ms	[1]7 bit counter	
RR interval step	t_{RR_LSB}	1.12	1.17	1.22	ms	[1]	
RR sleep maximum interval	$t_{RR\_sleep\_max}$	155	170.5	190	h	[1]10 bit counter	
RR sleep interval step	$t_{RR\_sleep\_LSB}$	9	10	11.2	min	[1]	
RR scheme duration	$t_{RR\_duration}$	–	1	2	ms	[1]default setting for PBOFF & CVM_DEL	
CRC check cyclic interval	t_{CRC_check}	47	49.15	52	ms	[1]	
Error counter	n_{ERROR}	0	–	7	–	[1]3 bit counter	
current source activation for NTC before RR starts	T_{settle}	38.4	40	41.6	ms	[1]	

1) Not subject to production test, specified by design.

8.4 Emergency mode (EMM) and ERR pin function

Two functions are implemented in TLE9012AQU to signal that an fault occurred:

- Emergency mode (EMM)
- ERR pin function

8.4.1 Emergency mode (EMM)

In case of an detected error, the TLE9012AQU can go into emergency mode (EMM). In this mode, all communication interfaces (IFH, IFL) will generate an emergency signal that can be detected by the transceiver device so that the transceiver can enable its ERRQ pin to forward the error detection to the host controller. The following chapters describe this procedure in more detail.

If the chain is in sleep mode, the devices contiguous to the affected one will first recognize the EMM signal as wake-up signal and will trigger a standard wake-up procedure. After the device is awake, the EMM signal will still be present. Therefore, if $n_{EMM\_dect\_wake\text{-}up}$ are detected after wake-up, it will interpret it as an EMM signal (no standard wake-up anymore) and trigger EMM transmitting mode (by extending the signal to n_{EMM}).

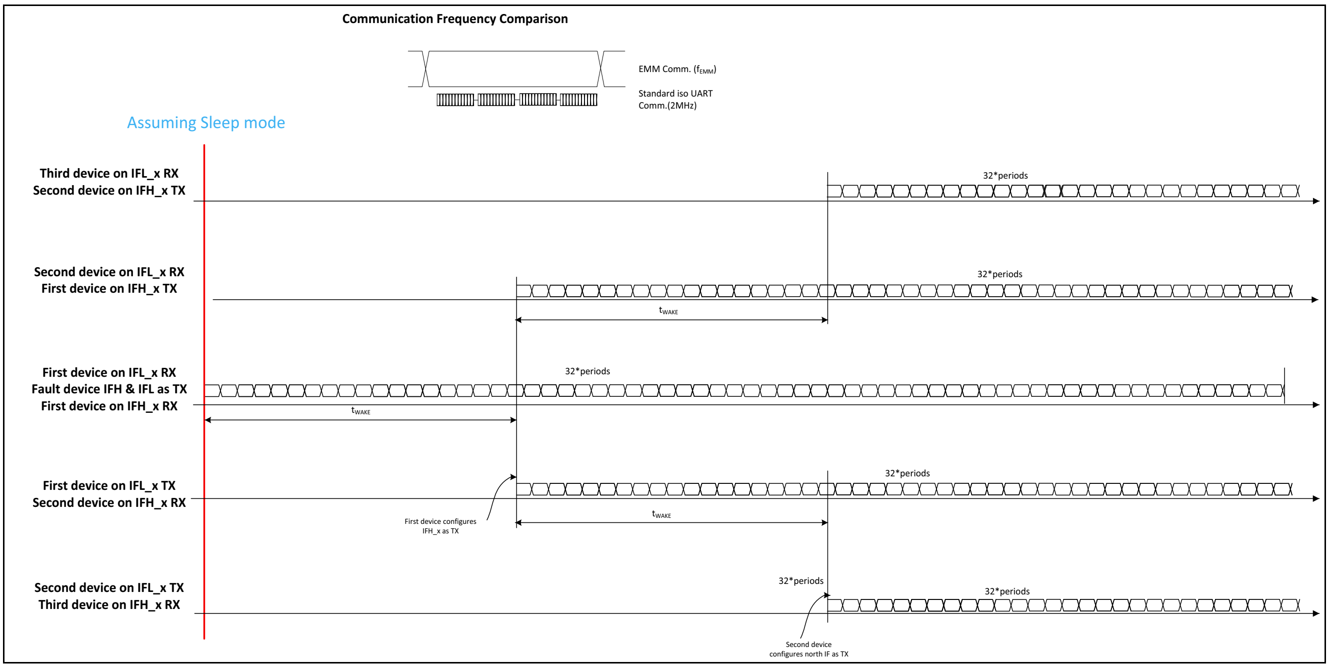


Figure 23 EMM signals during sleep mode

The EMM signal will arrive at the transceiver from both sides (top and bottom) in case of a chain being in sleep mode. After the EMM signal is transmitted, the devices will go back into sleep mode.

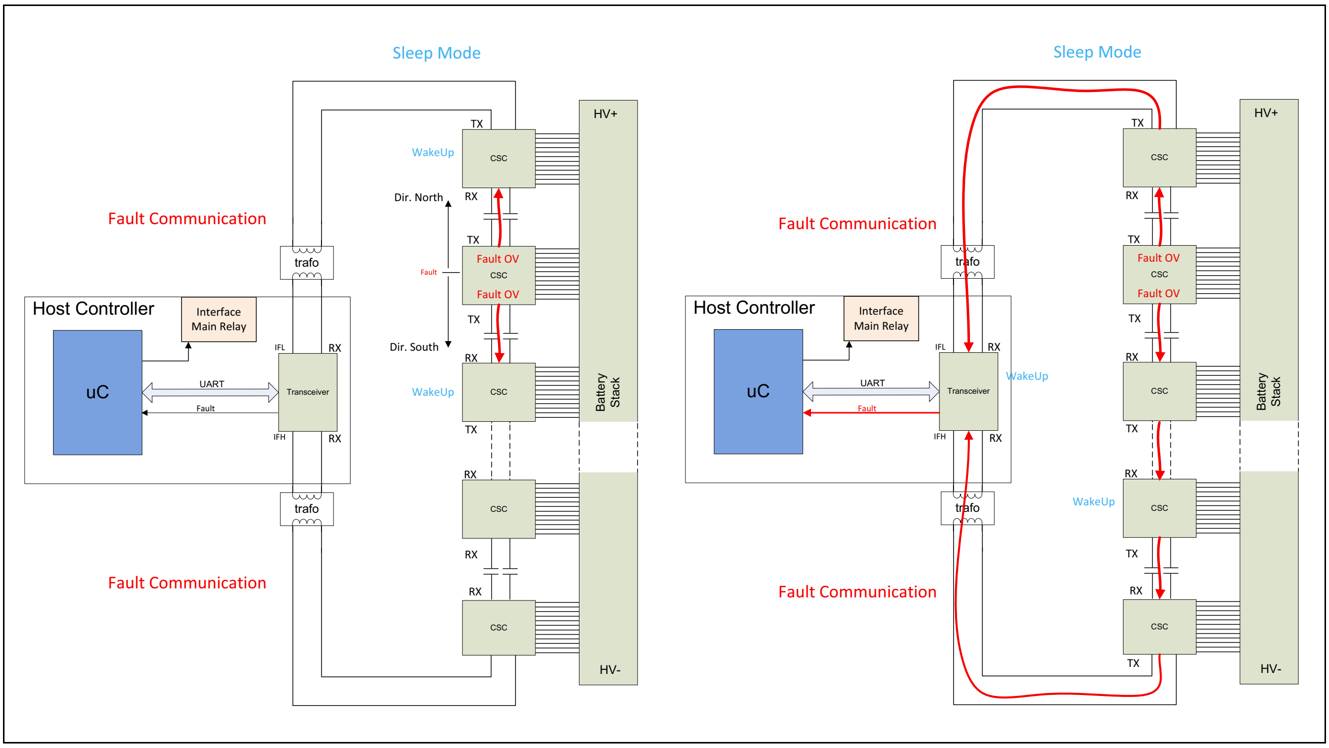


Figure 24 EMM during sleep mode

If the chain is in normal operation (i.e. communicating, measuring, etc.), a communication mode (MoT or MoB) is already defined. The affected device will also start transmitting the EMM signal. However, since the chain is already configured for either MoT or MoB communication, the contiguous devices will show either a TX interface or a RX interface. If the contiguous device shows a TX interface, the EMM will not be forwarded.

Therefore, the EMM signal will follow the path that shows the RX interface back to the microcontroller. The following figure shows an EMM communication in case of MoB/MoT configuration:

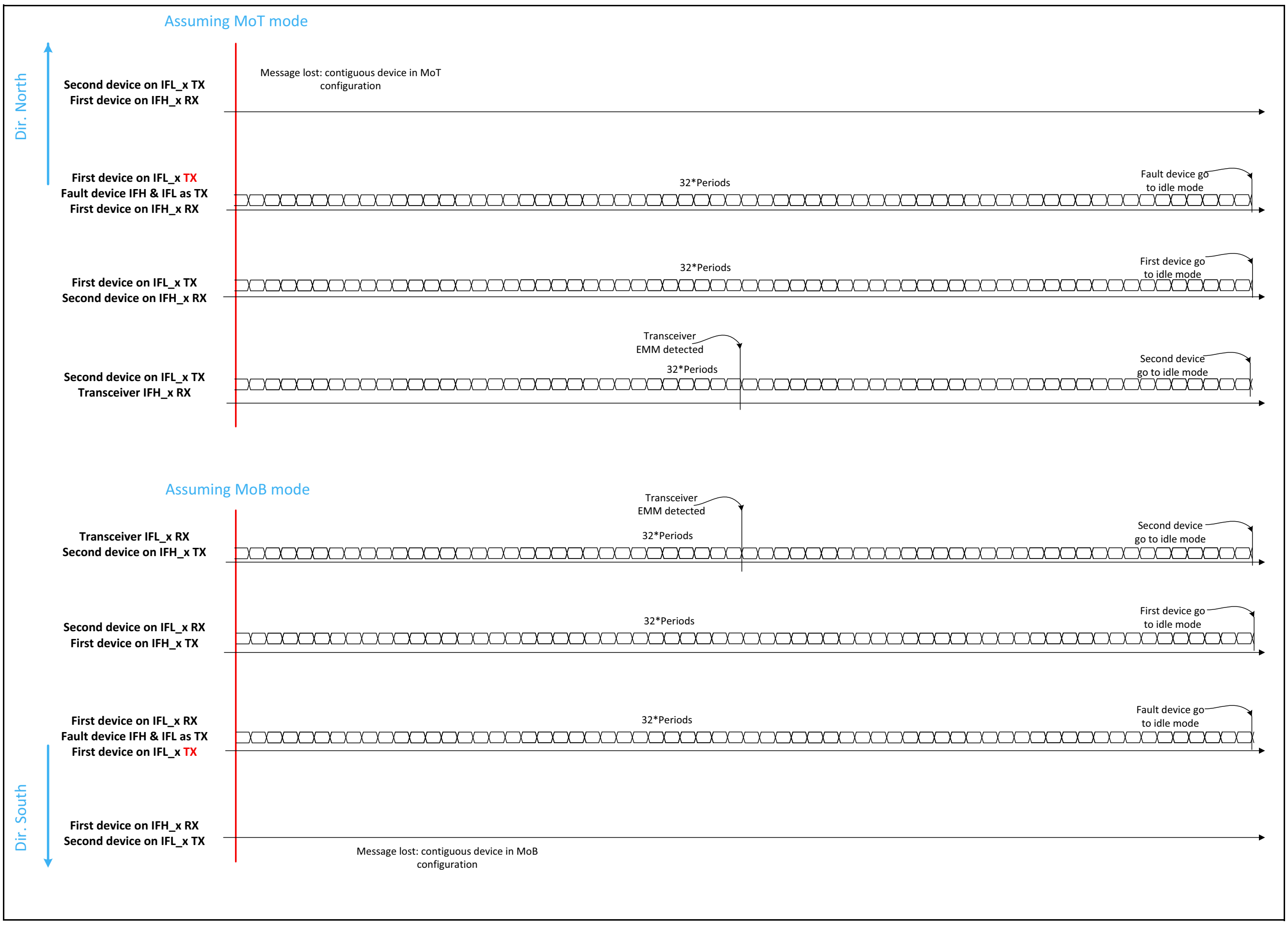


Figure 25 EMM signals during normal operation

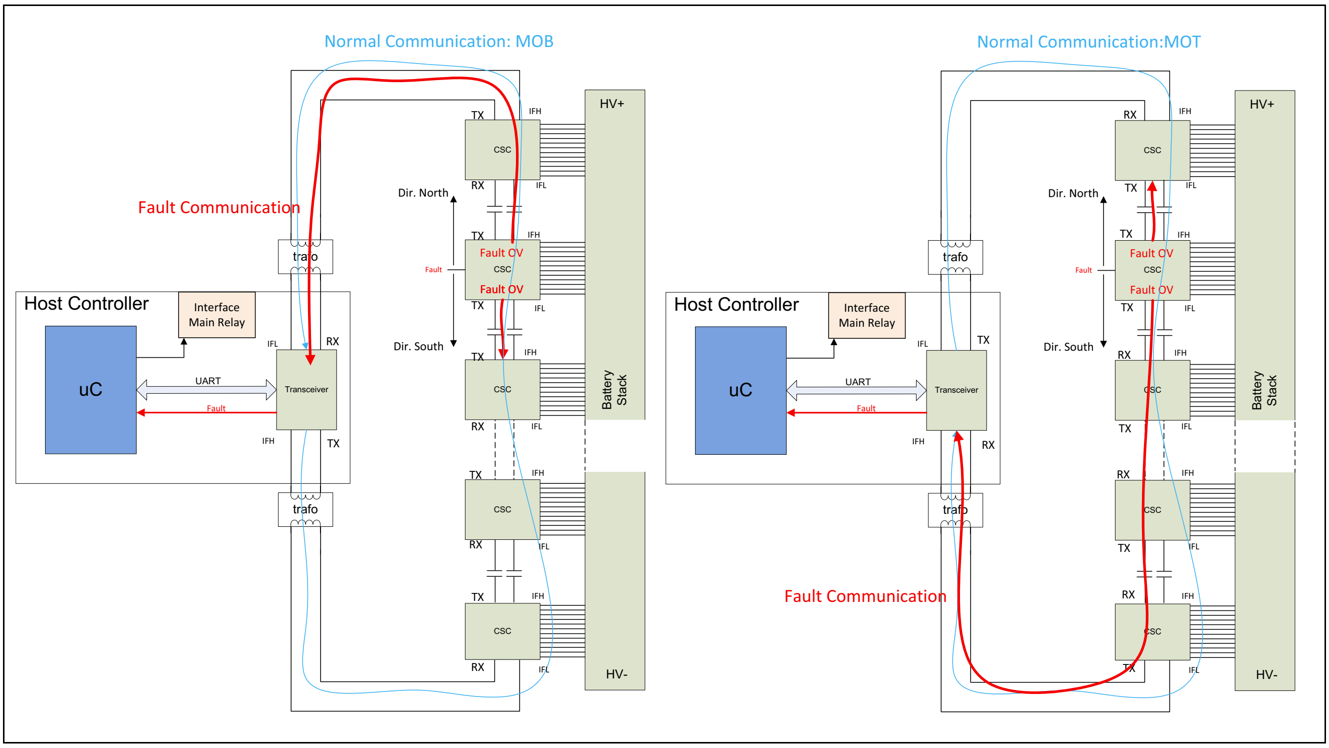


Figure 26 EMM during MoB/MoT configuration

The following possible faults can trigger the EMM mode:

- Overvoltage in 1 or more cells detected
- Undervoltage in 1 or more cells detected
- External temperature fault in 1 or more channels detected
- Open load in any Ux/Gx detected
- Overcurrent balancing error detected
- Undercurrent balancing error detected
- ADC cross-check error
- Internal temperature fault detected
- Register CRC check fault detected
- Internal IC error

All the faults above can trigger the EMM, however there is the possibility to mask any of them out by using the **FAULT_MASK** register. The faults still show up in the **GEN_DIAG** register and are therefore accessible even if they are masked out for an EMM trigger. **Figure 27** shows how the masking and EMM triggering works.

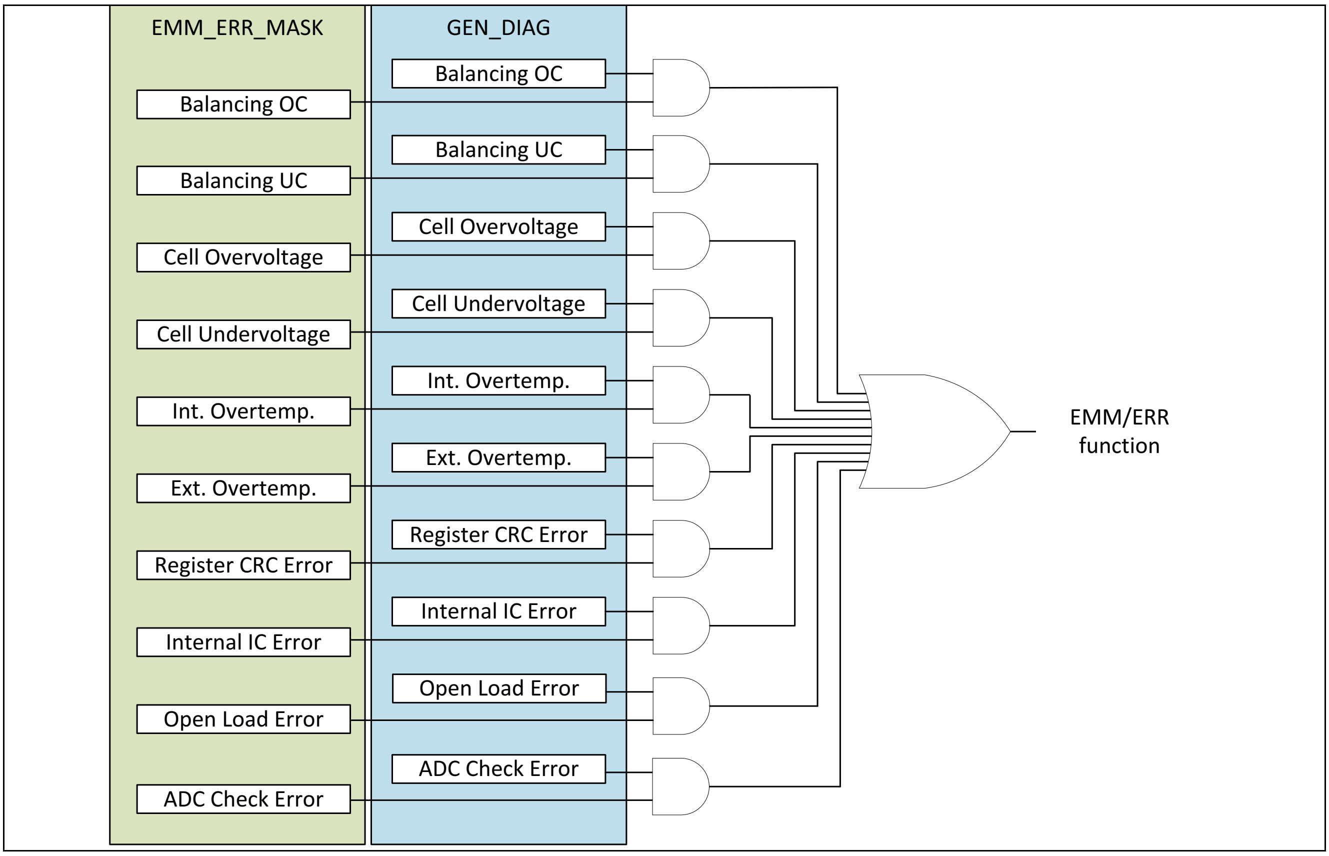


Figure 27 Masking function for EMM and ERR

After the EMM signal is transmitted, the part will go into sleep mode or back to normal mode again depending on which mode it was in before the EMM signal was transmitted.

The fault information in the **GEN_DIAG** register will not be lost by going into sleep mode. Only if the battery is disconnection, the information will be lost. Please note that the **GEN_DIAG** fault bits are latching and can only be reset by the microcontroller or if U12P is not supplied.

During the next round robin cycle after a fault was detected, the device will go again into EMM if the microcontroller did not reset the fault bit in the **GEN_DIAG** register or masked the EMM via the **FAULT_MASK** register in the meantime.

Please note: In case the internal IC error check (bit-field: INT_IC_ERR) routine detects an error during wake-up the LOCK_MEAS bit remains set and there is no round robin execution hence there is no EMM triggering happening at all.

8.4.2 ERR pin function

Additionally to the EMM mode, the TLE9012AQU has an ERR pin available. This pin is intended to be used in non-transceiver based setups (e.g. for only a few number of cells).

- ERR function as counterpart to the EMM signal with a similar functionality

Please note the pin levels are either GND (low) or VS (high).

ERR function

The ERR pin function can be enabled by setting the ERR_PIN bit-field. Enabling the ERR pin function disables the EMM signal via iso UART. After detecting a fault that leads to an emergency signal (see also **Figure 27**), the pin will go high. The following possible faults can trigger the ERR pin function (same as in EMM mode):

- Overvoltage in 1 or more cells detected
- Undervoltage in 1 or more cells detected
- External temperature fault in 1 or more channels detected
- Open load in any Ux/Gx detected
- Overcurrent balancing error detected
- Undercurrent balancing error detected
- ADC cross-check error
- Internal temperature fault detected
- Register CRC check fault detected
- Internal IC error

All the faults above can trigger the ERR pin function, there is the possibility to mask any of them out by using the **FAULT_MASK** register similar to the EMM signal. The faults still show up in the **GEN_DIAG** register and are therefore accessible even if they are masked out for an ERR/EMM trigger. **Figure 27** shows how the masking and ERR/EMM triggering works.

Once the ERR pin function has been triggered, the pin will stay high until all the faults above are cleared by clearing the faults in the **GEN_DIAG** register actively by the microcontroller.The microcontroller can stop this behavior by masking out the detected fault in the **FAULT_MASK** register. During sleep mode the ERR pin is set to low. Please note that the error information in the **GEN_DIAG** register will still be available after sleep mode, hence if the device exits sleep mode, the ERR pin will go high again if the non-masked error is still existing. Please see **Figure 28** for more details.

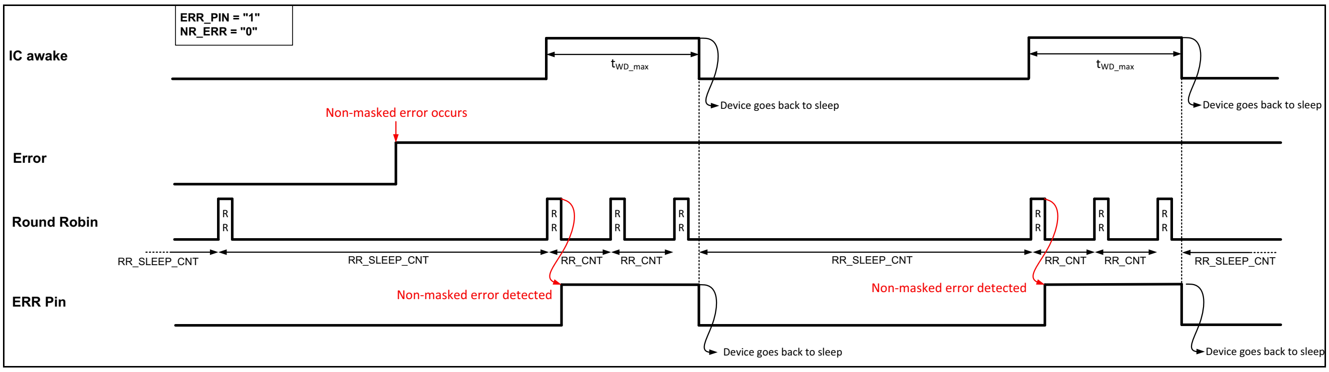


Figure 28 ERR pin function

8.4.3 Electrical characteristics

Table 17 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Emergency mode EMM							
EMM signal frequency	f_{EMM}	48	50	52	kHz	[1]	

Table 17 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Number of periods to detect EMM signal - straight after wake-up	$n_{EMM\_dect\_wake-up}$	4	–	4	periods	[1]number of periods; valid while IC is forwarding wake-up signal	
Number of periods to detect EMM signal - idle mode	n_{EMM_dect}	16	–	16	periods	[1]number of periods; valid while IC is in idle mode and not enumerated (ID = 0)	
Length in periods of EMM signal	n_{EMM}	32	–	32	periods	[1]	
ERR pin function							
Functional range of ERR pin function	V_{ERR}	4.75	–	V_{VS}	V	V_{VS} ≤ 20 V	
Source current	I_{SOURCE}	–	–	1	mA	current capability of pin additionally to R_pull-down (= 100 kΩ) current	
Activated output voltage	V_{ERR}	V_{VS} - 0.25	–	–	V	current capability 1 mA + current for R_pulldown = 100 kΩ	

1) Not subject to production test, specified by design.

9 General Purpose Input / Output (GPIO)

The TLE9012AQU has 4 GPIO pins (GPIO0/1, PWM0/1) which provide a versatile input/output interface. The GPIO0/1 pins have a double function and can be used as UART interface; if the UART is used, the GPIO functionality is deactivated. If the GPIO0/1 pins are not used as UART interface (wake-up received via iso UART interface), they can be configured as a digital input or a digital output. The setting as well as the monitoring of the data can be handled in the GPIO register.

Furthermore, the PWM0/1 can either be configured as standard GPIO (digital in/out) interface or as PWM output. The configuration of PWM0/1 must also be performed in the **GPIO** register. The PWM functionality can be configured via the **GPIO_PWM** register.

For the electrical characteristics of the GPIO please see the electrical characteristics of UART in **Table 18** since UART and GPIO is the same physical pin.

10 Communication interfaces

10.1 Physical layer

The TLE9012AQU supports two types of physical layers: UART-based and iso UART-based. Both are point-to-point communication protocols and can be used to communicate between the microcontroller in the system and the different slaves.

Each TLE9012AQU contains four different units:

- iso UART IFH
- iso UART IFL
- UART HS
- UART LS

In the following chapters each of these units will be described.

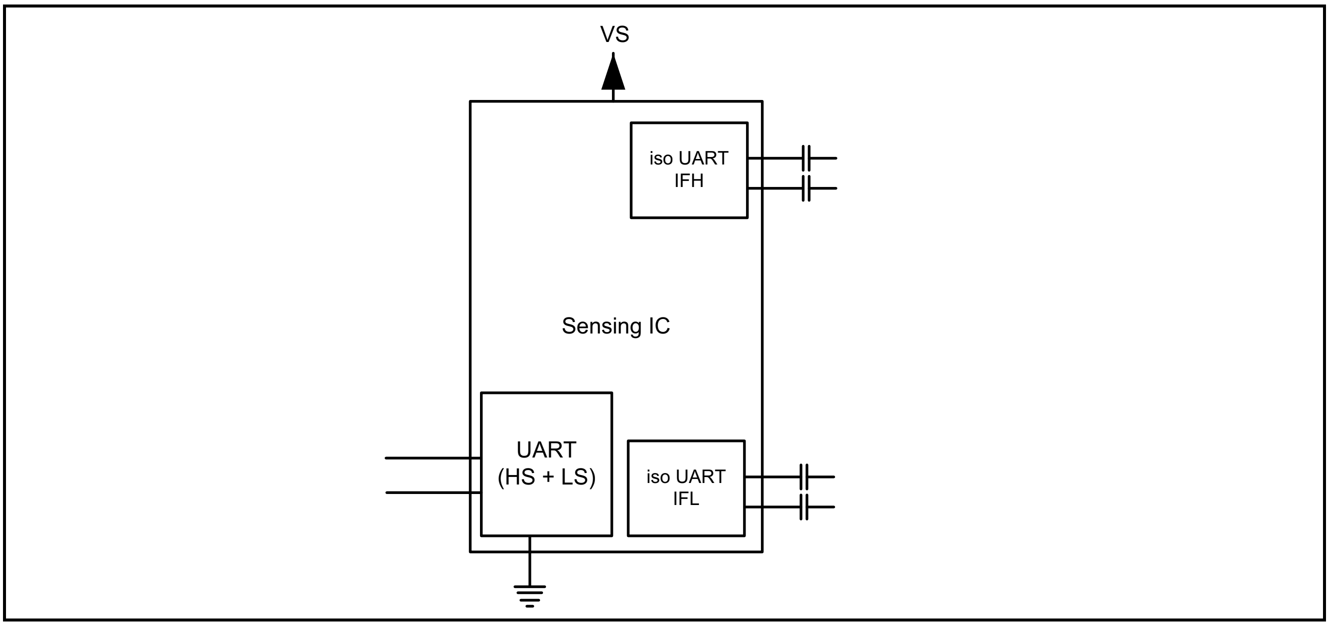


Figure 29 Typical communication block for TLE9012AQU

10.1.1 UART communication unit

The UART communication is logic-voltage-based. The voltage level for this communication is defined by the voltage between VIO to GND.

Due to the necessary GND connection the UART interface cannot be used for interblock communication if the devices are stacked (not galvanically isolated). Therefore the UART unit is intended to be used in systems where a few number of cells need to be controlled (no sensing IC stacking) as direct sensing IC to microcontroller communication interface. UART supports a communication speed of BR_{GPIO}

UART communication needs only 1 pin on the TLE9012AQU side since it has already integrated a logic controller which fulfills the function of switching between Tx and Rx mode. In a typical UART connection can be seen with 2 pins on the microcontroller side.

The UART LS unit is connected to the GPIO0 pin, and the UART HS unit is connected to the GPIO1 pin. These pins have a double function. During sleep mode, these pins will stay in low power RX mode. If a wake-up signal is detected through the GPIOx pins and the voltage at VIO is higher than the $V_{VIO\_th\_UV\_rise}$, the TLE9012AQU will configure the GPIO pin as UART. Furthermore it starts a wake-up procedure (as shown in **Chapter 8.2.3**) configured as MoB (see also **Chapter 10.2.1**) if the wake-up signal came through GPIO0 (UART LS) or MoT if the wake-up signal came through GPIO1 (UART HS). The GPIOx function will be disabled until the next wake-up cycle. On the other side, if the wake-up signal is detected through an iso UART pin, GPIOx will remain as standard IO and the UART function will be disabled until the next wake-up cycle.

If a wake-up signal is detected at the UART LS, the wake-up signal will be generated at the iso UART IFLH interface as soon as the device enters the idle mode. If a wake-up signal is detected at the UART HS, the wake-up signal will be generated at iso UART IFL interface as soon as the device enters the idle mode.

Please note: In case of communication via UART the logic level of the UART pin in default state shall be static "1".

The only difference between UART and iso UART communication is the physical layer. On higher levels (OSI model), UART and iso UART are equal.

In low voltage systems the ERR pin function is recommended for fault communication to the microcontroller. **Figure 30** shows a typical low voltage application including the ERR pin functionality.

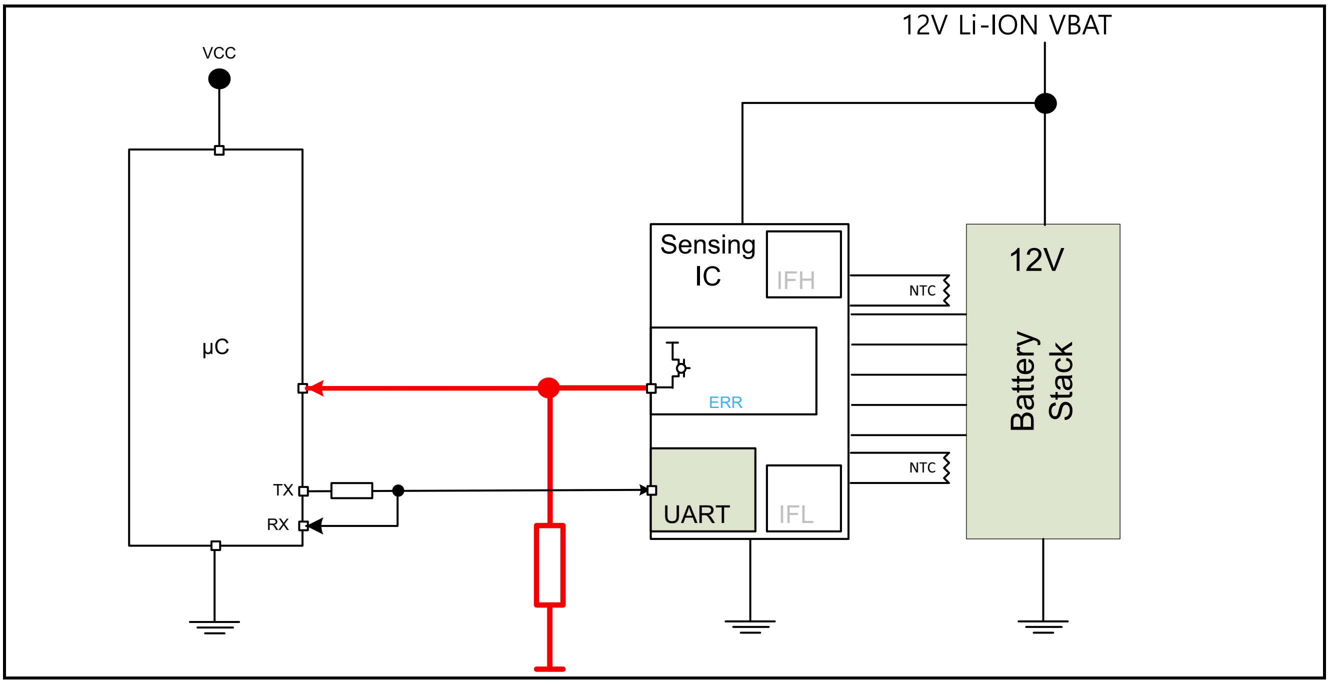


Figure 30 Typical 12 V application including ERR function

10.1.2 Communication Bus (iso UART) unit

The iso UART is an Infineon-proprietary point-to-point communication bus with a dedicated protocol. Every TLE9012AQU node, except the first and the last node in the chain, is connected to two neighboring TLE9012AQU devices via two physical links: high side interface (IFH) and low side interface (IFL).

The iso UART is based on differential bus lines. Both the high and low side interfaces are able to drive the differential lines (TX mode), and both have a differential receiver circuit (RX mode). The bus timing protocol determines which of the interface modules is allowed to drive the bus lines.

The iso UART physical layer is a $\pm V_{VDDC}$ edge detection based interface suitable for capacitive coupling as well as inductive coupling. This interface can offer the required galvanic isolation as well as the robustness to guarantee error free communication between the different CSCs in the battery system.

The iso UART physical layer will forward all messages (except if ID is #0 or the device is in sleep mode) coming in to the opposite side; i.e. if a device was woken up through the IFL, any message coming from the IFL will be forwarded through to the IFH. Also the message will be analyzed by the internal logic. Once the message CRC has been checked, the IC compares the NODE_ID with the message ID and processes the message if the IDs are matching.

The iso UART communication physical layer supports wake-up and EMM communication as described in **Chapter 8**.

The TLE9012AQU can also support a mixed system where the first interface is UART and the rest are iso UART. In this mode, the first IC needs to be woken-up by UART (see **Chapter 10.2**).

10.1.3 Electrical characteristics

Table 18 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
GPIO physical layer							
GPIO input threshold voltage LOW	$V_{GPIO\_th\_LOW}$	–	–	V_{VIO}* 0.3	V	–	
GPIO input threshold voltage HIGH	$V_{GPIO\_th\_HIGH}$	V_{VIO}* 0.7	–	-	V	–	
GPIO output voltage LOW	V_{GPIO_LOW}	0	–	0.45	V	$I_{GPIO} \leq 5$ mA	
GPIO output voltage HIGH	V_{GPIO_HIGH}	V_{VIO}- 0.45	–	V_{VIO}	V	I_{GPIO} >= -5 mA	
UART to iso UART propagation delay	$t_{UART\_isoUART\_del}$	–	25	100	ns	propagation delay from UART to iso UART	
GPIOn output current	I_{GPIOn}	-5	–	5	mA	current capability of GPIO output; $0 \leq n \leq 1$	
External capacitance on GPIOn	C_{GPIOn}	–	–	30	pF	1) $0 \leq n \leq 1$	
GPIO bitrate	BR_{GPIO}	1.45	2	2.1	Mbit/s	–	
iso UART physical layer							
iso UART current threshold LOW	$I_{isoUART\_th\_LOW}$	–6.75	-4.5	–2.25	mA	$(I_{IFx\_H} - I_{IFx\_L}) / 2$	
iso UART current threshold HIGH	$I_{isoUART\_th\_HIGH}$	2.25	4.5	6.75	mA	$(I_{IFx\_H} - I_{IFx\_L}) / 2$	
Transceiver R_{ON} @100 mA	R_{ON}	–	22	–	Ω	–	
iso UART propagation delay	$t_{isoUART\_prop\_del}$	–	25	100	ns	2) propagation delay from IFH to IFL and IFL to IFH	
iso UART bitrate	$BR_{isoUART}$	1.45	2	2.1	Mbit/s	–	
External series capacitor value	C_{SER}	0.95	1	1.05	nF	1)3)	
External series resistor value	R_{SER}	37.05	39	40.95	Ω	1)3)	

1) Not subject to production test, specified by design.
2) Tested with our standard external circuit (C_{SER}, R_{SER})
3) External RC network needs to be adjusted depending on the application constraints (i.e. cable length)

10.2 Bus topology

The TLE9012AQU offers the possibility to work in different configurations:

- Master on Top/Master on Bottom
- Ring mode

10.2.1 Master on Top/Master on Bottom (MoT/MoB)

In this mode, the master (µC) is always on the top or bottom of the chain; the TLE9012AQU will be connected on one side to the master (using the transceiver IC) and on the other side to the next TLE9012AQU in the chain. The next node will also have two connections to the previous neighbor and the next neighbor.

For an MoT topology, the requests will always be forwarded from the IFH to the IFL through the chain. Also for the MoB the requests will be forwarded from the IFL to the IFH. For the response message, the responding device will set both interfaces as TX. Further on, the rest of the chain will forward the message. Some nodes will need to switch their interfaces from TX to RX and RX to TX (this change in the iso UART interfaces is automatically controlled by the internal logic).

For power-balanced communication, the final node needs a termination network. **Figure 31** shows the termination network. The termination network is not required for proper functionality of the device itself.

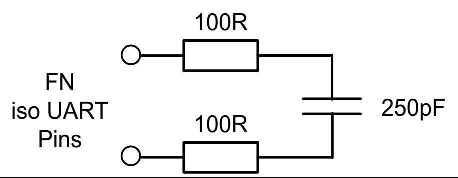


Figure 31 iso UART termination network

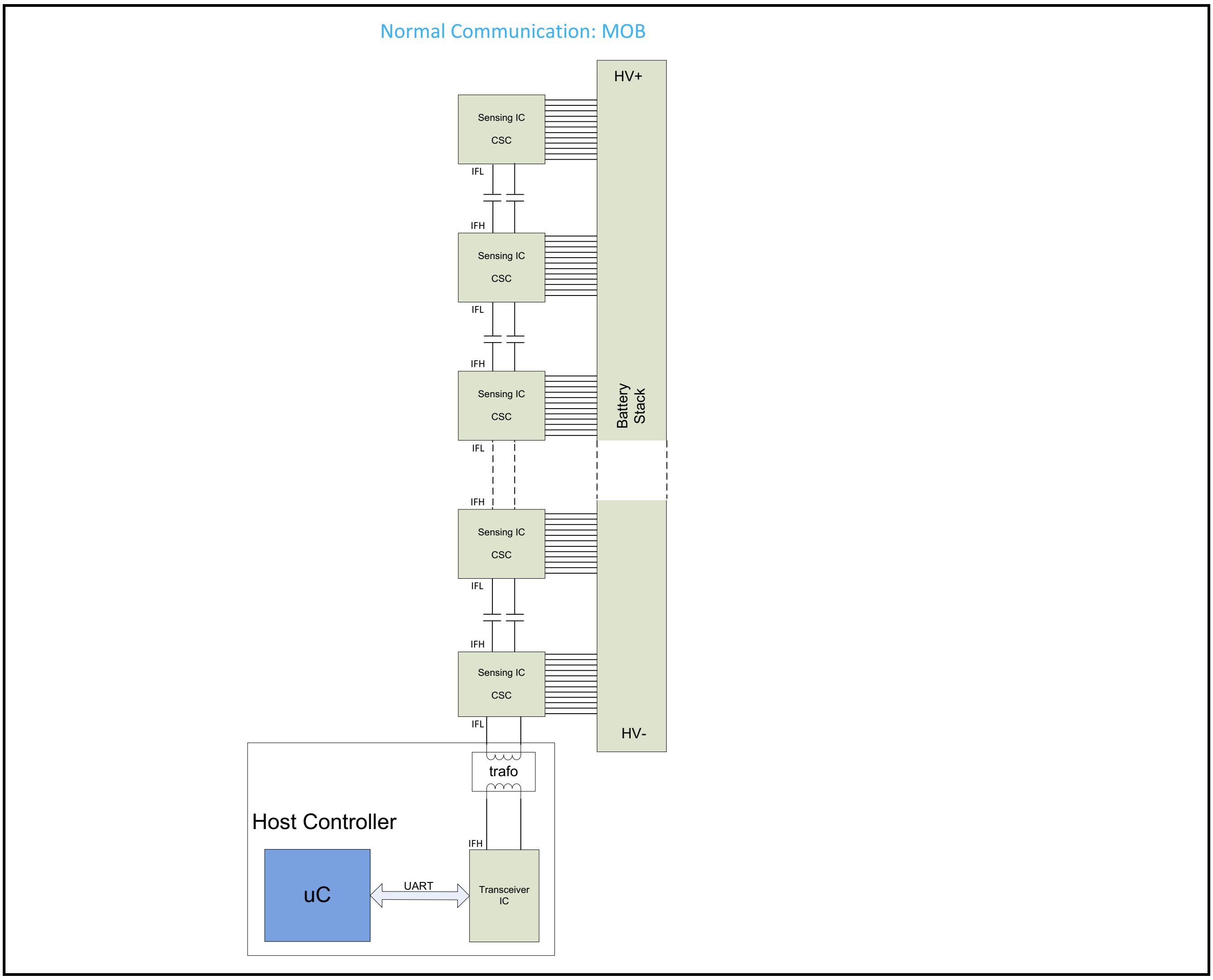


Figure 32 Network architecture for Master on Bottom configuration (simplified)

In case of a Master on Top configuration, the master of the chain will send the wake-up signal through the IFL, and the first device in the chain will receive it through the IFH. For a Master on Bottom topology, the master is sending messages through the IFH and the devices in the chain are receiving them through the IFL.

The topology MoT or MoB can be selected depending on which interface is used for receiving the wake-up signal. After a wake-up procedure is completed, a bit will be set in the **GEN_DIAG** register showing an MoT or MoB topology and this bit will remain fixed until the next wake-up cycle.

The MoT or MoB topology defines the main function (RX or TX mode) of each interface as follows:

Table 19 Interfaces

Topology	iso UART interface	Sleep mode	Idle interface status	EMM mode or response mode
Master on Bottom	IFH	Low power RX	TX	TX
	IFL	Low power RX	RX	TX
Master on Top	IFH	Low power RX	RX	TX
	IFL	Low power RX	TX	TX

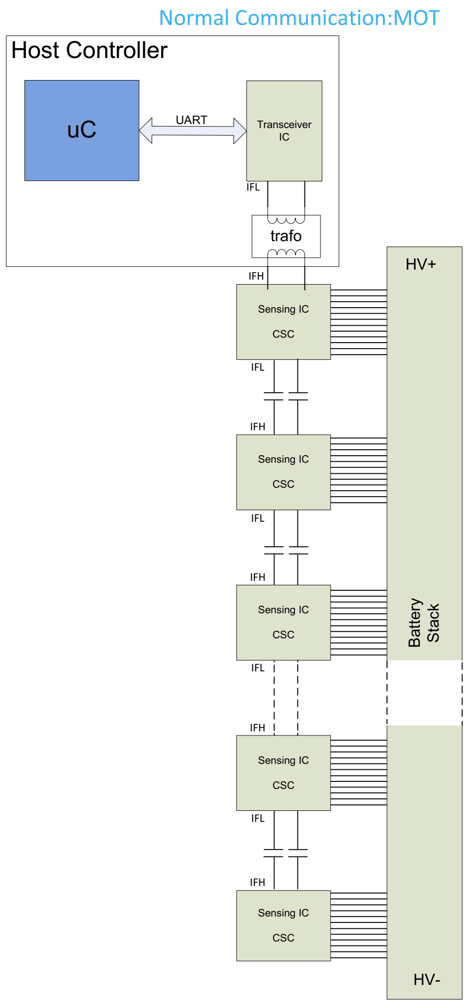


Figure 33 Network architecture for Master on Top configuration (simplified)

10.2.2 Ring topology

The TLE9012AQU offers the possibility to connect all the devices in a system by using the so called ring topology. This topology is very similar to MoB or MoT, but the last node in the chain is as well connected to the master through a second transceiver iso UART interface. In this case no termination network is required.

When using a ring topology the host controller may wake-up the chain by using either UART HS or UART LS. Once the wake-up signal is sent, the direction must be kept until the next wake-up cycle.

The requests will be forwarded through the chain respecting the direction set by wake-up. The master (microcontroller) will receive again the request from the opposite interface confirming that the full chain has no connections problem.

On the other side, the responses will be forwarded in both directions from the responding node. In this case, if the chain has no connection problems, the master will receive the same response from both interfaces.

The ring topology has significant advantages in terms of system availability under fault conditions.

If one of the connections is lost inside the chain, all the parts after this open wire will be separated from the master. In this case, the microcontroller will recognize that there is a problem if after the open wire no response from any node is received. Communication can be still achieved if following steps are considered. The microcontroller has to wait until the watchdog of the lost devices reaches underflow and go into sleep mode. The microcontroller needs to set the transceiver IC into sleep mode. Afterwards, the master can start a new wake-up procedure from the opposite interface to contact the lost devices. This would mean the BMS has then two sub-chains (MoT and MoB) which need to be alternately accessed (Transceiver IC needs to send into sleep mode to switch between MoT and MoB configuration). Please remember that in this case the numbering of the nodes in each of the sub-chains needs to be consecutive again to avoid any clashes in the communication.

Please note that since in this case the network is changed, balanced communication power consumption can not be guaranteed anymore.

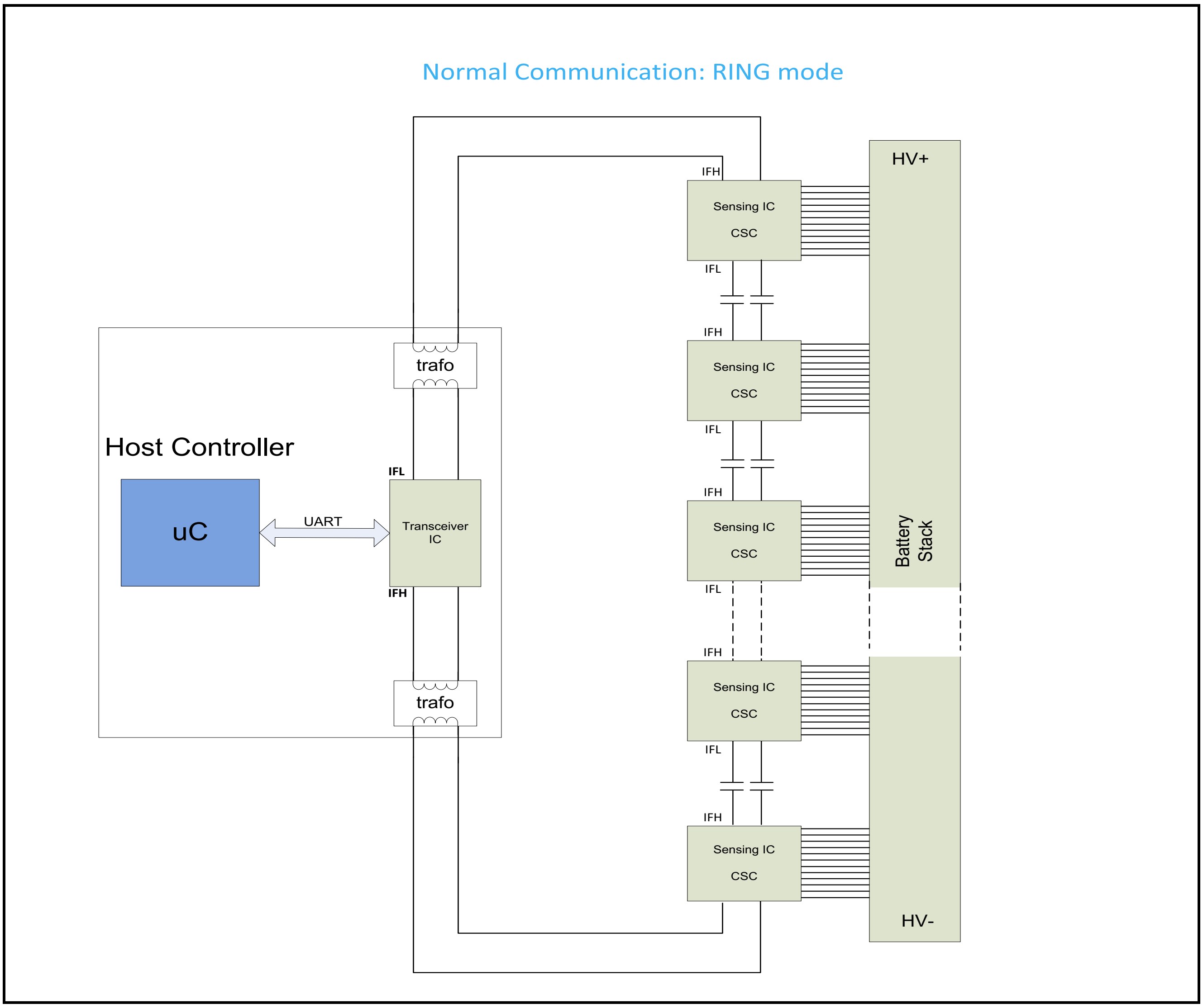


Figure 34 Network architecture for Ring mode configuration (simplified)

10.3 Frame description

The communication (UART or iso UART) frame structure is different for read and write operations. This is due to the fact that a data read request contains less information than a write request. Every request and response contains always a CRC that is checked on the TLE9012AQU on every incoming message. In addition, for every outgoing message a CRC is calculated and sent along with the response. A CRC is calculated over the full message length.

10.3.1 Request frames

There are 5 type of requests from the master:

- Write single register command
- Read single register command
- Read multiple registers command
- Broadcast write command
- Broadcast (BC) read single register command

The write single register command fulfills the function of writing data in one 16 bit register of one device while the read single register command is used to read the data of one 16 bit register of one device e.g. the voltage measurement result of one cell. The reading multiple registers command makes it possible to read multiple registers of one device, e.g. all 12 voltage measurement results of one device. Please see **Chapter 12** for more information.

Additionally a broadcast (BC) command can be used to communicate with all ICs in the chain – either with a BC read single register command to read data from the same register of all ICs, or with a BC write single register command to write data to the same register of all ICs in the chain. A typical command could be setting or reading a timer for all devices with one single command. By using ID=63 the master can initiate a broadcast command.

Please note: Please use only BC write commands to write into the **MULTI_READ_CFG** register if more than one device is connected in a chain.

Figure 35 shows the typical incoming requests from the master:

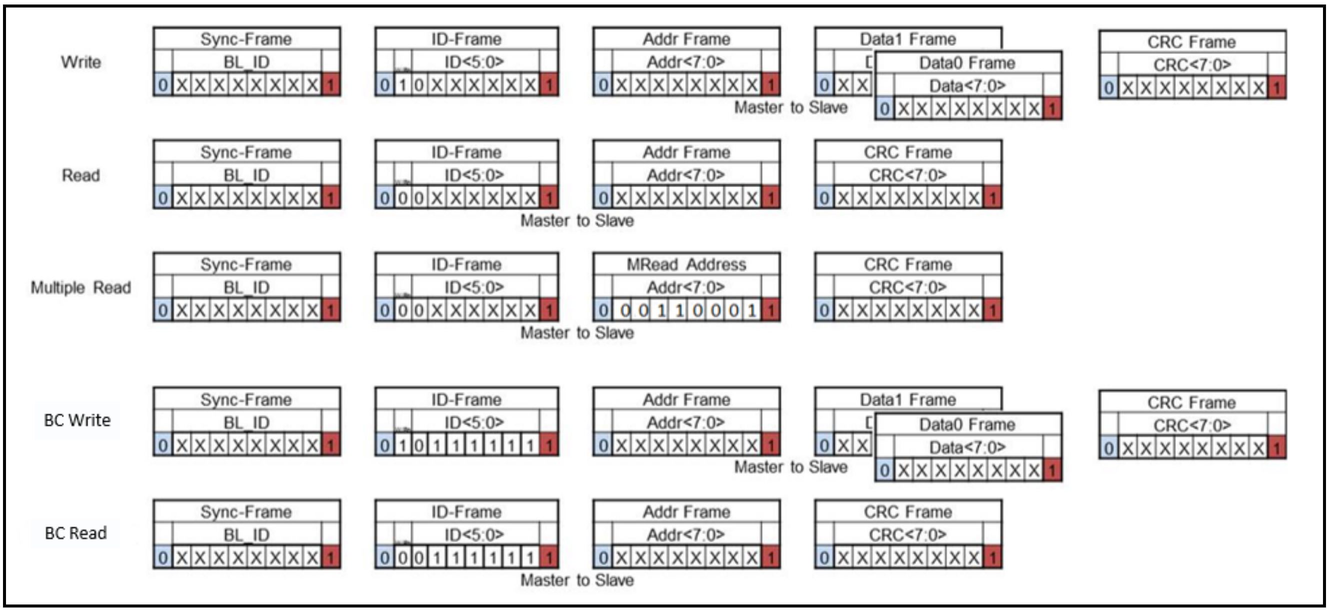


Figure 35 Communication master's possible requests

Synchronization frame

The sync frame is necessary to start the communication with a defined scheme. The sync recognition is edge triggered and recognizes the 0 -> 1 -> 0 -> 1 scheme. **Figure 36** shows the required fixed synchronization frame.

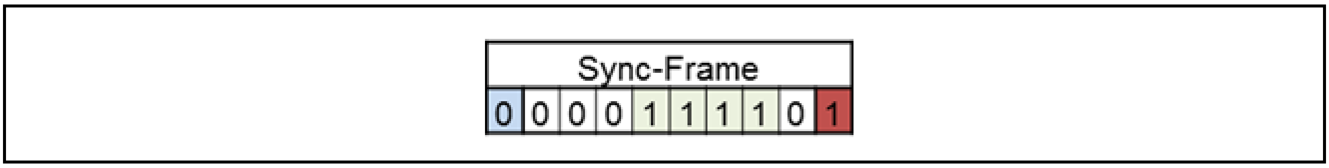


Figure 36 Synchronization frame

ID frame

The ID frame fulfills two functions. The MSB defines the kind of command: 1 means it is a write command while 0 means it is a read command. The next six bits represent the ID of the device the master wants to address. On the other side, all bits 1 in a row in the ID-Frame indicate a broadcast command. Furthermore the ID #0 is a special ID where no frames are forwarded to the next IC (see **Chapter 8.2**). Theoretically this means a maximum of 62 devices can be connected to one master; however only 20 devices are tested and guaranteed.

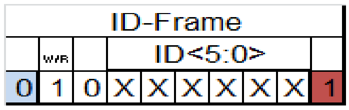


Figure 37 ID frame

Address frame

The address frame represents the register that the master wants to either write or read data. Please see **Chapter 12** for more information on read multiple registers with one command.

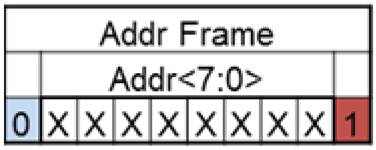


Figure 38 Address frame

CRC frame

As shown in **Figure 35**, cyclic redundancy check (CRC) status is evaluated by the TLE9012AQU.

For both the read and write request frames, a 8-bit CRC is calculated over the complete message length. The CRC code is based on an 8-bit polynomial G(z) = z8 + z5 + z3 +z2 + z +1. The TLE9012AQU calculates the CRC for incoming requests and compares it with the one included in the message. If the calculated CRC and the one in the message do not match, the device refuses to answer. Therefore the master would then run into a time-out and realize that the communication failed.

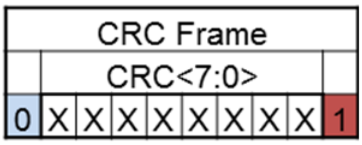


Figure 39 CRC frame

10.3.2 Reply frames

There are 6 different types of reply frames:

- Write reply frame single register
- Read reply frame single register
- Read reply frame multiple registers
- Broadcast write reply frame
- Broadcast read single register reply frame

Nevertheless the different reply frames contain only two different frame structures. One register writing reply frame or different types of reading reply frames.

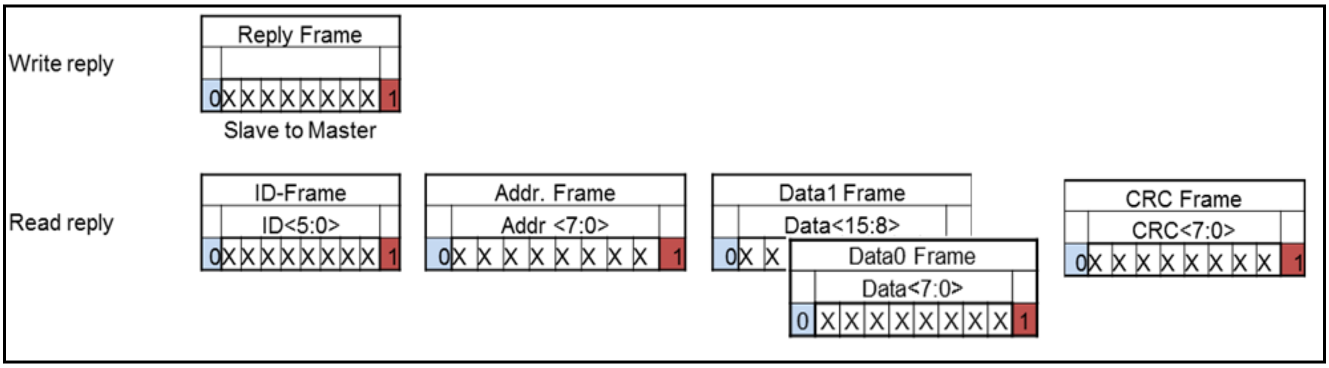


Figure 40 Slave's reply frames structures

Write reply frame

Since the entire register writing process is CRC-protected, there is no need for a detailed acknowledge frame. Therefore the writing reply frame is kept as short as possible to minimize communication-based power consumption and time. In case there is no message CRC error detected by the addressed device, it will send a write reply frame back. This means if the master does not get a write reply frame back after sending a write command, either the addressed device detected a CRC error or the connection is lost completely. The write reply frame contains the information shown in **Figure 41** and **Table 20**. Please see also **Chapter 12** for more information what needs to be considered when writing to registers.

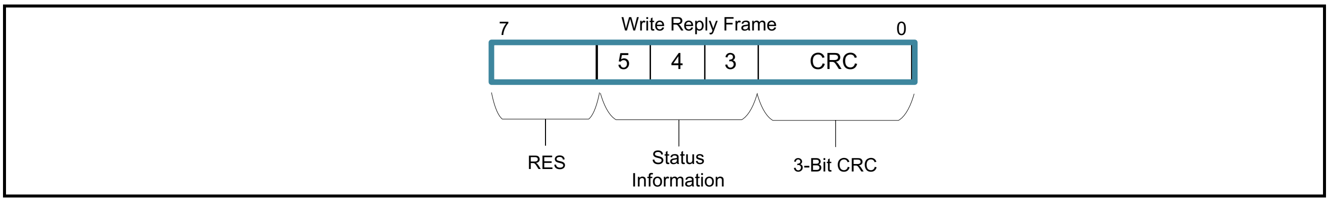


Figure 41 Slave's write reply frame

Table 20 Write reply frame status information

Bit	Data	Status Information
3	0	No fault indicated in **GEN_DIAG** register
	1	At least one fault is indicated in **GEN_DIAG** register
4	0	Register address for write command valid
	1	Register address for write command NOT valid
5	0	Write command was successful
	1	Write command was NOT successful (only checked for CRC protected registers, see also **Chapter 8.3.1**)

In case of a BC write command, each device in the chain will switch RX and TX units after successful writing. Then the last device in the chain (identified by setting the FN-Bit in the **CONFIG** register) sends a reply frame after successful register writing. That frame will be transported through the full chain back to the master if all device in between did switch RX and TX due to a successful writing. If the master receives the reply frame, it is confirmed that the BC write request was successful.

The CRC code is based on an 3-bit polynomial G(z) = z3 + z +1

Read reply frame

There are three different read requests. Depending on the request the reply frames sent by the CSC devices are different. A single register read reply frame looks exactly like shown in **Figure 40**. A multiple registers read reply frame looks like the one shown in **Figure 40** but the CSC device sends such a frame once for each register which is part of the multiple register reading command. The ID will stay constant while the address, the data and the CRC will be different for each message frame.

The BC command reply messages working in the same manner. A BC read for a single register will generate a reply message frame like in **Figure 40** transmitted from the device in the chain with ID #1, followed by the device with the ID #2 with a similar frame and so on. Each response frame will have the corresponding ID of the device which is answering, plus the register address (which will be the same for all Nodes).

10.4 Chain timing

The chain timing is shown in **Figure 42**. The pass through time for each node is $t_{isoUART\_prop\_del}$. This means the microcontroller is still sending while the beginning of the message is already back at the microcontroller in ring mode.

There is a reply delay t_{reply_delay} implemented to make sure that all nodes can change their TX/RX direction properly before their reply frame is send.

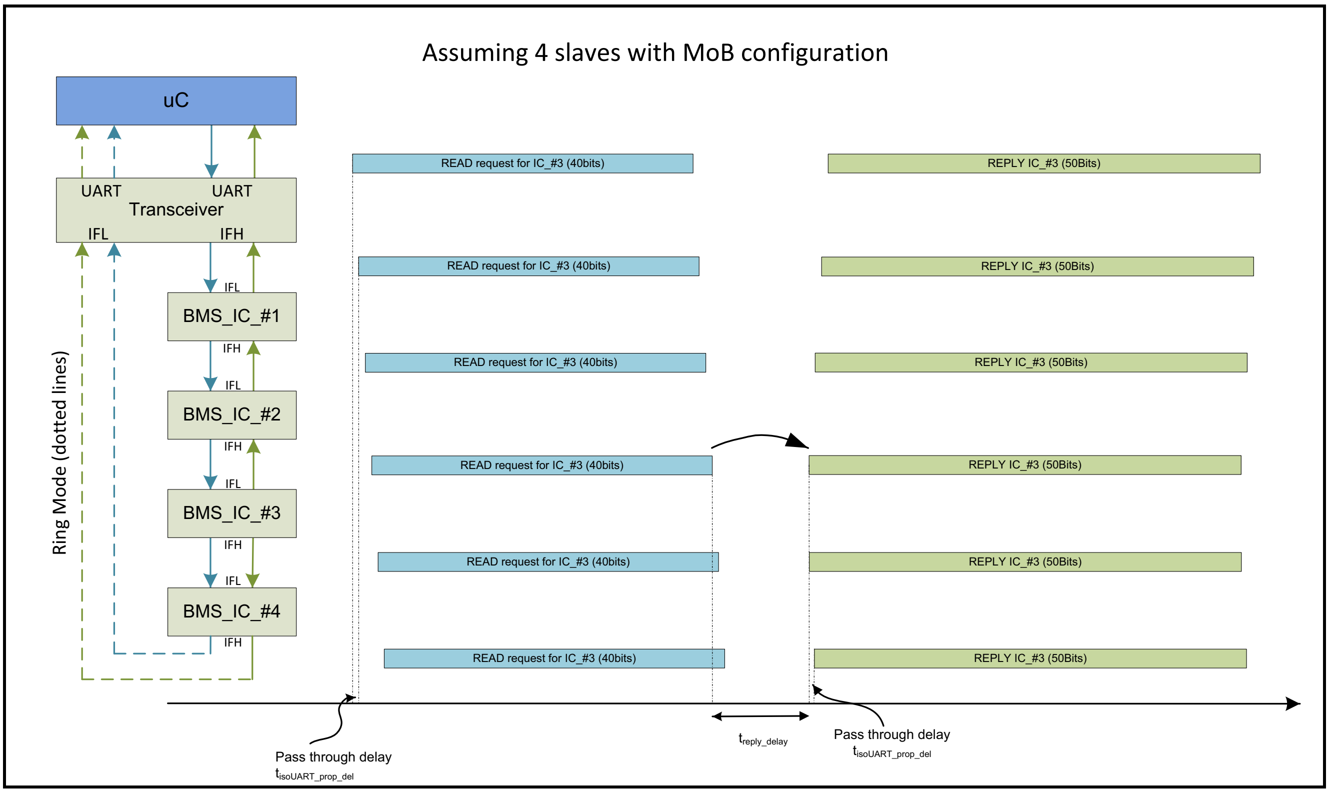


Figure 42 Timing

10.4.1 Electrical characteristics

Table 21 Electrical characteristics

V_{VS} = 4.75 V to 60 V, T_j = -40°C to +150°C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Delay timing							
Reply delay time	t_{reply_delay}	0	1.7	3	µs	[1]	

1) Not subject to production test, specified by design.

11 Built-in diagnosis features

This chapter provides a summary of the built-in diagnosis features of the TLE9012AQU. Furthermore it references to the related registers and bit-fields. There are four different types of diagnosis mechanisms implemented in the TLE9012AQU:

- Periodically triggered diagnosis mechanisms via round robin (please see also chapter **Chapter 8.3**)
- Periodically triggered diagnosis mechanisms with a fixed hardware cycle (please see below)
- Continuous hardware monitoring diagnosis (please see also chapter **Chapter 4.5** and **Chapter 10.3**)
- Manually triggerable diagnosis mechanisms (please see also chapter **Chapter 7**)

The following **Table 22** gives an overview of each built-in diagnosis mechanism mapped to one of the four types from above.

Table 22 Summary of built-in diagnosis mechanisms

Error	Register	Bit-field	State
Periodically triggered mechanism via round robin			
Balancing overcurrent	**GEN_DIAG**	BAL_ERR_OC	IC remains in normal mode. Balancing for affected cell(s) deactivated.
Balancing undercurrent	**GEN_DIAG**	BAL_ERR_UC	IC remains in normal mode. Balancing for affected cell(s) deactivated.
Cell overvoltage	**GEN_DIAG**	CELL_OV	IC remains in normal mode. Balancing for affected cell(s) deactivated.
Cell undervoltage	**GEN_DIAG**	CELL_UV	IC remains in normal mode. Balancing for affected cell(s) deactivated.
Internal overtemperature error	**GEN_DIAG**	INT_OT	IC remains in normal mode. Balancing deactivated
External temperature sensor error	**GEN_DIAG**	EXT_OT	IC remains in normal mode. Balancing deactivated
Open load detection (for all Ux/Gx)	**GEN_DIAG**	OL_ERR	IC remains in normal mode. Balancing deactivated
ADC result (CVM vs. BVM) comparison error	**GEN_DIAG**	ADC_ERR	IC remains in normal mode. Balancing deactivated
Periodically triggered mechanism with fixed hardware cycle			
Register CRC error	**GEN_DIAG**	REG_CRC_ERR	IC remains in normal mode. Balancing deactivated
Internal IC error	**GEN_DIAG**	INT_IC_ERR	IC remains in normal mode. Balancing deactivated.
Continuous hardware monitoring diagnosis			
VREGOUT overcurrent	**GEN_DIAG**	UV_SLEEP	IC goes to sleep mode
Internal supply undervoltage	**GEN_DIAG**	UV_SLEEP	IC goes to sleep mode
VIO undervoltage	**GPIO**	VIO_UV	IC remains in normal mode

Table 22 Summary of built-in diagnosis mechanisms

Error	Register	Bit-field	State
Incoming communication CRC error			IC remains in normal mode. Interfaces changed to default direction
Oscillator drift error detection			IC goes to sleep mode
Manually triggerable diagnosis mechanisms			
NTC source error check via R_{DIAG} measurement		RESULT	
Internal temperature MUX error via internal pull down switches	**AVM_CONFIG**	TEMP_MUX_DIAG_SEL	
External short of neighboring TMP pins via internal pull down switches	**AVM_CONFIG**	TEMP_MUX_DIAG_SEL	

Built-in diagnosis with fixed hardware cycle

There are additional internal checks implemented in the TLE9012AQU. First of all the registers with the following addresses are CRC protected: 01_H, 02_H, 03_H, 04_H, 05_H, 08_H, 09_H, $0A_H$, 14_H, 15_H, 17_H, 36_H, 38_H, $3A_H$. Additionally the internal IC data (e.g. ADC trimming values) is also ECC protected. The register CRC check as well as the internal data check is executed with a fixed hardware cycle time t_{CRC_check} independent of the round robin scheme interval time.

Please note: The register CRC error as well as the internal IC error do not have an error counter.

12 Registers

12.1 Registers overview

Table 23 gives an overview over all registers of the TLE9012AQU. Register fields labelled “RES” (reserved for future use) are as the name indicates reserved for potential future use. When writing into a register, the “RES” part of the register must always be written with “0”. The same applies for read only bit-fields. When reading, the contents of the “RES” fields should be masked out since the value is not defined.

- r = read access
- w = write access
- wo = write access only one time
- h = the IC hardware can change the contents of the field
- rocw = read only, clear bit by writing a “0” to the respective bit position
- rocwl = read only, clear bit by writing a “0”, linked register is reset to default state
- rocr = read only, clearing bit by reading

Table 23 Register Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
Registers overview, Registers description			
PART_CONFIG	Partitioning config (supplied in sleep)	01_H	0800_H
OL_OV_THR	Cell voltage thresholds (supplied in sleep)	02_H	$FFFF_H$
OL_UV_THR	Cell voltage thresholds (supplied in sleep)	03_H	0000_H
TEMP_CONF	Temperature measurement configuration (supplied in sleep)	04_H	0000_H
INT_OT_WARN_CONF	Internal temperature measurement configuration (supplied in sleep)	05_H	0000_H
RR_ERR_CNT	Round Robin ERR counters (supplied in sleep)	08_H	0002_H
RR_CONFIG	Round Robin configuration (supplied in sleep)	09_H	8024_H
FAULT_MASK	ERR pin / EMM mask (supplied in sleep)	$0A_H$	3400_H
GEN_DIAG	General diagnosis (supplied in sleep)	$0B_H$	0000_H
CELL_UV	Cell voltage supervision warning flags UV (supplied in sleep)	$0C_H$	0000_H
CELL_OV	Cell voltage supervision warning flags OV (supplied in sleep)	$0D_H$	0000_H
EXT_TEMP_DIAG	External overtemperature warning flags (supplied in sleep)	$0E_H$	0000_H
DIAG_OL	Diagnosis OPENLOAD (supplied in sleep)	10_H	0000_H
REG_CRC_ERR	REG_CRC_ERR (supplied in sleep)	11_H	0000_H
OP_MODE	Operation mode	14_H	0000_H
BAL_CURR_THR	Balancing current thresholds	15_H	$00AC_H$
BAL_SETTINGS	Balance settings	16_H	0000_H
AVM_CONFIG	Auxiliary Voltage Measurement Configuration	17_H	$001C_H$

Table 23 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
MEAS_CTRL	Measurement control	18_H	0021_H
CVM_0	Cell voltage measurement 0	19_H	0000_H
CVM_1	Cell voltage measurement 1	$1A_H$	0000_H
CVM_2	Cell voltage measurement 2	$1B_H$	0000_H
CVM_3	Cell voltage measurement 3	$1C_H$	0000_H
CVM_4	Cell voltage measurement 4	$1D_H$	0000_H
CVM_5	Cell voltage measurement 5	$1E_H$	0000_H
CVM_6	Cell voltage measurement 6	$1F_H$	0000_H
CVM_7	Cell voltage measurement 3	20_H	0000_H
CVM_8	Cell voltage measurement 8	21_H	0000_H
CVM_9	Cell voltage measurement 9	22_H	0000_H
CVM_10	Cell voltage measurement 10	23_H	0000_H
CVM_11	Cell voltage measurement 11	24_H	0000_H
BVM	Block voltage measurement	28_H	0000_H
EXT_TEMP_0	Temp result 0	29_H	0000_H
EXT_TEMP_1	Temp result 1	$2A_H$	0000_H
EXT_TEMP_2	Temp result 2	$2B_H$	0000_H
EXT_TEMP_3	Temp result 3	$2C_H$	0000_H
EXT_TEMP_4	Temp result 4	$2D_H$	0000_H
EXT_TEMP_R_DIAG	Temp result R Diagnose	$2F_H$	0000_H
INT_TEMP	Chip temperature	30_H	0000_H
MULTI_READ	Multiread command	31_H	0000_H
MULTI_READ_CFG	Multiread Configuration	32_H	0000_H
BAL_DIAG_OC	Passive bal. diagnosis OVERCURRENT	33_H	0000_H
BAL_DIAG_UC	Passive bal. diagnosis UNDERCURRENT	34_H	0000_H
CONFIG	Configuration	36_H	0000_H
GPIO	General purpose input / output	37_H	0000_H
GPIO_PWM	PWM settings	38_H	0000_H
ICVID	IC version and manufacturing ID	39_H	$C101_H$
MAILBOX	Mailbox register	$3A_H$	0000_H
CUSTOMER_ID_0	Customer ID	$3B_H$	0000_H
CUSTOMER_ID_1	Customer ID	$3C_H$	0000_H
WDOG_CNT	Watchdog counter	$3D_H$	$007F_H$

12.1.1 Registers description

PART_CONFIG

PART_CONFIG	**Offset**	**Reset Value**
Partitioning config (supplied in sleep)	**01_H**	**0800_H**

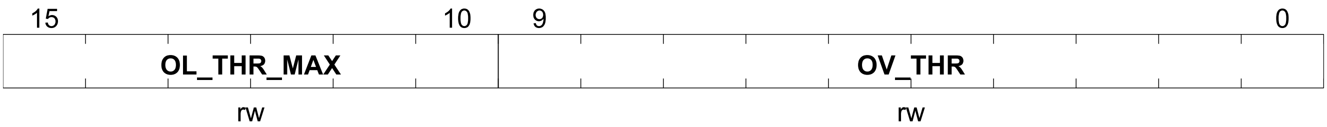
15–12	11	10	9	8	7	6	5	4	3	2	1	0
RES	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*	EN_*
rwh	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 00000_B , not defined (default)
EN_CELL11	11	r	**Enable cell monitoring for cell 11** Please note: Cell 11 must be connected 1_B , cell attached (default)
EN_CELL10	10	rw	**Enable cell monitoring for cell 10** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL9	9	rw	**Enable cell monitoring for cell 9** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL8	8	rw	**Enable cell monitoring for cell 8** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL7	7	rw	**Enable cell monitoring for cell 7** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL6	6	rw	**Enable cell monitoring for cell 6** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL5	5	rw	**Enable cell monitoring for cell 5** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached

Field	Bits	Type	Description
EN_CELL4	4	rw	**Enable cell monitoring for cell 4** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL3	3	rw	**Enable cell monitoring for cell 3** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL2	2	rw	**Enable cell monitoring for cell 2** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL1	1	rw	**Enable cell monitoring for cell 1** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached
EN_CELL0	0	rw	**Enable cell monitoring for cell 0** Please note: Cells must be connected consecutively starting from cell 11 0_B , no cell attached (default) 1_B , cell attached

OL_OV_THR

OL_OV_THR	**Offset**	**Reset Value**
Cell voltage thresholds (supplied in sleep)	**02_H**	**$FFFF_H$**



Field	Bits	Type	Description
OL_THR_MAX	15:10	rw	**Openload maximum voltage drop threshold (LSB10)** 6 bit (LSB10) to define the maximum threshold for the voltage drop while OL-diagnosis (I_{OL_DIAG} * Rf). If dropvoltage > OL_thr_max, the OLx bit of channel x is set. $11\ 1111_B$, threshold (default)
OV_THR	9:0	rw	**Overvoltage fault threshold (LSB10)** 10 bit overvoltage fault threshold. Battery input voltages (U0 to U11) are tested for overvoltage with given value. OV Error is detected and indicated in GEN_DIAG register if cell voltage is HIGHER than OV fault threshold. $11\ 1111\ 1111_B$, threshold (default)

OL_UV_THR

OL_UV_THR	**Offset**	**Reset Value**
Cell voltage thresholds (supplied in sleep)	**03_H**	**0000_H**

15–10	9–0
OL_THR_MIN	UV_THR
rw	rw

Field	Bits	Type	Description
OL_THR_MIN	15:10	rw	**Openload minimum voltage drop threshold (LSB10)** 6 bit (LSB10) to define the minimum threshold for the voltage drop while OL-diagnosis (I_{OL_DIAG} * Rf). If voltage drop < OL_thr_min, the OLx bit of channel x is set. $00\ 0000_B$, threshold (default)
UV_THR	9:0	rw	**Undervoltage fault threshold (LSB10)** 10 bit undervoltage fault threshold. Battery input voltages (U0 to U11) are tested for undervoltage with given value. UV Error is detected and indicated in GEN_DIAG register if cell voltage is LOWER than UV fault threshold. $00\ 0000\ 0000_B$, threshold (default)

TEMP_CONF

TEMP_CONF	**Offset**	**Reset Value**
Temperature measurement configuration (supplied in sleep)	**04_H**	**0000_H**

15	14–12	11–10	9–0
RES	NR_TEMP_S*	I_NTC	EXT_OT_THR
rwh	rw	rw	rw

Field	Bits	Type	Description
RES	15	rwh	**Reserved for future use** 0_B , not defined (default)
NR_TEMP_SENSE	14:12	rw	**Number of external temperature sensors** 000_B , no external TMP sensor (default) 001_B , TMP0 active 010_B , TMP0 + TMP1 active 011_B , TMP0 + TMP1 + TMP 2 active 100_B , TMP0 + TMP1 + TMP 2 + TMP 3 active 101_B , TMP0 + TMP1 + TMP 2 + TMP 3 + TMP 4 active

Field	Bits	Type	Description
I_NTC	11:10	rw	**Current source used for OT fault** 00_B , I_{TMPn_0} used (default) 01_B , I_{TMPn_1} used 10_B , I_{TMPn_2} used 11_B , I_{TMPn_3} used
EXT_OT_THR	9:0	rw	**External temperature overtemperature threshold** 10 bit overtemperature fault threshold. Overtemperature error is detected and indicated in GEN_DIAG register if the RESULT is < EXT_OT_THR. Balancing is deactivated. $00\ 0000\ 0000_B$, threshold (default)

INT_OT_WARN_CONF

INT_OT_WARN_CONF	**Offset**	**Reset Value**
Internal temperature measurement configuration (supplied in sleep)	**05_H**	**0000_H**

15–10	9–0
RES	INT_OT_THR
rwh	rw

Field	Bits	Type	Description
RES	15:10	rwh	**Reserved for future use** $0000\ 00_B$, not defined (default)
INT_OT_THR	9:0	rw	**Internal temperature overtemperature threshold** 10 bit overtemperature fault threshold. Overtemperature error is detected and indicated in GEN_DIAG register if internal temperature result is LOWER than the fault threshold. Balancing is deactivated. $00\ 0000\ 0000_B$, threshold (default)

RR_ERR_CNT

RR_ERR_CNT	**Offset**	**Reset Value**
Round Robin ERR counters (supplied in sleep)	**08_H**	**0002_H**

15–6	5–3	2–0
RR_SLEEP_CNT	NR_EXT_TE*	NR_ERR
rw	rw	rw

Field	Bits	Type	Description
RR_SLEEP_CNT	15:6	rw	**Round Robin timing in sleep mode** 0_B , RR in sleep mode is deactivated (default) 1_B , $t_{RR\_sleep\_LSB}$ $3FF_H$, $t_{RR\_sleep\_LSB}$ *1023
NR_EXT_TEMP_START	5:3	rw	**External temperature triggering in round robin** 0_B , every RR (default) 1_B , 1 RR measurement, 1 RR no measurement 10_B , 1 RR measurement, 2 RR no measurement 11_B , 1 RR measurement, 3 RR no measurement 100_B , 1 RR measurement, 4 RR no measurement 101_B , 1 RR measurement, 5 RR no measurement 110_B , 1 RR measurement, 6 RR no measurement 111_B , 1 RR measurement, 7 RR no measurement
NR_ERR	2:0	rw	**Number of errors** Number of consecutive detected errors before error is valid and set in GEN_DIAG and individual fault registers. Only used for faults where counter NR_ERR is active (this can be set in register NR_ERR_MASK). Please note: The register CRC errors as well as the internal IC errors do not have an error counter. 000_B , 0 001_B , 1 010_B , 2 (default) **...** 111_B , 7

RR_CONFIG

RR_CONFIG **Round Robin configuration (supplied in sleep)**	**Offset** **09_H**	**Reset Value** **8024_H**

15	14	13	12	11	10	9	8	7	6 … 0
M_N*	M_N*	M_N*	M_N*	M_N*	M_N*	M_N*	M_N*	RR_*	RR_CNT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
M_NR_ERR_BAL_OC	15	rw	**mask NR_ERR counter for balancing error overcurrent** 0_B , No masking of NR_ERR. Counter is active 1_B , NR_ERR counter masked. Fault valid after first detection (default)
M_NR_ERR_BAL_UC	14	rw	**mask NR_ERR counter for balancing error undercurrent** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection

Field	Bits	Type	Description
M_NR_ERR_CELL_OV	13	rw	**mask NR_ERR counter for overvoltage error** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection
M_NR_ERR_CELL_UV	12	rw	**mask NR_ERR counter for undervoltage error** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection
M_NR_ERR_INT_OT	11	rw	**mask NR_ERR counter for internal temperature error** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection
M_NR_ERR_EXT_OT	10	rw	**mask NR_ERR counter for external temperature error** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection
M_NR_ERR_OL_ERR	9	rw	**mask NR_ERR counter for open load error** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection
M_NR_ERR_ADC_ERR	8	rw	**mask NR_ERR counter for ADC error** 0_B , No masking of NR_ERR. Counter is active (default) 1_B , NR_ERR counter masked. Fault valid after first detection
RR_SYNC	7	rw	**Round Robin synchronization** 0_B , no synch with WD_CNT write access (default) 1_B , synch with WD_CNT write access (RR will be started by write access, if RR is already running the RR will be restarted from beginning again.)
RR_CNT	6:0	rw	**Round Robin counter** Setting round robin counter (default: 010 0100 ~ 50 ms) 0_H , Round Robin starts every t_{RR_min} $7F_H$, Round Robin starts every t_{RR_max}

FAULT_MASK

FAULT_MASK	**Offset**	**Reset Value**
ERR pin / EMM mask (supplied in sleep)	**$0A_H$**	**3400_H**

15	14	13	12	11	10	9	8	7	6	5	4 … 0
M_B*	M_B*	M_C*	M_C*	M_I*	M_E*	M_R*	M_I*	M_O*	M_A*	ERR*	RES
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rwh

Field	Bits	Type	Description
M_BAL_ERR_OC	15	rw	**EMM/ERR mask for balancing error overcurrent** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error

Field	Bits	Type	Description
M_BAL_ERR_UC	14	rw	**EMM/ERR mask for balancing error undercurrent** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error
M_CELL_OV	13	rw	**EMM/ERR mask for cell overvoltage error** 0_B , ERR/EMM will NOT be set if this type of error occurs 1_B , ERR/EMM will be set for this type of error (default)
M_CELL_UV	12	rw	**EMM/ERR mask for cell undervoltage error** 0_B , ERR/EMM will NOT be set if this type of error occurs 1_B , ERR/EMM will be set for this type of error (default)
M_INT_OT	11	rw	**EMM/ERR mask for internal temperature error** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error
M_EXT_OT	10	rw	**EMM/ERR mask for external temperature error** 0_B , ERR/EMM will NOT be set if this type of error occurs 1_B , ERR/EMM will be set for this type of error (default)
M_REG_CRC_ERR	9	rw	**EMM/ERR mask for register CRC error** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error
M_INT_IC_ERR	8	rw	**EMM/ERR mask for internal IC error** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error
M_OL_ERR	7	rw	**EMM/ERR mask for openload error** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error
M_ADC_ERR	6	rw	**EMM/ERR mask for ADC error** 0_B , ERR/EMM will NOT be set if this type of error occurs (default) 1_B , ERR/EMM will be set for this type of error
ERR_PIN	5	rw	**Enable Error PIN functionality** 0_B , ERR pin deactivated, EMM signal over iso UART active. Device goes back to the mode as it was before the EMM. (default) 1_B , ERR Pin function enabled. Fault indication only via ERR Pin. EMM signal over iso UART deactivated. If ERR PIN triggered, pin stays high (device is then in normal mode) until watchdog runs out or pin is cleared.
RES	4:0	rwh	**Reserved for future use** 00000_B , not defined (default)

GEN_DIAG

GEN_DIAG	**Offset**	**Reset Value**
General diagnosis (supplied in sleep)	**$0B_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BAL*	BAL*	CEL*	CEL*	INT*	EXT*	REG*	INT*	OL_*	ADC*	UV_*	RR_*	LOC*	BAL*	MOT*	GPI*
rocwl	rocwl	rocwl	rocwl	rocw	rocwl	rocwl	rocw	rocwl	rocw	rocw	rh	rh	rh	rh	rh

Field	Bits	Type	Description
BAL_ERR_OC	15	rocwl	**Balancing error overcurrent (will be reset in sleep mode)** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no balancing error. (default) 1_B , balancing error occurred. Detailed information in the respective error register
BAL_ERR_UC	14	rocwl	**Balancing error undercurrent (will be reset in sleep mode)** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no balancing error (default) 1_B , balancing error occurred. Detailed information in the respective error register
CELL_OV	13	rocwl	**Cell overvoltage (OV) error** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no OV error (default) 1_B , OV error occurred. Detailed information in the respective error register
CELL_UV	12	rocwl	**Cell undervoltage (UV) error** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no UV error (default) 1_B , UV error occurred. Detailed information in the respective error register
INT_OT	11	rocw	**Internal temperature (OT) error** 0_B , no internal OT error (default) 1_B , internal OT error occurred. Balancing is deactivated.
EXT_OT	10	rocwl	**External temperature error** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no external OT/OL/Short error (default) 1_B , external OT/OL/Short error occurred. Detailed information in the respective error register. Balancing is deactivated.
REG_CRC_ERR	9	rocwl	**Register CRC error** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no CRC check error (default) 1_B , CRC check error occurred. Detailed information in the respective error register. Balancing is deactivated.

Field	Bits	Type	Description
INT_IC_ERR	8	rocw	**Internal IC error** 0_B , no internal error (default) 1_B , internal IC check error occurred. Balancing is deactivated.
OL_ERR	7	rocwl	**Openload error** Please Note: Resetting the error here resets also the respective detailed error register 0_B , no openload error (default) 1_B , openload error occurred. Detailed information in the respective error register. Balancing is deactivated.
ADC_ERR	6	rocw	**ADC Error** 0_B , no ADC mismatch between sum of CVM and BVM (default) 1_B , ERROR of ADC-result comparison. Balancing is deactivated.
UV_SLEEP	5	rocw	**Undervoltage induced sleep** 0_B , no UV induced sleep (default) 1_B , UV induced sleep occurred
RR_ACTIVE	4	rh	**Round Robin active** This bit indicates if the Round Robin scheduler was active during read. 0_B , no Round Robin active (default) 1_B , Round Robin active
LOCK_MEAS	3	rh	**Lock measurement** This bit indicates an ongoing CVM, BVM or AVM or a delayed RR. 0_B , no measurement ongoing (default) 1_B , CVM, BVM or AVM measurement ongoing
BAL_ACTIVE	2	rh	**Balancing active** 0_B , no balancing ongoing (default) 1_B , balancing ongoing, at least one channel is ON
MOT_MOB_N	1	rh	**Master on Top/Bottom configuration** 0_B , configured as master on bottom (default) 1_B , configured as master on top
GPIO_WAKEUP	0	rh	**Wake-up via GPIO** 0_B , wake-up via iso UART (default) 1_B , wake-up via GPIO

CELL_UV

CELL_UV	Offset	Reset Value
Cell voltage supervision warning flags UV (supplied in sleep)	$0C_H$	0000_H

15–12	11	10	9	8	7	6	5	4	3	2	1	0
RES	UV_*	UV_*	UV_9	UV_8	UV_7	UV_6	UV_5	UV_4	UV_3	UV_2	UV_1	UV_0
rwh	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
UV_11	11	rocw	**Undervoltage in cell 11** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 11 (default) 1_B , undervoltage in cell 11. Balancing is deactivated for this cell.
UV_10	10	rocw	**Undervoltage in cell 10** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 10 (default) 1_B , undervoltage in cell 10. Balancing is deactivated for this cell.
UV_9	9	rocw	**Undervoltage in cell 9** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 9 (default) 1_B , undervoltage in cell 9. Balancing is deactivated for this cell.
UV_8	8	rocw	**Undervoltage in cell 8** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 8 (default) 1_B , undervoltage in cell 8. Balancing is deactivated for this cell.
UV_7	7	rocw	**Undervoltage in cell 7** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 7(default) 1_B , undervoltage in cell 7. Balancing is deactivated for this cell.
UV_6	6	rocw	**Undervoltage in cell 6** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 6(default) 1_B , undervoltage in cell 6. Balancing is deactivated for this cell.
UV_5	5	rocw	**Undervoltage in cell 5** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 5 (default) 1_B , undervoltage in cell 5. Balancing is deactivated for this cell.
UV_4	4	rocw	**Undervoltage in cell 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 4 (default) 1_B , undervoltage in cell 4. Balancing is deactivated for this cell.
UV_3	3	rocw	**Undervoltage in cell 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 3 (default) 1_B , undervoltage in cell 3. Balancing is deactivated for this cell.
UV_2	2	rocw	**Undervoltage in cell 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 2 (default) 1_B , undervoltage in cell 2. Balancing is deactivated for this cell.

Field	Bits	Type	Description
UV_1	1	rocw	**Undervoltage in cell 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 1 (default) 1_B , undervoltage in cell 1. Balancing is deactivated for this cell.
UV_0	0	rocw	**Undervoltage in cell 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no undervoltage in cell 0 (default) 1_B , undervoltage in cell 0. Balancing is deactivated for this cell.

CELL_OV

CELL_OV | **Offset** | **Reset Value**

Cell voltage supervision warning flags OV (supplied in sleep) | **$0D_H$** | **0000_H**

15 … 12	11	10	9	8	7	6	5	4	3	2	1	0
RES	OV_*	OV_*	OV_9	OV_8	OV_7	OV_6	OV_5	OV_4	OV_3	OV_2	OV_1	OV_0
rwh	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
OV_11	11	rocw	**Overvoltage in cell 11** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 11 (default) 1_B , overvoltage in cell 11. Balancing is deactivated for this cell.
OV_10	10	rocw	**Overvoltage in cell 10** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 10 (default) 1_B , overvoltage in cell 10. Balancing is deactivated for this cell.
OV_9	9	rocw	**Overvoltage in cell 9** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 9 (default) 1_B , overvoltage in cell 9. Balancing is deactivated for this cell.
OV_8	8	rocw	**Overvoltage in cell 8** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 8 (default) 1_B , overvoltage in cell 8. Balancing is deactivated for this cell.
OV_7	7	rocw	**Overvoltage in cell 7** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 7 (default) 1_B , overvoltage in cell 7. Balancing is deactivated for this cell.

Field	Bits	Type	Description
OV_6	6	rocw	**Overvoltage in cell 6** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 6 (default) 1_B , overvoltage in cell 6. Balancing is deactivated for this cell.
OV_5	5	rocw	**Overvoltage in cell 5** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 5 (default) 1_B , overvoltage in cell 5. Balancing is deactivated for this cell.
OV_4	4	rocw	**Overvoltage in cell 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 4 (default) 1_B , overvoltage in cell 4. Balancing is deactivated for this cell.
OV_3	3	rocw	**Overvoltage in cell 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 3 (default) 1_B , overvoltage in cell 3. Balancing is deactivated for this cell.
OV_2	2	rocw	**Overvoltage in cell 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 2 (default) 1_B , overvoltage in cell 2. Balancing is deactivated for this cell.
OV_1	1	rocw	**Overvoltage in cell 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 1 (default) 1_B , overvoltage in cell 1. Balancing is deactivated for this cell.
OV_0	0	rocw	**Overvoltage in cell 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overvoltage in cell 0 (default) 1_B , overvoltage in cell 0. Balancing is deactivated for this cell.

EXT_TEMP_DIAG

EXT_TEMP_DIAG	Offset	Reset Value
External overtemperature warning flags (supplied in sleep)	**$0E_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	OT_4	SHO*	OPE*	OT_3	SHO*	OPE*	OT_2	SHO*	OPE*	OT_1	SHO*	OPE*	OT_0	SHO*	OPE*
rwh	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
RES	15	rwh	**Reserved for future use** 0000_B , not defined (default)

Field	Bits	Type	Description
OT_4	14	rocw	**Overtemperature in ext. temp 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overtemperature in ext. temp 4 (default) 1_B , ADC conversion of ext. temp 4 measurement < overtemperature threshold EXT_OT_THR
SHORT_4	13	rocw	**Short in ext. temp 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no short in ext. temp 4 (default) 1_B , short in ext. temp 4
OPEN_4	12	rocw	**Openload in ext. temp 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload in ext. temp 4 (default) 1_B , openload in ext. temp 4
OT_3	11	rocw	**Overtemperature in ext. temp 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overtemperature in ext. temp 3 (default) 1_B , ADC conversion of ext. temp 3 measurement < overtemperature threshold EXT_OT_THR
SHORT_3	10	rocw	**Short in ext. temp 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no short in ext. temp 3 (default) 1_B , short in ext. temp 3
OPEN_3	9	rocw	**Openload in ext. temp 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload in ext. temp 3 (default) 1_B , openload in ext. temp 3
OT_2	8	rocw	**Overtemperature in ext. temp 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overtemperature in ext. temp 2 (default) 1_B , ADC conversion of ext. temp 2 measurement < overtemperature threshold EXT_OT_THR
SHORT_2	7	rocw	**Short in ext. temp 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no short in ext. temp 2 (default) 1_B , short in ext. temp 2
OPEN_2	6	rocw	**Openload in ext. temp 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload in ext. temp 2 (default) 1_B , openload in ext. temp 2
OT_1	5	rocw	**Overtemperature in ext. temp 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overtemperature in ext. temp 1 (default) 1_B , ADC conversion of ext. temp 1 measurement < overtemperature threshold EXT_OT_THR

Field	Bits	Type	Description
SHORT_1	4	rocw	**Short in ext. temp 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no short in ext. temp 1 (default) 1_B , short in ext. temp 1
OPEN_1	3	rocw	**Openload in ext. temp 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload in ext. temp 1 (default) 1_B , openload in ext. temp 1
OT_0	2	rocw	**Overtemperature in ext. temp 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no overtemperature in ext. temp 0 (default) 1_B , ADC conversion of ext. temp 0 measurement < overtemperature threshold EXT_OT_THR
SHORT_0	1	rocw	**Short in ext. temp 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no short in ext. temp 0 (default) 1_B , short in ext. temp 0
OPEN_0	0	rocw	**Openload in ext. temp 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload in ext. temp 0 (default) 1_B , openload in ext. temp 0

DIAG_OL

DIAG_OL **Diagnosis OPENLOAD (supplied in sleep)**	**Offset** **10_H**	**Reset Value** **0000_H**

15–12	11	10	9	8	7	6	5	4	3	2	1	0
RES	OL_*	OL_*	OL_9	OL_8	OL_7	OL_6	OL_5	OL_4	OL_3	OL_2	OL_1	OL_0
rwh	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
OL_11	11	rocw	**Openload in cell 11** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_10	10	rocw	**Openload in cell 10** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel

Field	Bits	Type	Description
OL_9	9	rocw	**Openload in cell 9** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_8	8	rocw	**Openload in cell 8** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_7	7	rocw	**Openload in cell 7** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_6	6	rocw	**Openload in cell 6** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_5	5	rocw	**Openload in cell 5** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_4	4	rocw	**Openload in cell 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_3	3	rocw	**Openload in cell 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_2	2	rocw	**Openload in cell 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_1	1	rocw	**Openload in cell 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel (default) 1_B , openload detected in respective channel
OL_0	0	rocw	**Openload in cell 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no openload detected in respective channel(default) 1_B , openload detected in respective channel

REG_CRC_ERR

REG_CRC_ERR | **Offset** | **Reset Value**
REG_CRC_ERR (supplied in sleep) | **11_H** | **0000_H**

15–7	6–0
RES	ADDR
rwh	rocw

Field	Bits	Type	Description
RES	15:7	rwh	**Reserved for future use** 0 0000 0000_B , not defined (default)
ADDR	6:0	rocw	**Register Address of register where CRC check failed** Register address of CRC check fail, Can also be cleared on write '0' to connected GEN_DIAG register bit 000 0000_B , Register address (default)

OP_MODE

OP_MODE | **Offset** | **Reset Value**
Operation mode | **14_H** | **0000_H**

15–2	1	0
RES	EXT*	PD
rwh	rw	rw

Field	Bits	Type	Description
RES	15:2	rwh	**Reserved for future use** 0000_H , not defined (default)
EXT_WD	1	rw	**Extended watchdog** 0_B , no extended watchdog (default) 1_B , extended watchdog active
PD	0	rw	**Activate sleep mode** 0_B , chip operating in normal mode (default) 1_B , chip is set to sleep mode. No further communication possible after bit is set to '1'

BAL_CURR_THR

BAL_CURR_THR | **Offset** | **Reset Value**
Balancing current thresholds | **15_H** | **$00AC_H$**

15–8	7–0
UC_THR	OC_THR
rw	rw

Field	Bits	Type	Description
UC_THR	15:8	rw	**Undercurrent fault threshold** 8 bit to define the min. voltage drop during balancing diagnosis. If the voltage drop (IBal * Rf) < UC_THR the undercurrent is detected. $0000\ 0000_B$, default
OC_THR	7:0	rw	**Overcurrent fault threshold** 8 bit to define the max. voltage drop during balancing diagnosis. If the voltage drop (IBal * Rf) > OC_THR the overcurrent is detected. $1010\ 1100_B$, default

BAL_SETTINGS

BAL_SETTINGS	**Offset**	**Reset Value**
Balance settings	**16_H**	**0000_H**

15–12	11	10	9	8	7	6	5	4	3	2	1	0
RES	ON_*	ON_*	ON_9	ON_8	ON_7	ON_6	ON_5	ON_4	ON_3	ON_2	ON_1	ON_0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
ON_11	11	rwh	**Switching state of balancing driver 11** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_10	10	rwh	**Switching state of balancing driver 10** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_9	9	rwh	**Switching state of balancing driver 9** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_8	8	rwh	**Switching state of balancing driver 8** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_7	7	rwh	**Switching state of balancing driver 7** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on

Field	Bits	Type	Description
ON_6	6	rwh	**Switching state of balancing driver 6** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_5	5	rwh	**Switching state of balancing driver 5** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_4	4	rwh	**Switching state of balancing driver 4** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_3	3	rwh	**Switching state of balancing driver 3** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_2	2	rwh	**Switching state of balancing driver 2** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_1	1	rwh	**Switching state of balancing driver 1** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on
ON_0	0	rwh	**Switching state of balancing driver 0** 0_B , respective balancing switch off (default) 1_B , respective balancing switch on

AVM_CONFIG

AVM_CONFIG **Auxiliary Voltage Measurement Configuration**	**Offset** **17_H**	**Reset Value** **0007_H**

15–10	9	8	7	6	5	4	3	2–0
RES	R_D*	RES	AVM*	AVM*	AVM*	AVM*	AVM*	TEMP_MUX_*
rwh	rw	rwh	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:10	rwh	**Reserved for future use** 0000 00_B , not defined (default)
R_DIAG	9	rw	**Masking diagnosis resistor as part of AVM** 0_B , manual AVM diagnosis resistor measurement masked out when AVM_START bit triggered (default) 1_B , manual AVM diagnosis resistor measurement performed when AVM_START bit triggered
RES	8	rwh	**Reserved for future use** 0_B , not defined (default)

Field	Bits	Type	Description
AVM_TMP4_MASK	7	rw	**Masking auxiliary measurement via deactive TMP 4 as part of AVM** 0_B , manual AVM TMP4 measurement masked out when AVM_START bit triggered (default) 1_B , manual AVM TMP4 measurement performed when AVM_START bit triggered
AVM_TMP3_MASK	6	rw	**Masking auxiliary measurement via deactive TMP 3 as part of AVM** 0_B , manual AVM TMP3 measurement masked out when AVM_START bit triggered (default) 1_B , manual AVM TMP3 measurement performed when AVM_START bit triggered
AVM_TMP2_MASK	5	rw	**Masking auxiliary measurement via deactive TMP 2 as part of AVM** 0_B , manual AVM TMP2 measurement masked out when AVM_START bit triggered (default) 1_B , manual AVM TMP2 measurement performed when AVM_START bit triggered
AVM_TMP1_MASK	4	rw	**Masking auxiliary measurement via deactive TMP 1 as part of AVM** 0_B , manual AVM TMP1 measurement masked out when AVM_START bit triggered (default) 1_B , manual AVM TMP1 measurement performed when AVM_START bit triggered
AVM_TMP0_MASK	3	rw	**Masking auxiliary measurement via deactive TMP 0 as part of AVM** 0_B , manual AVM TMP0 measurement masked out when AVM_START bit triggered (default) 1_B , manual AVM TMP0 measurement performed when AVM_START bit triggered
TEMP_MUX_DIAG_SEL	2:0	rw	**Selector for ext. temp diagnose** 000_B , pull-down for ext. temp 0 measurement is active 001_B , pull-down for ext. temp 1 measurement is active 010_B , pull-down for ext. temp 2 measurement is active 011_B , pull-down for ext. temp 3 measurement is active 100_B , pull-down for ext. temp 4 measurement is active 111_B , No pull-down active (default)

MEAS_CTRL

MEAS_CTRL	**Offset**	**Reset Value**
Measurement control	**18_H**	**0021_H**

15	14:12	11	10:8	7	6	5	4:0
CVM*	CVM_BIT_W*	BVM*	BVM_BIT_W*	AVM*	RES	PBO*	CVM_DEL
rwh	rw	rwh	rw	rwh	rwh	rw	rw

Field	Bits	Type	Description
CVM_START	15	rwh	**Start cell voltage measurement** Bit cleared if conversion done 0_B , no measurement ongoing (default) 1_B , trigger measurement
CVM_BIT_WIDTH	14:12	rw	**Bit width of cell voltage measurement** 0_B , 10 bit (default) 1_B , 11 bit 110_B , 16 bit
BVM_START	11	rwh	**Start block voltage measurement** Bit cleared if conversion done 0_B , no measurement ongoing (default) 1_B , trigger measurement
BVM_BIT_WIDTH	10:8	rw	**Bit width of block voltage measurement** 0_B , 10 bit (default) 1_B , 11 bit 110_B , 16 bit
AVM_START	7	rwh	**Start auxiliary voltage measurement** Bit cleared if conversion done 0_B , no measurement ongoing (default) 1_B , trigger measurement, if BVM_START=0
RES	6	rwh	**Reserved for future use** 0_B , not defined (default)
PBOFF	5	rw	**Enable PBOFF time** 0_B , keep balancing state for CVM / BVM 1_B , switch off balancing before conversion starts (default)
CVM_DEL	4:0	rw	**CVM delay timer** Wait for CVM_DEL before CVM and/or BVM is started 0_B , no settling time 1_B , $t_{CVM\_del\_LSB}$ (default) 11111_B , $\times t_{CVM\_del\_LSB}$

CVM_0

CVM_0	**Offset**	**Reset Value**
Cell voltage measurement 0	**19_H**	**0000_H**

15		0
	RESULT	
	rh	

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 0** 0000_H , default

CVM_1

CVM_1 **Cell voltage measurement 1**	**Offset** **$1A_H$**	**Reset Value** **0000_H**

15		0
	RESULT	
	rh	

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 1** 0000_H , default

CVM_2

CVM_2 **Cell voltage measurement 2**	**Offset** **$1B_H$**	**Reset Value** **0000_H**

15		0
	RESULT	
	rh	

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 2** 0000_H , default

CVM_3

CVM_3 | **Offset** | **Reset Value**
Cell voltage measurement 3 | **$1C_H$** | **0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 3** 0000_H , default

CVM_4

CVM_4 | **Offset** | **Reset Value**
Cell voltage measurement 4 | **$1D_H$** | **0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 4** 0000_H , default

CVM_5

CVM_5 | **Offset** | **Reset Value**
Cell voltage measurement 5 | **$1E_H$** | **0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 5** 0000_H , default

CVM_6

CVM_6	**Offset**	**Reset Value**
Cell voltage measurement 6	**$1F_H$**	**0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 6** 0000_H , default

CVM_7

CVM_7	**Offset**	**Reset Value**
Cell voltage measurement 7	**20_H**	**0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 7** 0000_H , default

CVM_8

CVM_8	**Offset**	**Reset Value**
Cell voltage measurement 8	**21_H**	**0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 8** 0000_H , default

CVM_9

CVM_9 **Cell voltage measurement 9**	**Offset** **22_H**	**Reset Value** **0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 9** 0000_H , default

CVM_10

CVM_10 **Cell voltage measurement 10**	**Offset** **23_H**	**Reset Value** **0000_H**

15 … 0
RESULT
rh

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 10** 0000_H , default

CVM_11

CVM_11 **Cell voltage measurement 11**	**Offset** **24_H**	**Reset Value** **0000_H**

15		0
RESULT		
rh		

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of cell voltage measurement 11** 0000_H , default

BVM

BVM — **Offset** — **Reset Value**
Block voltage measurement — **28_H** — **0000_H**

15		0
RESULT		
rh		

Field	Bits	Type	Description
RESULT	15:0	rh	**Result of block voltage measurement** 0000_H , default

EXT_TEMP_0

EXT_TEMP_0 — **Offset** — **Reset Value**
Temp result 0 — **29_H** — **0000_H**

15 14	13	12	11 10	9 ... 0
RES	VAL*	PUL*	INTC	RESULT
rwh	rocr	rh	rh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available (default) 1_B , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_0 register

Field	Bits	Type	Description
PULLDOWN	12	rh	**Indicating pull-down switch state** 0_B , normal measurement done (default) 1_B , pull-down for Mux-test was active during conversion
INTC	11:10	rh	**Indicates which current source was used** number of current source that was active for latest measurement 00_B , source I_{TMP0_0} used (default) 01_B , source I_{TMP0_1} used 10_B , source I_{TMP0_2} used 11_B , source I_{TMP0_3} used
RESULT	9:0	rh	**Result of ext. temp 0 measurement** SD-ADC result of resistance or voltage measurement. 000_H , (default)

EXT_TEMP_1

EXT_TEMP_1	**Offset**	**Reset Value**
Temp result 1	**$2A_H$**	**0000_H**

15–14	13	12	11–10	9–0
RES	VAL*	PUL*	INTC	RESULT
rwh	rocr	rh	rh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available 1_B , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_1 register
PULLDOWN	12	rh	**Indicating pull-down switch state** 0_B , normal measurement done 1_B , pull-down for Mux-test was active during conversion
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement 00_B , source I_{TMP1_0} used (default) 01_B , source I_{TMP1_1} used 10_B , source I_{TMP1_2} used 11_B , source I_{TMP1_3}used
RESULT	9:0	rh	**Result of ext. temp 1 measurement** SD-ADC result of resistance or voltage measurement. 000_H , default

EXT_TEMP_2

EXT_TEMP_2	**Offset**	**Reset Value**
Temp result 2	**$2B_H$**	**0000_H**

15:14	13	12	11:10	9:0
RES	VAL*	PUL*	INTC	RESULT
rwh	rocr	rh	rh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available 1_B , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_2 register
PULLDOWN	12	rh	**Indicating pull-down switch state** 0_B , normal measurement done 1_B , pull-down for Mux-test was active during conversion
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement 00_B , source I_{TMP0_0}used (default) 01_B , source I_{TMP0_1} used 10_B , source I_{TMP0_1} used 11_B , source I_{TMP0_3} used
RESULT	9:0	rh	**Result of ext. temp 2 measurement** SD-ADC result of resistance or voltage measurement. 000_H , default

EXT_TEMP_3

EXT_TEMP_3	**Offset**	**Reset Value**
Temp result 3	**$2C_H$**	**0000_H**

15:14	13	12	11:10	9:0
RES	VAL*	PUL*	INTC	RESULT
rwh	rocr	rh	rh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)

Field	Bits	Type	Description
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available 1_B , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_3 register
PULLDOWN	12	rh	**Indicating pull-down switch state** 0_B , normal measurement done 1_B , pull-down for Mux-test was active during conversion
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement 00_B , source I_{TMP1_0} used (default) 01_B , source I_{TMP1_1} used 10_B , source I_{TMP1_2} used 11_B , source I_{TMP1_3} used
RESULT	9:0	rh	**Result of ext. temp 3 measurement** SD-ADC result of resistance or voltage measurement. 000_H , default

EXT_TEMP_4

EXT_TEMP_4	**Offset**	**Reset Value**
Temp result 4	**$2D_H$**	**0000_H**

15 14	13	12	11 10	9 … 0
RES	VAL*	PUL*	INTC	RESULT
rwh	rocr	rh	rh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available 1_B , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_4 register
PULLDOWN	12	rh	**Indicating pull-down switch state** 0_B , normal measurement done 1_B , pull-down for Mux-test was active during conversion
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement 00_B , source I_{TMPn_0} used (default) 01_B , source I_{TMPn_0} used 10_B , source I_{TMPn_0} used 11_B , source I_{TMPn_0} used

Field	Bits	Type	Description
RESULT	9:0	rh	**Result of ext. temp 4 measurement** SD-ADC result of resistance or voltage measurement. 000_H , default

EXT_TEMP_R_DIAG

EXT_TEMP_R_DIAG	**Offset**	**Reset Value**
Temp result R Diagnose	**$2F_H$**	**0000_H**

15 14	13	12	11 10	9 … 0
RES	VAL*	RES	INTC	RESULT
rwh	rocr	rwh	rh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available 1_B , a new result is stored in the register, cleared automatically after readout of the EXT_TEMP_R_DIAG register
RES	12	rwh	**Reserved for future use** 0_B , not defined (default)
INTC	11:10	rh	**Indicates which current source was used** Number of current source that was active for latest measurement 00_B , source I_{TMP0_0} used (default) 01_B , source I_{TMP0_1} used 10_B , source I_{TMP0_2} used 11_B , source I_{TMP0_3} used
RESULT	9:0	rh	**Result of diagnosis resistor measurement** SD-ADC result 000_H , default

INT_TEMP

INT_TEMP	**Offset**	**Reset Value**
Chip temperature	**30_H**	**0000_H**

15 14	13	12 … 10	9 … 0
RES	VAL*	RES	RESULT
rwh	rocr	rwh	rh

Field	Bits	Type	Description
RES	15:14	rwh	**Reserved for future use** 00_B , not defined (default)
VALID	13	rocr	**Indicating a valid result** 0_B , no new result available (default) 1_B , a new result is stored in the register, cleared automatically after readout of the INT_TEMP register
RES	12:10	rwh	**Reserved for future use** 000_B , not defined (default)
RESULT	9:0	rh	**Result of internal temperature measurement** SD-ADC result of internal temperature measurement. 000_H , default

MULTI_READ

MULTI_READ	**Offset**	**Reset Value**
Multiread command	**31_H**	**0000_H**

15 ... 0
UNDEFINED
rh

Field	Bits	Type	Description
UNDEFINED	15:0	rh	**Used in combination with MULTI_READ_CFG** Reading this register by the host starts the multiple register read routine which got define in the MULTI_READ_CFG register 0000_H , not defined (default)

MULTI_READ_CFG

MULTI_READ_CFG	**Offset**	**Reset Value**
Multiread Configuration	**32_H**	**0000_H**

15–10	9	8	7–5	4	3–0
RES	INT*	EXT*	EXT_TEMP_*	BVM*	CVM_SEL
rwh	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RES	15:10	rwh	**Reserved for future use** 00_H , not defined (default)

Field	Bits	Type	Description
INT_TEMP_SEL	9	rw	**Selects if INT_TEMP result is part of the multiread** 0_B , no INT_TEMP result (default) 1_B , result of INT_TEMP
EXT_TEMP_R_SEL	8	rw	**Selects if R_DIAG result is part of the multiread** 0_B , no R_DIAG result (default) 1_B , result of R_DIAG
EXT_TEMP_SEL	7:5	rw	**Selects which TEMP result is part of the multiread** 0_B , no TEMP result (default) 1_B , result of TEMP 0 10_B , result of TEMP 0 & TEMP 1 11_B , result of TEMP 0 & TEMP 1 & TEMP 2 100_B , result of TEMP 0 & TEMP 1 & TEMP 2 & TEMP 3 101_B , result of TEMP 0 & TEMP 1 & TEMP 2 & TEMP 3 & TEMP 4
BVM_SEL	4	rw	**Selects if BVM result is part of the multiread** 0_B , no BVM result (default) 1_B , result of BVM
CVM_SEL	3:0	rw	**Selects which CVM results are part of the multiread** 0_B , no CVM result (default) 1_B , only result of Cell 11 10_B , results of Cell 11- 10 11_B , results of Cell 11- 9 1100_B , results of cell 11- 0 $1101...1111_B$, no CVM result

BAL_DIAG_OC

BAL_DIAG_OC	**Offset**	**Reset Value**
Passive bal. diagnosis OVERCURRENT	**33_H**	**0000_H**

15–12	11	10	9	8	7	6	5	4	3	2	1	0
RES	OC_*	OC_*	OC_9	OC_8	OC_7	OC_6	OC_5	OC_4	OC_3	OC_2	OC_1	OC_0
rwh	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
OC_11	11	rocw	**Balancing overcurrent in cell 11** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.

Field	Bits	Type	Description
OC_10	10	rocw	**Balancing overcurrent in cell 10** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_9	9	rocw	**Balancing overcurrent in cell 9** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_8	8	rocw	**Balancing overcurrent in cell 8** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_7	7	rocw	**Balancing overcurrent in cell 7** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_6	6	rocw	**Balancing overcurrent in cell 6** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_5	5	rocw	**Balancing overcurrent in cell 5** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.

Field	Bits	Type	Description
OC_4	4	rocw	**Balancing overcurrent in cell 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_3	3	rocw	**Balancing overcurrent in cell 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_2	2	rocw	**Balancing overcurrent in cell 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_1	1	rocw	**Balancing overcurrent in cell 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.
OC_0	0	rocw	**Balancing overcurrent in cell 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing overcurrent detected in respective cell (default) 1_B , balancing overcurrent detected in respective cell. Balancing is deactivated for this cell.

BAL_DIAG_UC

BAL_DIAG_UC **Offset** **Reset Value**
Passive bal. diagnosis UNDERCURRENT **34_H** **0000_H**

15–12	11	10	9	8	7	6	5	4	3	2	1	0
RES	UC_*	UC_*	UC_9	UC_8	UC_7	UC_6	UC_5	UC_4	UC_3	UC_2	UC_1	UC_0
rwh	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw	rocw

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
UC_11	11	rocw	**Balancing undercurrent in cell 11** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_10	10	rocw	**Balancing undercurrent in cell 10** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_9	9	rocw	**Balancing undercurrent in cell 9** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_8	8	rocw	**Balancing undercurrent in cell 8** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_7	7	rocw	**Balancing undercurrent in cell 7** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_6	6	rocw	**Balancing undercurrent in cell 6** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.

Field	Bits	Type	Description
UC_5	5	rocw	**Balancing undercurrent in cell 5** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_4	4	rocw	**Balancing undercurrent in cell 4** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_3	3	rocw	**Balancing undercurrent in cell 3** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_2	2	rocw	**Balancing undercurrent in cell 2** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_1	1	rocw	**Balancing undercurrent in cell 1** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.
UC_0	0	rocw	**Balancing undercurrent in cell 0** Can also be cleared on write '0' to connected GEN_DIAG register bit 0_B , no balancing undercurrent detected in respective cell (default) 1_B , balancing undercurrent detected in respective cell. Balancing is deactivated for this cell.

CONFIG

CONFIG | **Offset** | **Reset Value**
Configuration | **36_H** | **0000_H**

15:12	11	10	9	8:6	5:0
RES	FN	RES	EN_*	RES	NODE_ID
rwh	rwo	rwh	rwo	rwh	rwo

Field	Bits	Type	Description
RES	15:12	rwh	**Reserved for future use** 0000_B , not defined (default)
FN	11	rwo	**Final Node** The final node in stack must have this bit set. If the final node does not have FN set, no reply frame on broadcast will be sent -> iso UART time-out. 0_B , not the final node (default) 1_B , final node
RES	10	rwh	**Reserved for future use** 0_B , not defined (default)
EN_ALL_ADC	9	rwo	**Enable all ADCs** If this bit is set CVM is done for each channel independent of PART_CONFIG setup. But the results are only available for the cells activated in PART_CONFIG 0_B , only ADCs enabled which are defined in PART_CONFIG as active cell 1_B , all ADCs enabled
RES	8:6	rwh	**Reserved for future use** 000_B , not defined (default)
NODE_ID	5:0	rwo	**Address (ID) of the node, distributed during enumeration** NODE_ID = 0 --> iso UART signals are not forwarded NODE_ID = 63 --> reserved for broadcast commands 000000_B , (default)

GPIO

GPIO | **Offset** | **Reset Value**
General purpose input / output | **37_H** | **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIO*	RES	DIR*	OUT*	PWM*	IN_*	DIR*	OUT*	PWM*	IN_*	DIR*	OUT*	IN_*	DIR*	OUT*	IN_*
rocw	rwh	rw	rw	rw	rh	rw	rw	rw	rh	rw	rw	rh	rw	rw	rh

Field	Bits	Type	Description
VIO_UV	15	rocw	**VIO undervoltage error (supplied in sleep)** 0_B , no VIO undervoltage error (default) 1_B , VIO undervoltage error occurred
RES	14	rwh	**Reserved for future use** 0_B , not defined (default)
DIR_PWM0	13	rw	**PWM 0 direction** 0_B , input (output stage = HiZ) (default) 1_B , output (output stage enabled)
OUT_PWM0	12	rw	**PWM 0 output setting** 0_B , drive L (default) 1_B , drive H
PWM_PWM0	11	rw	**PWM 0 enable PWM function** 0_B , no PWM function (default) 1_B , if DIR_PWM0 = 1, then PWM output regarding PWM_GPIO register and OUT_PWM0 is ignored. If DIR_PWM0 = 0, GPIO input and no PWM function.
IN_PWM0	10	rh	**PWM 0 input state** 0_B , pin reads L (default) 1_B , pin reads H Also active for DIR_PWM0 = 1 (reading back driven value)
DIR_PWM1	9	rw	**PWM 1 direction** 0_B , input (output stage = HiZ) (default) 1_B , output (output stage enabled)
OUT_PWM1	8	rw	**PWM 1 output setting** 0_B , drive L (default) 1_B , drive H
PWM_PWM1	7	rw	**PWM 1 enable PWM function** 0_B , no PWM function (default) 1_B , if DIR_PWM1 = 1, then PWM output regarding PWM_GPIO register and OUT_PWM1 is ignored. If DIR_PWM1 = 0, GPIO input and no PWM function.
IN_PWM1	6	rh	**PWM 1 input state** 0_B , pin reads L (default) 1_B , pin reads H Also active for DIR_PWM1 = 1 (reading back driven value)
DIR_GPIO1	5	rw	**GPIO 1 direction (ignored if communication over GPIO pins)** 0_B , input (output stage = HiZ) (default) 1_B , output (output stage enabled)
OUT_GPIO1	4	rw	**GPIO 1 output setting (ignored if communication over GPIO pins)** 0_B , drive L (default) 1_B , drive H

Field	Bits	Type	Description
IN_GPIO1	3	rh	**GPIO 1 input state (ignored if communication over GPIO pins)** 0_B , pin reads L (default) 1_B , pin reads H Also active for DIR_GPIO1 = 1 (reading back driven value)
DIR_GPIO0	2	rw	**GPIO 0 direction (ignored if communication over GPIO pins)** 0_B , input (output stage = HiZ) (default) 1_B , output (output stage enabled)
OUT_GPIO0	1	rw	**GPIO 0 output setting (ignored if communication over GPIO pins)** 0_B , drive L (default) 1_B , drive H
IN_GPIO0	0	rh	**GPIO 0 input state (ignored if communication over GPIO pins)** 0_B , pin reads L (default) 1_B , pin reads H Also active for DIR_GPIO0 = 1 (reading back driven value)

GPIO_PWM

GPIO_PWM	**Offset**	**Reset Value**
PWM settings	**38_H**	**0000_H**

15–13	12–8	7–5	4–0
RES	PWM_PERIOD	RES	PWM_DUTY_CYCLE
rwh	rw	rwh	rw

Field	Bits	Type	Description
RES	15:13	rwh	**Reserved for future use** 000_B , not defined (default)
PWM_PERIOD	12:8	rw	**PWM period time setting** 2 us - 62 µs 00000_B , no PWM (default) 00001_B , 2 µs 00010_B , 4 µs **...** 11111_B , 62 µs
RES	7:5	rwh	**Reserved for future use** 000_B , not defined (default)

Field	Bits	Type	Description
PWM_DUTY_CYCLE	4:0	rw	**PWM duty cycle** 0 - 100% 00000_B , no PWM (default) 00001_B , 3.57% 00010_B , 7.14% **...** 11100_B , 100% **...** 11111_B , 100%

ICVID

ICVID — **Offset** — **Reset Value**

IC version and manufacturing ID — **39_H** — **$C110_H$**

15 … 8	7 … 0
MANUFACTURER_ID	VERSION_ID
rh	rh

Field	Bits	Type	Description
MANUFACTURER_ID	15:8	rh	**Manufacturer ID** Read only manufacture ID 11000001_B , default
VERSION_ID	7:0	rh	**Version ID** Read only version ID 00010000_B , default

MAILBOX

MAILBOX — **Offset** — **Reset Value**

Mailbox register — **$3A_H$** — **0000_H**

15 … 0
DATA
rw

Field	Bits	Type	Description
DATA	15:0	rw	**Data storage register** 2 data byte data storage 0000_H , (default)

CUSTOMER_ID_0

CUSTOMER_ID_0	Offset	Reset Value
Customer ID	$3B_H$	0000_H

15 … 0
DATA
rh

Field	Bits	Type	Description
DATA	15:0	rh	**Reserved for potential unique ID part 1** 0000_H , (default)

CUSTOMER_ID_1

CUSTOMER_ID_1	Offset	Reset Value
Customer ID	$3C_H$	0000_H

15 … 0
DATA
rh

Field	Bits	Type	Description
DATA	15:0	rh	**Reserved for potential unique ID part 2** 0000_H , (default)

WDOG_CNT

WDOG_CNT	Offset	Reset Value
Watchdog counter	$3D_H$	$007F_H$

15 … 7	6 … 0
MAIN_CNT	WD_CNT
rh	rwh

Field	Bits	Type	Description
MAIN_CNT	15:7	rh	**Main counter** Used to enable µC to measure main oscillator frequency. LSB = t_{count_LSB} 0 0000 0000$_B$, (default)
WD_CNT	6:0	rwh	**Watchdog counter (LP oscillator)** 0$_B$, device goes to sleep 1$_B$, t_{WD_LSB} (EXT_WD = 0) 1$_B$, $t_{WD\_EXT\_LSB}$ (EXT_WD = 1) 111 1111$_B$, t_{WD_LSB} * 127 (EXT_WD = 0) (default) 111 1111$_B$, $t_{WD\_EXT\_LSB}$ * 127 (EXT_WD = 1)

13 Application information

Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the circuit must be verified in the real application. Please ask for the Application Note regarding Application Information for more details.

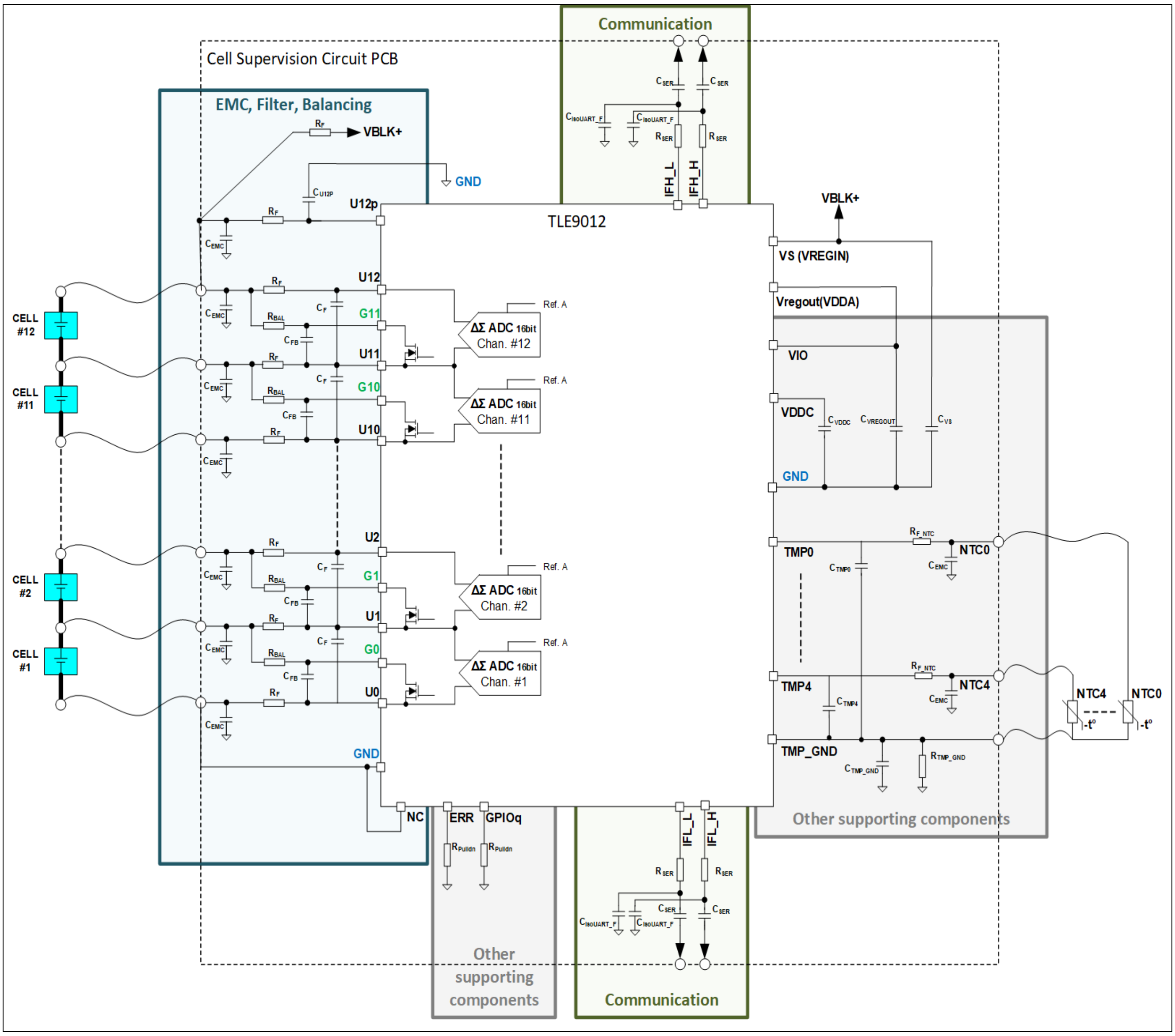


Figure 43 Application circuitry example

Note: Hot-plug and EMC robustness is dependent on used PCB components and PCB routing.

14 Package outlines

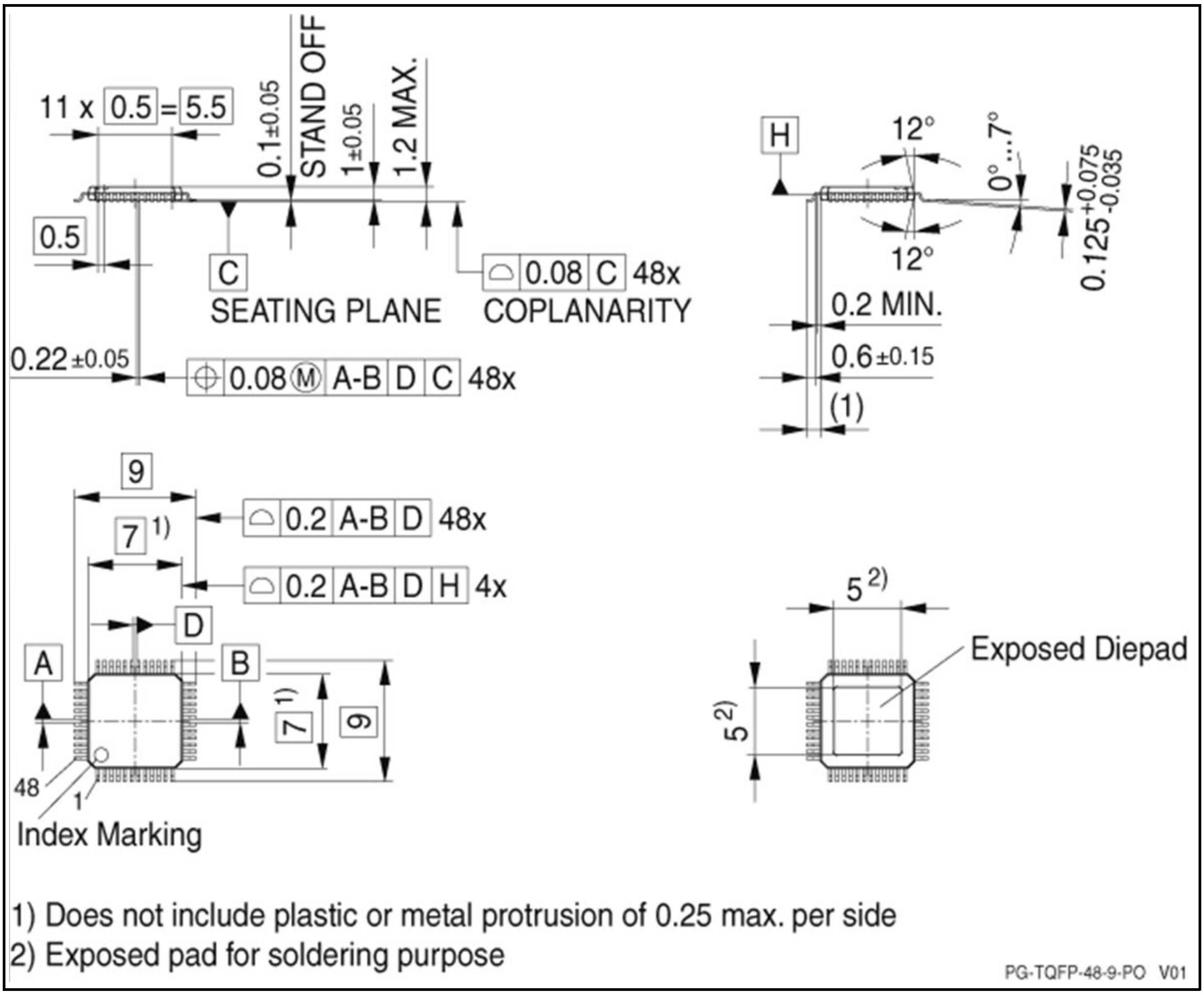


Figure 44 Package outlines and footprint PG-TQFP-48

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

15 Revision history

Revision	Date	Changes
1.1	2020-06-09	Editorial changes **Table 2** Cell sense input voltages rel. Un: max. limit increased **Table 8** Minor parameter adjustment **Table 11** Sink current for open load diagnosis: max. limit decreased
1.0	2019-12-13	Initial Datasheet

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