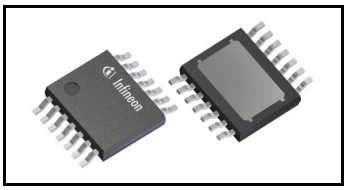
TLE94003EP



Features

- Three half bridge power outputs
- Very low power consumption in sleep mode
- 3.3V / 5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Direct interface for control and diagnosis
- Overtemperature protection
- Over- and Undervoltage lockout
- Cross-current protection

Potential applications

- HVAC Flap DC motors
- Monostable and bistable relays
- Side mirror x-y adjustment

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100

Description

The TLE94003EP is a protected triple half-bridge driver designed especially for automotive motion control applications such as side mirror x-y adjustment. It is part of a larger family offering half-bridge drivers from three outputs to twelve outputs with direct interface or SPI interface.

The half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a direct interface. It offers diagnosis features such as short circuit, power supply failure and overtemperature detection. In combination with its low quiescent current, this device is attractive among others for automotive applications. The small fine pitch exposed pad package, PG-TSDSO-14, provides good thermal performance and reduces PCB-board space and costs.

Type	Package	Marking
TLE94003EP	PG-TSDSO-14	TLE94003

Table 1 Product Summary

Operating Voltage	V_S	5.5 ... 20 V
Logic Supply Voltage	V_{DD}	3.0 ... 5.5 V
Maximum Supply Voltage for Load Dump Protection	$V_{S(LD)}$	40 V
Minimum Overcurrent Threshold	I_{SD}	0.9 A
Maximum On-State Path Resistance at T_j = 150°C	$R_{DSON(total)\_HSx+LSy}$	1.8 + 1.8 Ω
Typical Quiescent Current at T_j = 85°C	I_{SQ}	0.1 µA

Table of Contents

1 Pin Configuration

1.1 Pin Assignment

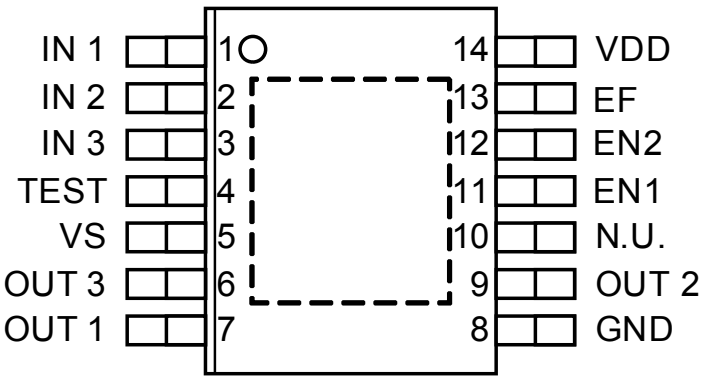


Figure 1 Pin Configuration TLE94003EP with direct interface

1.2 Pin Definitions and Functions

Pin	Symbol	Function
1	IN1	Direct input control for power half-bridge 1
2	IN2	Direct input control for power half-bridge 2
3	IN3	Direct input control for power half-bridge 3
4	TEST	Test input. This pin can be left open or be terminated to ground
5	VS	Main supply voltage for power half bridges.
6	OUT 3	Power half-bridge 3
7	OUT 1	Power half-bridge 1
8	GND	Ground
9	OUT 2	Power half-bridge 2
10	N.U.	Not used. This pin should either be left open or terminated to ground.
11	EN1	Enable input for Half-bridges 1/2 with internal pull-down
12	EN2	Enable input for Half-bridge 3 with internal pull-down
13	EF	Error Flag
14	VDD	Logic supply voltage
EDP	-	Exposed Die Pad; For cooling and EMC purposes only - not usable as electrical ground. Electrical ground must be provided by pins 8. [1)]

1) The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB. The exposed pad (EP) must be either left open or connected to GND. It is recommended to connect EP to GND for best EMC and thermal performance.

Pin Configuration

Note: Not used (N.U.) pins and unused outputs are recommended to be left unconnected (open) on the application board. If N.U. pins or unused output pins are routed to an external connector which leaves the PCB, then these outputs should have provision for a zero ohm jumper (depopulated if unused) or ESD protection. In other words, they should be treated like used pins.

2 Block Diagram

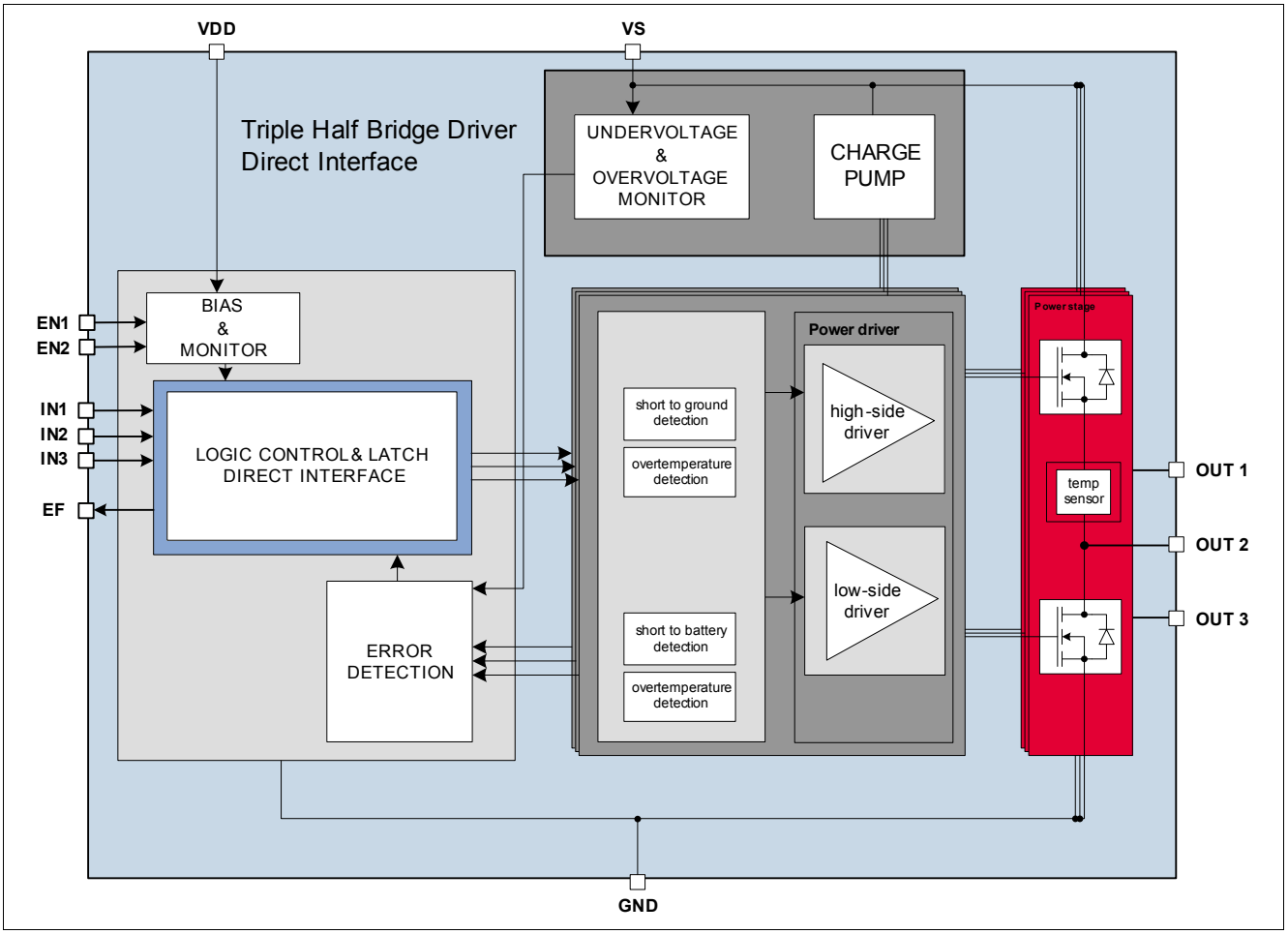


Figure 2 Block Diagram TLE94003EP (Direct Interface)

2.1 Voltage and current definition

Figure 3 shows terms used in this datasheet, with associated convention for positive values.

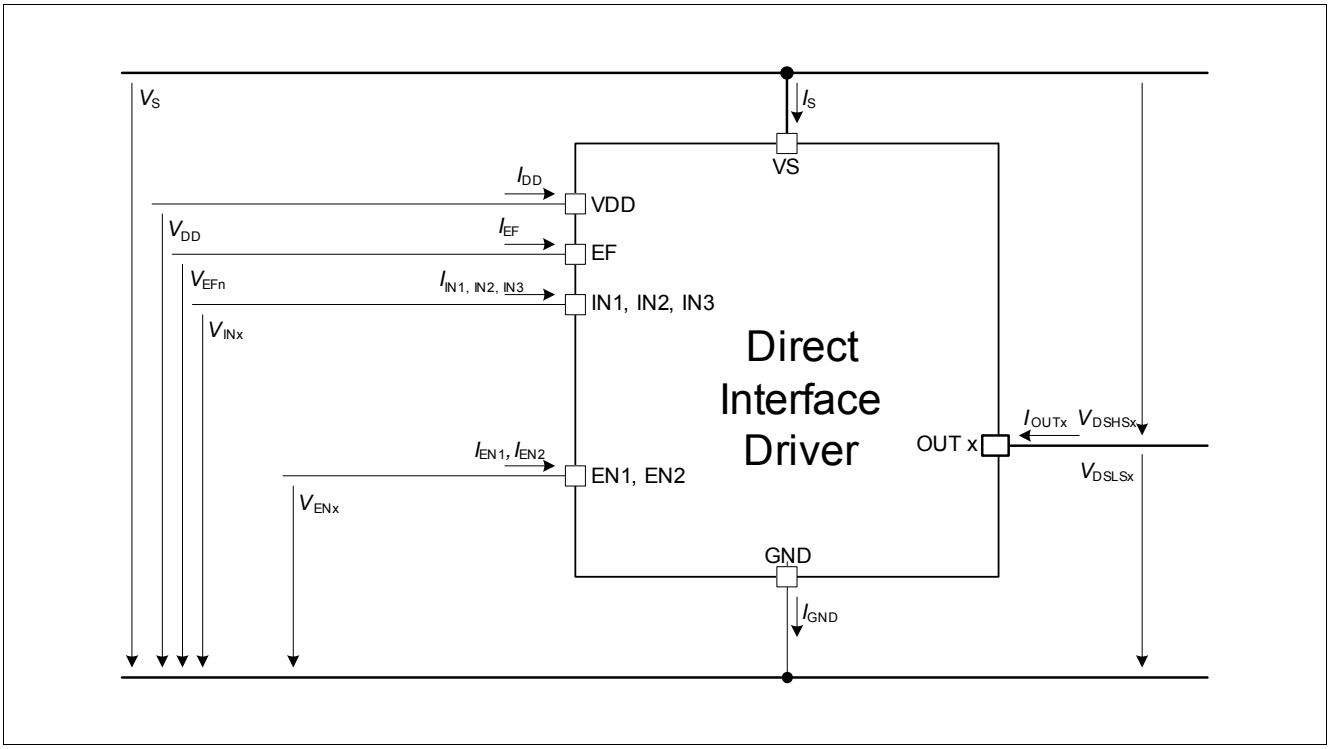


Figure 3 Voltage and Current Definition

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings[1] T_j = -40°C to +150°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V		P_4.1.1
Supply Voltage Slew Rate	$\lvert dV_S/dt \rvert$	–	–	10	V/µs	V_S increasing and decreasing [1]	P_4.2.2
Power half-bridge output voltage	V_{OUT}	-0.3	–	40	V	0 V < V_{OUT} < V_S [2]	P_4.1.2
Logic supply voltage	V_{DD}	-0.3	–	5.5	V	0 V < V_S < 40 V	P_4.1.3
Logic input voltages (EN1, EN2, IN1, IN2, IN3)	V_{ENn}, V_{INn}	-0.3	–	VDD	V	0 V < V_S < 40 V 0 V < V_{DD} < 5.5V	P_4.1.16
Logic output voltage (EF)	V_{EF}	-0.3	–	VDD	V	0 V < V_S < 40 V 0 V < V_{DD} < 5.5V	P_4.1.17
Currents							
Continuous Supply Current for V_S	I_S	0	–	1.5	A	–	P_4.1.20
Current per GND pin	I_{GND}	0	–	2.0	A	–	P_4.1.14
Output Currents	I_{OUT}	-2.0	–	2.0	A	–	P_4.1.15
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.8
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.9
ESD Susceptibility							
ESD susceptibility OUTn and VS pins versus GND. All other pins grounded.	V_{ESD}	-4	–	4	kV	JEDEC HBM[1)3)]	P_4.1.10
ESD susceptibility all pins	V_{ESD}	-2	–	2	kV	JEDEC HBM[1)3)]	P_4.1.11
ESD susceptibility all pins	V_{ESD}	-500	–	500	V	CDM[1)4)]	P_4.1.12
ESD susceptibility corner pins	V_{ESD}	-750	–	750	V	CDM[1)4)]	P_4.1.13

1) Not subject to production test, specified by design
2) Also applicable to not used (N.U.) pins
3) ESD susceptibility, “JEDEC HBM” according to ANSI/ ESDA/ JEDEC JS001 (1.5 kΩ, 100pF)
4) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional Range

Table 3 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	5.5	–	20	V	–	P_4.2.1
Logic supply voltage range for normal operation	V_{DD}	3.0	–	5.5	V	–	P_4.2.3
Logic input voltages (EN1, EN2, IN1, IN2, IN3)	V_{INn}, V_{ENn}	-0.3	–	5.5	V	–	P_4.2.6
Junction temperature	T_j	-40	–	150	°C		P_4.2.5

Note: Within the normal functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal Resistance

Table 4 Thermal Resistance TLE94003EP

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case, T_A = -40°C	R_{thjC_cold}	–	16	–	K/W	1)	
Junction to Case, T_A = 85°C	R_{thjC_hot}	–	19	–	K/W	1)	
Junction to ambient, T_A = -40°C (1s0p, minimal footprint)	$R_{thjA\_cold\_min}$	–	136	–	K/W	1) 2)	
Junction to ambient, T_A = 85°C (1s0p, minimal footprint)	$R_{thjA\_hot\_min}$	–	148	–	K/W	1) 2)	
Junction to ambient, T_A = -40°C (1s0p, 300mm2 Cu)	$R_{thjA\_cold\_300}$	–	79	–	K/W	1) 3)	
Junction to ambient, T_A = 85°C (1s0p, 300mm2 Cu)	$R_{thjA\_hot\_300}$	–	95	–	K/W	1) 3)	
Junction to ambient, T_A = -40°C (1s0p, 600mm2 Cu)	$R_{thjA\_cold\_600}$	–	77	–	K/W	1) 4)	
Junction to ambient, T_A = 85°C (1s0p, 600mm2 Cu)	$R_{thjA\_hot\_600}$	–	94	–	K/W	1) 4)	
Junction to ambient, T_A = -40°C (2s2p)	$R_{thjA\_cold\_2s2p}$	–	63	–	K/W	1) 5)	
Junction to ambient, T_A = 85°C (2s2p)	$R_{thjA\_hot\_2s2p}$	–	82	–	K/W	1) 5)	

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with minimal footprint copper area and 35µm thickness. Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

3) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 300mm2 copper area and 35µm thickness. Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

4) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 1s0p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with additional cooling of 600mm2 copper area and 35µm thickness. Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

5) Specified R_{thJA} value is according to JEDEC JESD51-2, -3 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 x 114.3 x 1.5mm board with two inner copper layers (4 x 35µm Cu). Ta = -40°C, each channel dissipates 0.2W. Ta = 85°C, each channel dissipates 0.135W.

3.4 Electrical Characteristics

Table 5 Electrical Characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN1= HIGH and EN2= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption, EN1 = EN2 = GND							
Supply Quiescent current	I_{SQ}	–	0.1	2	µA	-40°C ≤ T_j ≤ 85°C	P_4.4.1
Logic supply quiescent current	I_{DD_Q}	–	0.1	1	µA	-40°C ≤ T_j ≤ 85°C	P_4.4.2
Total quiescent current	I_{SQ} + I_{DD_Q}	–	0.6	3	µA	-40°C ≤ T_j ≤ 85°C	P_4.4.3
Current Consumption, EN=HIGH							
Supply current	I_{S_HSON}	–	1.5	3	mA	All high-sides ON[1)2)]	P_4.4.101
Logic supply current	I_{DD}	–	0.6	2.5	mA		P_4.4.5
Over- and Undervoltage Lockout							
Undervoltage Switch ON voltage threshold	$V_{UV\ ON}$	4.4	4.90	5.3	V	V_S increasing	P_4.4.8
Undervoltage Switch OFF voltage threshold	$V_{UV\ OFF}$	4	4.50	4.9	V	V_S decreasing	P_4.4.9
Undervoltage Switch ON/OFF hysteresis	$V_{UV\ HY}$	–	0.40	–	V	$V_{UV\ ON}$ - $V_{UV\ OFF}$ [2)]	P_4.4.10
Overvoltage Switch OFF voltage threshold	$V_{OV\ OFF}$	21	23	25	V	V_S increasing	P_4.4.11
Overvoltage Switch ON voltage threshold	$V_{OV\ ON}$	20	22	24	V	V_S decreasing	P_4.4.12
Overvoltage Switch ON/OFF hysteresis	$V_{OV\ HY}$	–	1	–	V	$V_{OV\ OFF}$ - $V_{OV\ ON}$ [2)]	P_4.4.13
V_{DD} Power-On-Reset	$V_{DD\ POR}$	2.40	2.63	2.90	V	V_{DD} increasing	P_4.4.14
V_{DD} Power-Off-Reset	$V_{DD\ POffR}$	2.35	2.57	2.85	V	V_{DD} decreasing	P_4.4.15
V_{DD} Power ON/OFF hysteresis	$V_{DD\ POR\ HY}$	–	0.06	–	V	$V_{DD\ POR}$ - $V_{DD\ POffR}$ [2)]	P_4.4.98
Static Drain-source ON-Resistance (High-Side or Low-Side)							
High-Side or Low-Side R_{DSON} (all outputs)	$R_{DSON\_HB\_25C}$	–	825	1200	mΩ	I_{OUT} = ±0.5 A; T_j = 25 °C	P_4.4.16
High-Side or Low-Side R_{DSON} (all outputs)	$R_{DSON\_HB\_150C}$	–	1350	1800	mΩ	I_{OUT} = ±0.5 A; T_j = 150 °C	P_4.4.17
Output Protection and Diagnosis of high-side (HS) channels of half-bridge output							
HS Overcurrent Shutdown Threshold	I_{SD_HS}	-1.5	-1.2	-0.9	A	See **Figure 7**	P_4.4.20
Difference between shutdown and limit current	I_{LIM_HS} - I_{SD_HS}	-1.2	-0.6	0	A	[2)] $\|I_{LIM\_HS}\| \geq \|I_{SD\_HS}\|$ See **Figure 7**	P_4.4.21

Table 5 Electrical Characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN1= HIGH and EN2= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overcurrent Shutdown filter time	t_{dSD_HS}	15	19	23	µs	2)	P_4.4.22
Output Protection and Diagnosis of low-side (LS) channels of half-bridge output							
LS Overcurrent Shutdown Threshold	I_{SD_LS}	0.9	1.2	1.5	A	See **Figure 8**	P_4.4.27
Difference between shutdown and limit current	I_{LIM_LS} - I_{SD_LS}	0	0.6	1.2	A	2) $I_{LIM\_LS} \geq I_{SD\_LS}$ **Figure 8**	P_4.4.28
Overcurrent Shutdown filter time	t_{dSD_LS}	15	19	23	µs	2)	P_4.4.29
Outputs OUT(1...n) leakage current							
HS leakage current in off state	I_{QLHn_NOR}	-2	-0.5	–	µA	V_{OUTn} = 0V ; OUT1/2: EN1=GND, EN2=High; OUT3: EN1=High,EN2=GND	P_4.4.32
HS leakage current in off state	I_{QLHn_SLE}	-2	-0.5	–	µA	V_{OUTn} = 0V; EN1 = EN2 =GND	P_4.4.33
LS Leakage current in off state	I_{QLLn_NOR}	–	0.5	2	µA	V_{OUTn} = V_S ; OUT1/2: EN1=GND, EN2=High; OUT3: EN1=High,EN2=GND	P_4.4.34
LS Leakage current in off state	I_{QLLn_SLE}	–	0.5	2	µA	V_{OUTn} = V_S ; EN1 = EN2 =GND	P_4.4.35
Output Switching Times. See Figure 9 and Figure 10.							
Slew rate of high-side and low-side outputs	d_{VOUT}/dt	0.1	0.45	0.75	V/µs	Resistive load = 100Ω; V_S=13.5V 3)	P_4.4.36
Output delay time high side driver on	t_{dONH}	5	20	35	µs	Resistive load = 100Ω to GND	P_4.4.37
Output delay time high side driver off	t_{dOFFH}	15	45	75	µs	Resistive load = 100Ω to GND	P_4.4.38
Output delay time low side driver on	t_{dONL}	5	20	35	µs	Resistive load = 100Ω to VS	P_4.4.39
Output delay time low side driver off	t_{dOFFL}	15	45	75	µs	Resistive load = 100Ω to VS	P_4.4.40
Cross current protection time, high to low	t_{DHL}	100	130	160	µs	Resistive load = 100Ω2)	P_4.4.41
Cross current protection time, low to high	t_{DLH}	100	130	160	µs	Resistive load = 100Ω2)	P_4.4.42

Table 5 Electrical Characteristics, V_S =5.5 V to 20 V, V_{DD} = 3.0V to 5.5V, T_j = -40°C to +150°C, EN1= HIGH and EN2= HIGH, I_{OUTn}= 0 A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V and T_J = 25 °C unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified) (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input Interface: Logic Inputs EN1, EN2							
Set up time after sleep mode	t_{SET_DI}	–	–	150	µs	2) See **Figure 5**	P_4.4.49
High-input voltage	V_{ENH}	0.7 * V_{DD}	–	V_{DD}	V	–	P_4.4.43
Low-input voltage	V_{ENL}	0	–	0.3 * V_{DD}	V	–	P_4.4.44
Hysteresis of input voltage	V_{ENHY}	–	500	–	mV	2)	P_4.4.45
Pull down resistor	R_{PD_EN}	20	40	70	kΩ	V_{EN} = 0.2 x V_{DD}	P_4.4.46
EF reset time	t_{EF_RESET}	250	–	–	ns	2) Set ENx to Low for t_{EF_RESET} to reset EF	P_4.4.121
Input Interface: Logic Inputs IN1, IN2, IN3							
High input voltage threshold	V_{INnH}	0.7 * V_{DD}	–	V_{DD}	V	–	P_4.4.90
Low input voltage threshold	V_{INnL}	0	–	0.3 * V_{DD}	V	–	P_4.4.91
Hysteresis of input voltage	V_{INnHY}	–	500	–	mV	2)	P_4.4.92
Pull-down resistor	R_{PD}	20	40	70	kΩ	–	P_4.4.94
Output Interface: Logic Output EF							
High output voltage level	V_{EFH}	V_{DD} - 0.4	V_{DD} - 0.2	V_{DD}	V	I_{EFH} = -1.6 mA	P_4.4.88
Low output voltage level	V_{EFL}	0	0.2	0.4	V	I_{EFL} = 1.6 mA	P_4.4.95
Leakage current	I_{EFLK}	-1	–	1	µA	0V < V_{EF} < 5.5V	P_4.4.96
Thermal Shutdown							
Thermal shutdown junction temperature	T_{jSD}	160	175	190	°C	See **Figure 11** 2)	P_4.4.81
Thermal comparator hysteresis	T_{jHYS}	–	4	–	°C	2)	P_4.4.82

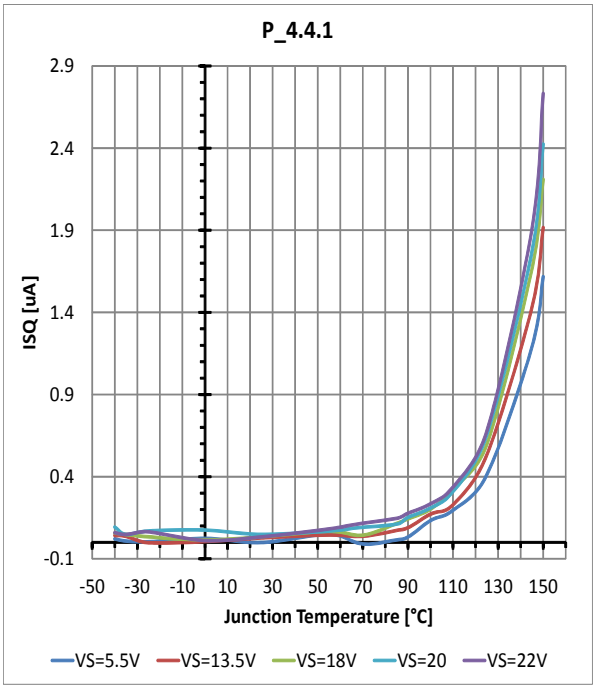
1) I_{S_HSON} does not include the load current
2) Not subject to production test, specified by design
3) Measured for 20% - 80% of V_S.

4 Characterization results

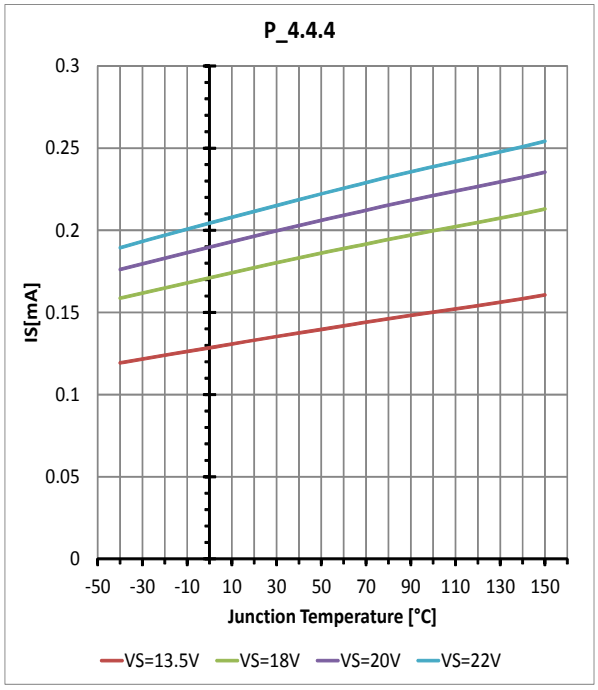
Performed on 5 devices, over operating temperature and nominal/extended supply range.

Typical performance characteristics

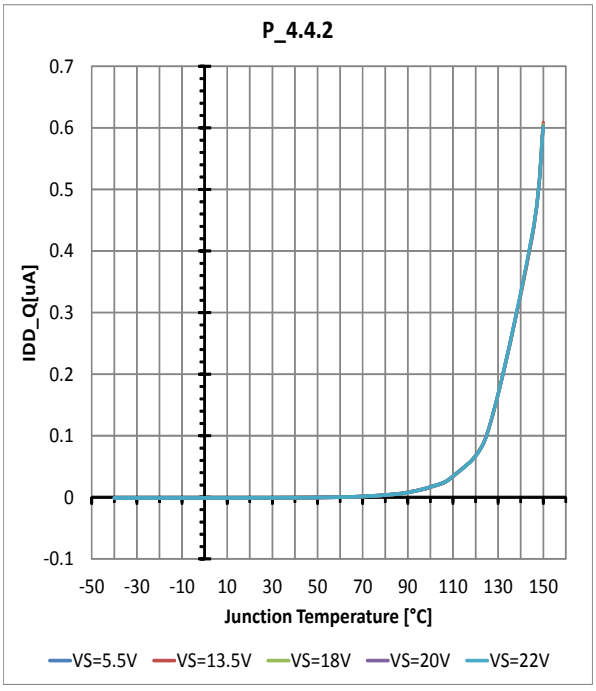
Supply quiescent current



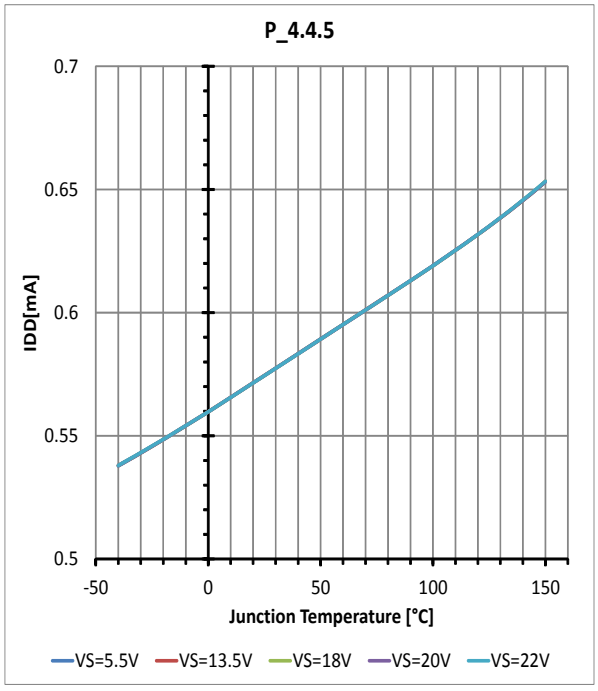
Supply current



Logic supply quiescent current

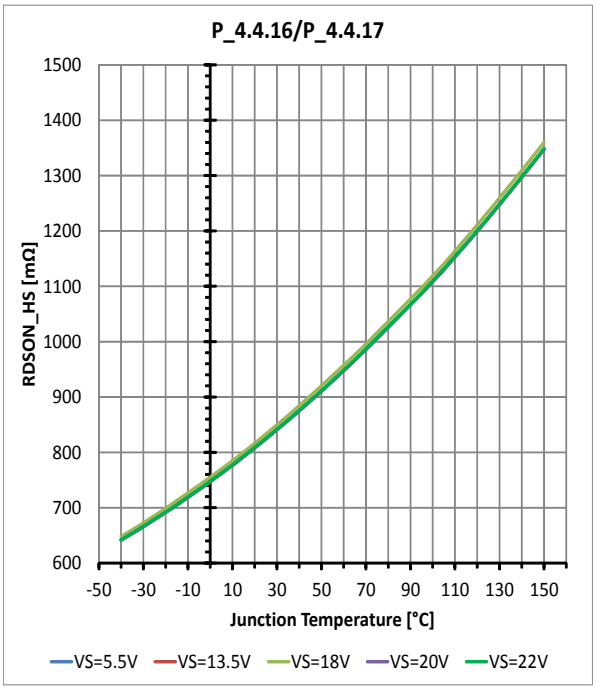


Logic supply current

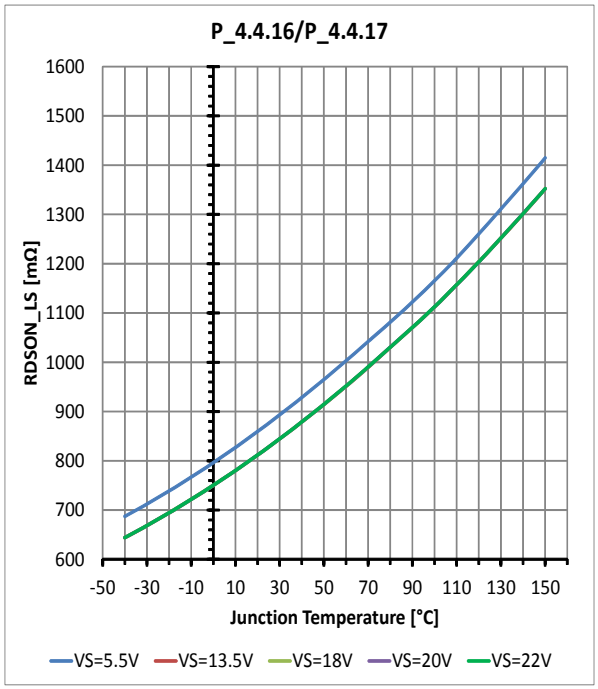


Characterization results

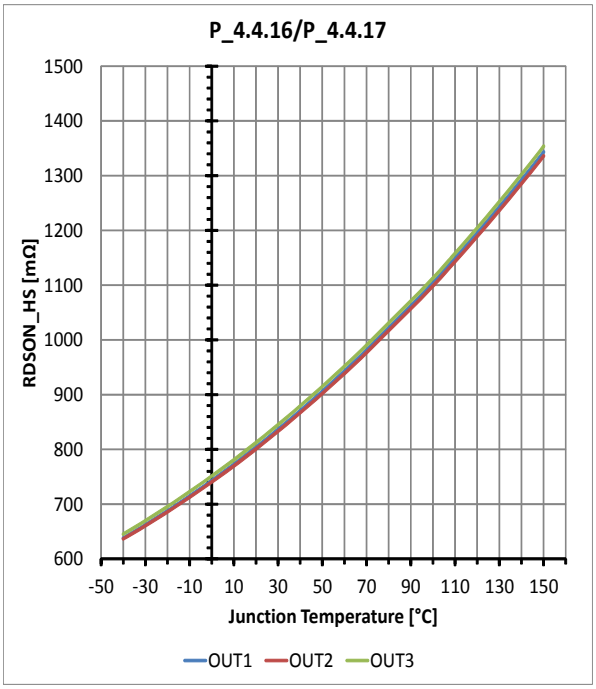
HS static Drain-source ON-resistance



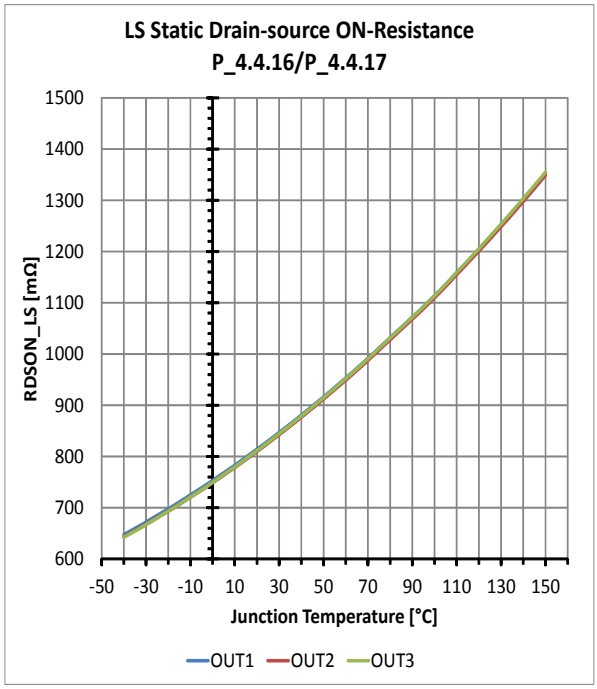
LS static Drain-source ON-resistance



HS static drain-source ON-resistance VS = 13.5V and VDD = 5V

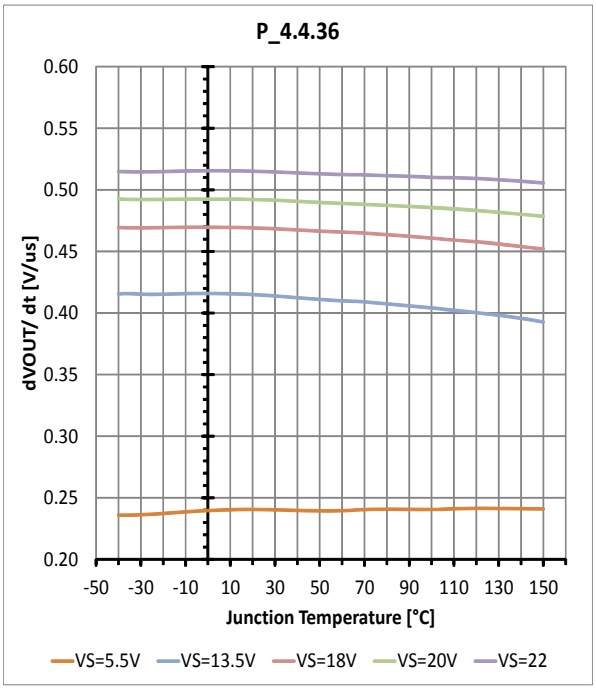


LS static drain-source ON-resistance VS = 13.5V and VDD = 5V

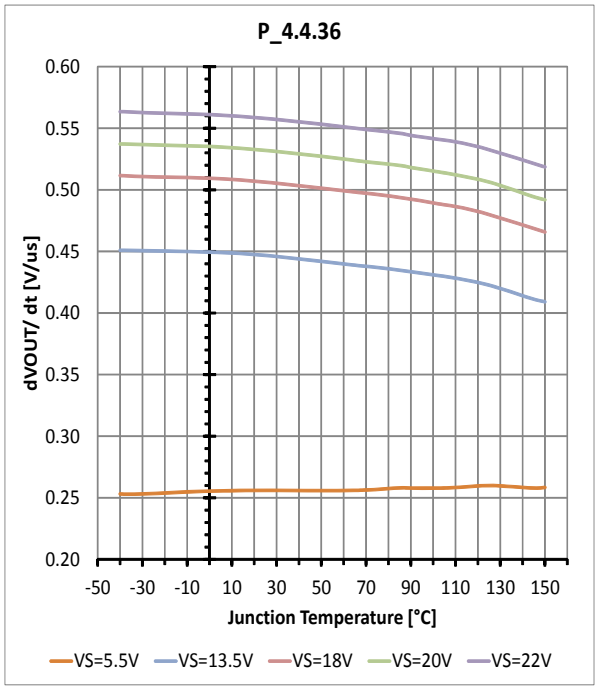


Characterization results

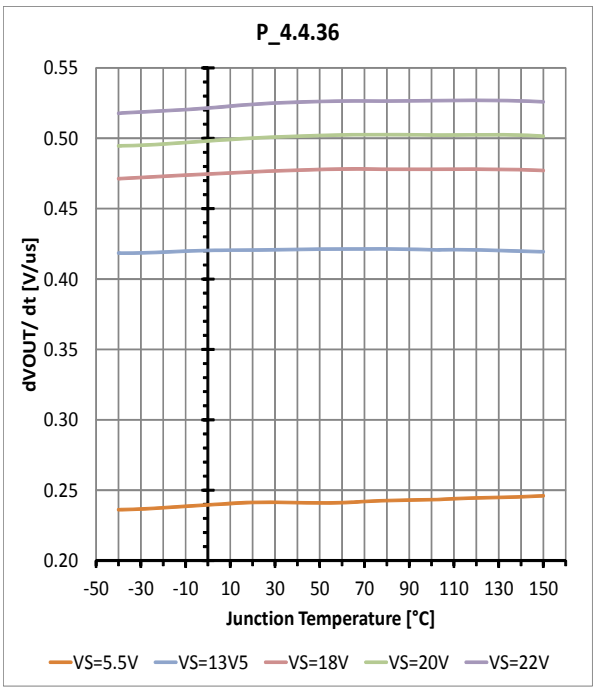
Slew rate ON of high-side outputs



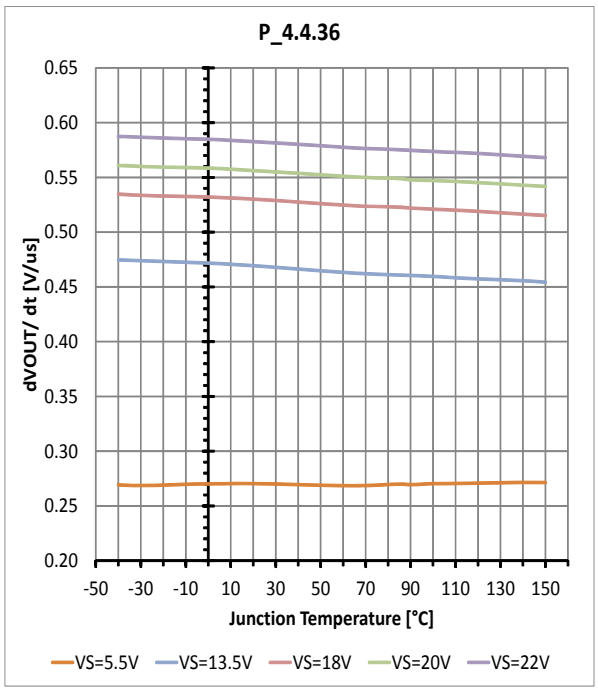
Slew rate ON of low-side outputs



Slew rate OFF of high-side outputs

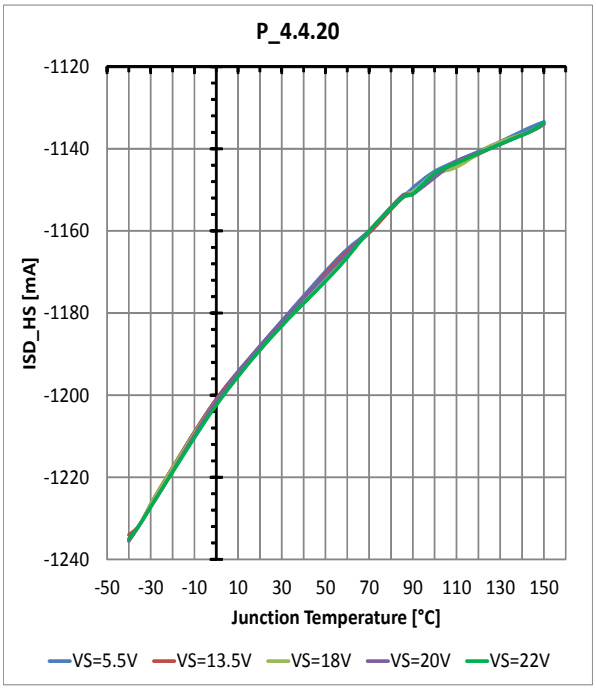


Slew rate OFF of low-side outputs

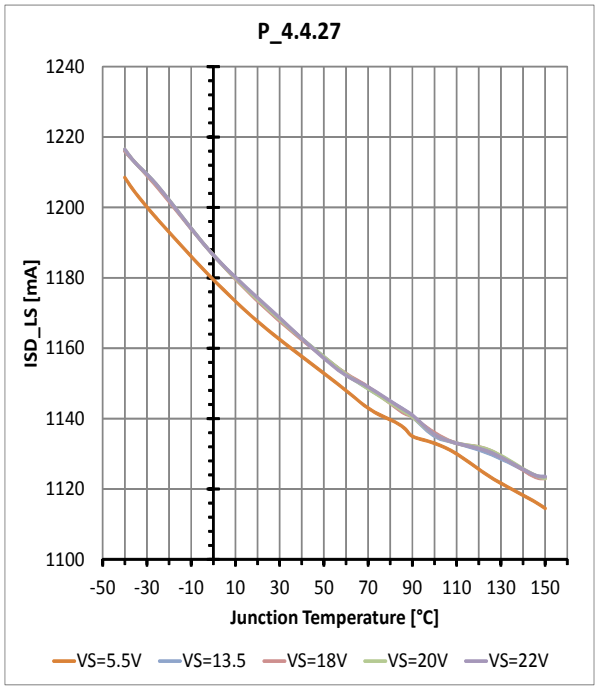


Characterization results

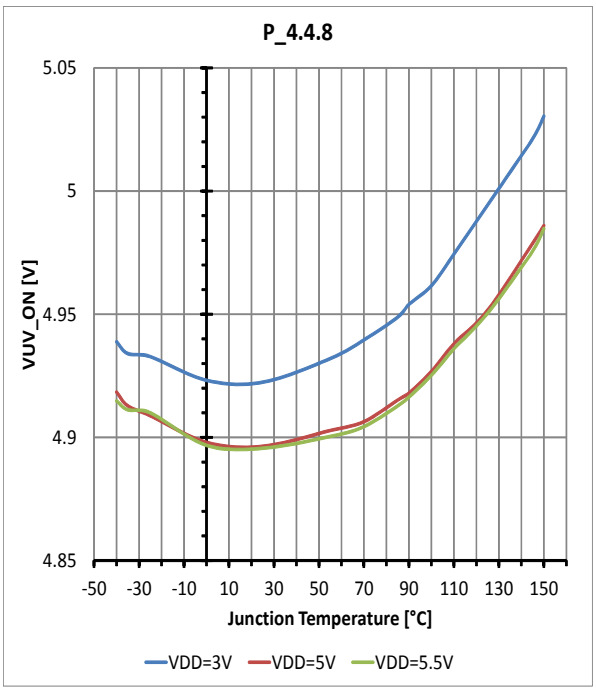
HS overcurrent shutdown threshold



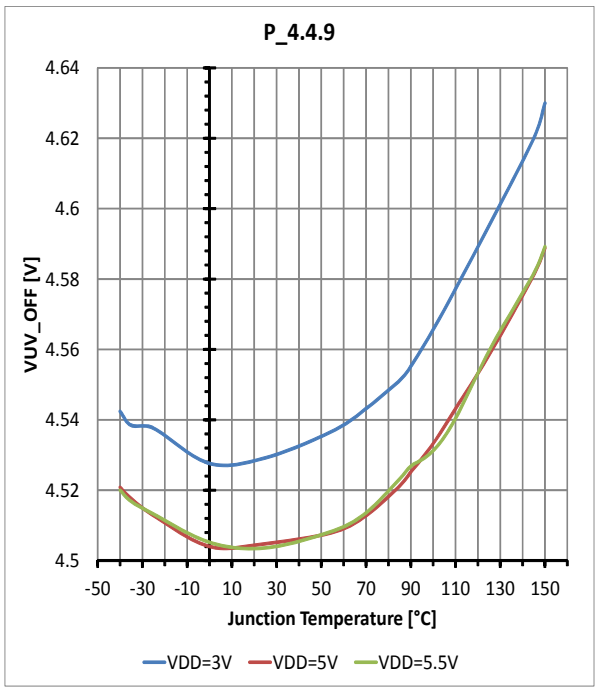
LS overcurrent shutdown threshold



Undervoltage switch ON voltage threshold

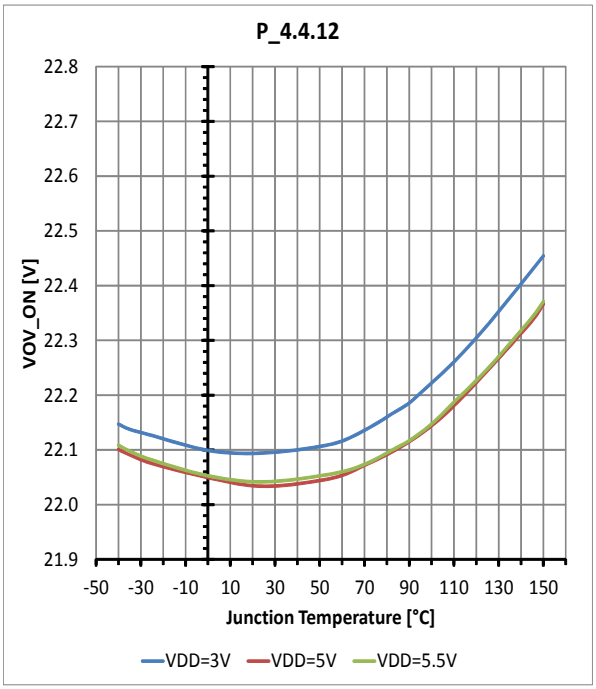


Undervoltage switch OFF voltage threshold

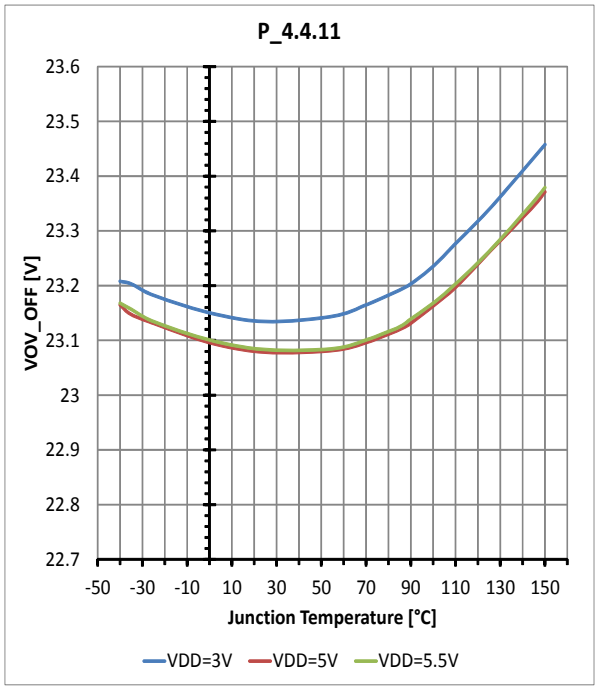


Characterization results

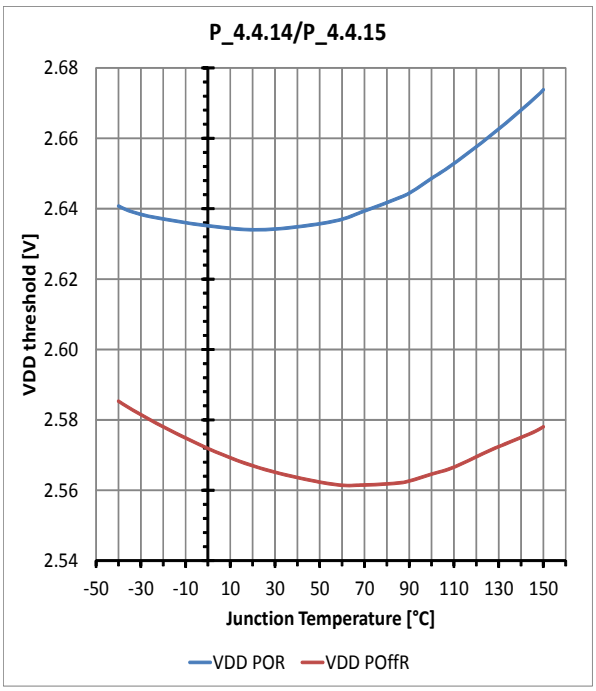
Overvoltage switch ON voltage threshold



Overvoltage switch OFF voltage threshold



VDD Power-on-reset and VDD Power-off-reset



5 General Description

5.1 Power Supply

The TLE94003EP has two power supply inputs, V_S and V_{DD}. The half bridge outputs are supplied by V_S, which is connected to the 12V automotive supply rail. V_{DD} is used to supply the I/O buffers and internal voltage regulator of the device.

V_S and V_{DD} supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on V_S. The system can therefore continue to operate once V_S has recovered, without having to resend commands to the device.

A rising edge on V_{DD} crossing $V_{DD\ POR}$ triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched off (high impedance).

An electrolytic and 100nF ceramic capacitors are recommended to be placed as close as possible to the V_S supply pin of the device for improved EMC performance in the high and low frequency band. The electrolytic capacitor must be dimensioned to prevent the VS voltage from exceeding the absolute maximum rating. In addition, decoupling capacitors are recommended on the V_{DD} supply pin.

5.2 Operation modes

5.2.1 Normal mode

The TLE94003EP enters normal mode by setting EN1 or EN2 to High. In normal mode, the charge pump is active and all output transistors can be activated or deactivated according to **Chapter 6.1**.

5.2.2 Sleep mode

The TLE94003EP enters sleep mode by setting the EN1 and EN2 pins to Low. The EN1 and EN2 inputs have an internal pull-down resistor.

In sleep mode, all output transistors are turned off and the logic content is reset. The current consumption is reduced to $I_{SQ} + I_{DD\_Q}$.

5.3 Reset Behaviour

The following reset triggers have been implemented in the TLE94003EP:

V_{DD} Undervoltage Reset:

The digital block will be deactivated, the logic contents cleared and the output stages are switched off if V_{DD} is below the undervoltage threshold, $V_{DD\ POffR}$. The digital block is initialized once V_{DD} voltage levels is above the undervoltage threshold, $V_{DD\ POR}$.

Reset on EN1/2 pins:

If the EN1/2 pins are pulled Low, the logic content is reset and the device enters sleep mode.

5.4 Reverse Polarity Protection

The TLE94003EP requires an external reverse polarity protection. During reverse polarity, the free-wheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow (I_{RB}) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended (see **Figure 4**).

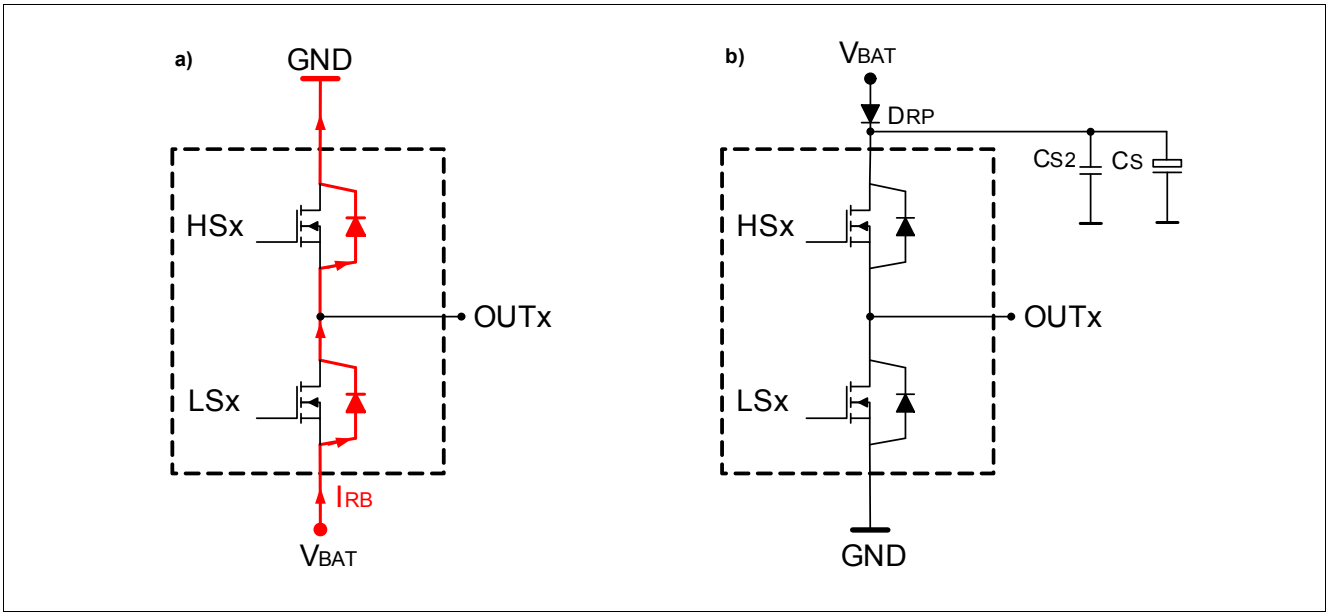


Figure 4 Reverse Polarity Protection

6 Half-Bridge Outputs

The half-bridge outputs of the TLE94003EP are intended to drive motor loads. They consist of a total of three DMOS half-bridges, which can be driven either continuously or in PWM via INx pins. The output stages integrated circuits protect the outputs against overcurrent and overtemperature.

6.1 Output Stages

EN1 and EN2 inputs control the state of the device according to **Table 6**.

- When EN1 = 0 and EN2 = 0, the device enters sleep mode with low power consumption and all outputs are OFF (high impedance).
- When EN1=1, HB1 and HB2 are enabled
- When EN2=1, HB3 is enabled

Table 6 Device states

EN1	EN2	HB1/2	HB 3	Device state
0	0	OFF	OFF	Sleep mode, all outputs are OFF
0	1	OFF	Enabled	Device is in normal mode
1	0	Enabled	OFF	Device is in normal mode
1	1	Enabled	Enabled	Device is in normal mode

*Note: After the transition from sleep mode to normal mode, the outputs are OFF for a duration t_{SET_DI} .See **Figure 5***

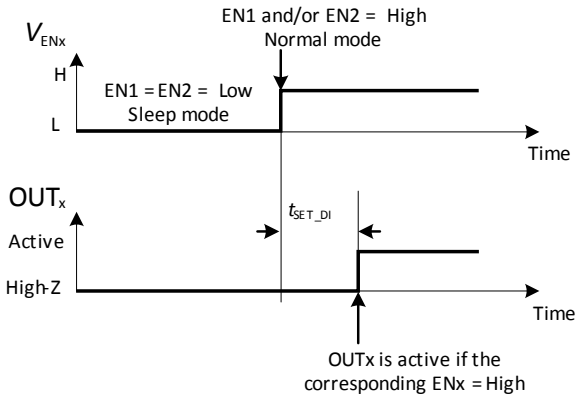


Figure 5 Output setup time after a transition from standby to normal mode

The control inputs consist of CMOS-compatible schmitt-triggers with hysteresis. There are altogether three control inputs, i.e. IN1, IN2 and IN3 with internal pull-down resistors.

If EN1 = 0, HB1 and HB2 are OFF. If EN1 = 1, HB1 and HB2 are controlled according to**Table 7**

Table 7 Functional Truth Table for HB1 and HB2

EN1	IN1	IN2	HB1	HB2	Mode
0	X	X	OFF	OFF	HB1 and HB2 are OFF
1	0	0	L	L	Brake Low

Half-Bridge Outputs

Table 7 Functional Truth Table for HB1 and HB2

EN1	IN1	IN2	HB1	HB2	Mode
1	0	1	L	H	Motor counter-clockwise
1	1	0	H	L	Motor clockwise
1	1	1	H	H	Brake High

If EN2 = 0, HB3 is high impedance. If EN2 = 1, the states of HB3 is controlled according to**Table 8**

Table 8 Functional Truth table for HB3

EN2	IN3	HB3
0	X	OFF
1	0	L
1	1	H

If two motors are connected in cascaded configuration (see **Figure 6**), the motors and the half-bridges behave according to **Table 9**.

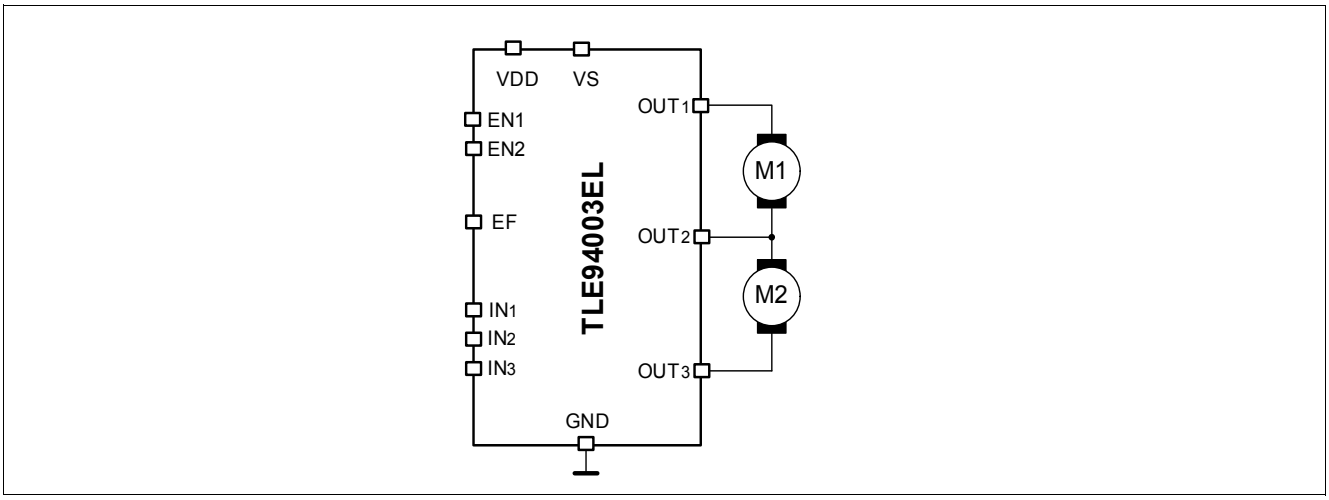


Figure 6 TLE94003EP with two motors in cascaded configuration

Table 9 Functional Truth Table for HB1, HB2 and HB3 controlling two cascaded motors

EN1	EN2	IN1	IN2	IN3	HB1	HB2	HB3	Motor1	Motor 2
0	0	X	X	X	OFF	OFF	OFF	OFF	OFF
1	0	0	0	X	L	L	OFF	Brake Low	OFF
1	0	0	1	X	L	H	OFF	Counter-clockwise	OFF
1	0	1	0	X	H	L	OFF	Clockwise	OFF
1	0	1	1	X	H	H	OFF	Brake High	OFF
1	1	0	0	0	L	L	L	Brake Low	Brake Low
1	1	0	0	1	L	L	H	Brake Low	Counter-clockwise
1	1	0	1	0	L	H	L	Counter-clockwise	Clockwise
1	1	0	1	1	L	H	H	Counter-clockwise	Brake High
1	1	1	0	0	H	L	L	Clockwise	Brake Low

Half-Bridge Outputs

Table 9 Functional Truth Table for HB1, HB2 and HB3 controlling two cascaded motors

EN1	EN2	IN1	IN2	IN3	HB1	HB2	HB3	Motor1	Motor 2
1	1	1	0	1	H	L	H	Clockwise	Counter-clockwise
1	1	1	1	0	H	H	L	Brake High	Clockwise
1	1	1	1	1	H	H	H	Brake High	Brake High

6.2 Diagnosis Monitoring

The EF pin (push-pull output) reports the following error conditions:

- Overcurrent (OC)
- Overtemperature (OT)
- VS overvoltage and VS undervoltage

EF reports an overcurrent event on HB1/2 only if EN1 = 1. Likewise, EF reports an overcurrent on HB3 only if EN2 = 1.

After an overcurrent event is detected on HB1/2, EF is latched to 1, until EN1 = 0.Likewise, after an overcurrent event detected on HB3, EF is latched to 1 until EN2 = 0.

EF reports overtemperature or VS overvoltage/undervoltage events if the device is in normal mode (EN1 = 1 or EN2 = 1). The error flag is latched to 1 for these fault conditions until EN1 = 0 and EN2 = 0

Table 10 Error reporting by EF pin

EN1	EN2	Error reported by EF pin
0	0	Not applicable, the device is in sleep mode
1	0	OC on HB1/2, OT, VS under/overvoltage
0	1	OC on HB3, OT, VS under/overvoltage
1	1	OC on HB1/2, OC on HB3, OT, VS under/overvoltage

The table below depicts the EF behaviour:

Table 11 Error flag behaviour and reset conditions

Fault condition	EF	Reset conditions
No fault	0	–
Overcurrent on HB1 or HB2	1 (latched)	Set EN1 pin to 0 for **tEF_RESET**
Overcurrent on HB3	1 (latched)	Set EN2 pin to 0 for **tEF_RESET**
VS overvoltage	1 (latched)	$V_S < V_{OV\,ON}$, EN1 = 0 and EN2 = 0 for **tEF_RESET**
VS undervoltage	1 (latched)	$V_S > V_{UV\,ON}$, EN1 = 0 and EN2 = 0 for **tEF_RESET**
Overtemperature	1 (latched)	EN1 = 0 and EN2 = 0 for **tEF_RESET**

6.3 Protection

This device has embedded protective functions which are designed to prevent the destruction of the device under fault conditions described in this section. Fault conditions are treated as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

6.3.1 Short Circuit of Output to Supply or Ground

The high-side switches are protected against short circuits to ground whereas the low-side switches are protected against short circuits to supply.

The high-side and low-side switches will enter into an over-current condition if the current within the switch exceeds the overcurrent shutdown detection threshold, I_{SD}. Upon detection of the I_{SD} threshold, an

overcurrent shutdown filter, t_{dSD} is begun. As the current rises beyond the threshold I_{SD}, it will be limited by the current limit threshold, I_{LIM}. Upon expiry of the overcurrent shutdown filter time, the affected power switch is latched off (see **Figure 7** and **Figure 8**) and the EF is set to 1 and latched.

The faulty power switch remains deactivated and EF is latched as long as the corresponding ENx =1.

To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists) the microcontroller shall:

1. clear the error flag by setting the corresponding ENx to 0 (see **Table 11**)
2. set the corresponding ENx to 1 in order to re-enable the corresponding half-bridges

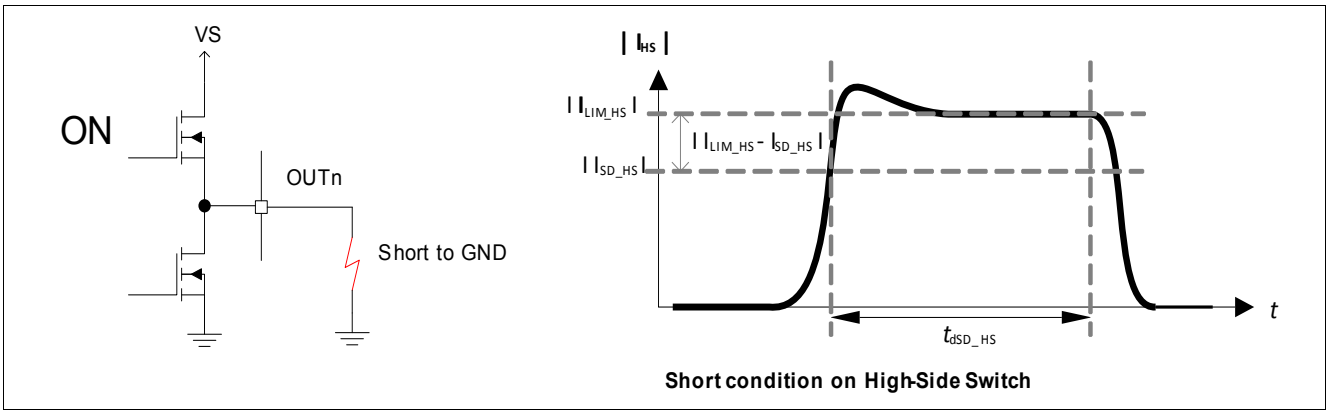


Figure 7 High-Side Switch - Short Circuit and Overcurrent Protection

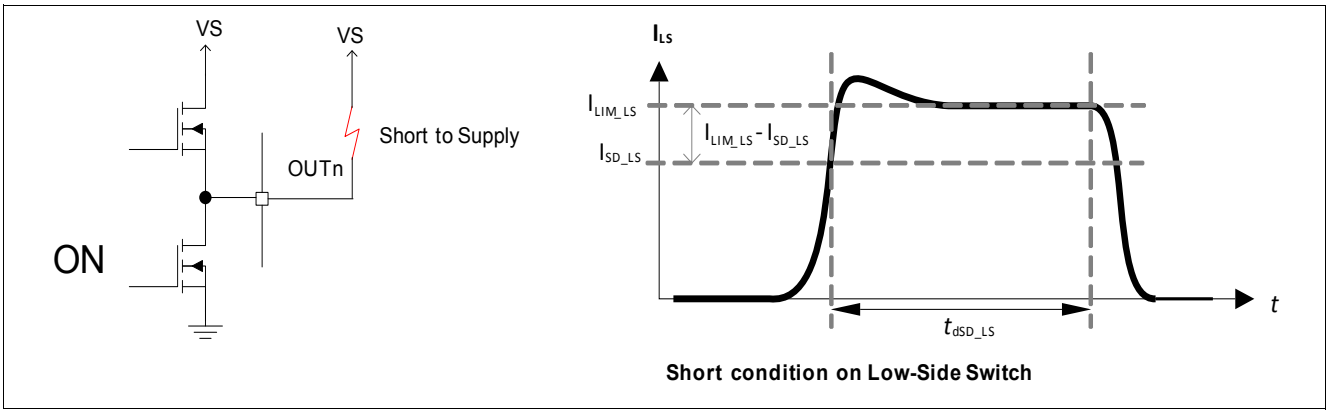


Figure 8 Low-Side Switch - Short Circuit and Overcurrent Protection

6.3.2 Cross-current protection

In bridge configurations the high-side and low-side power transistors are ensured never to be simultaneously “ON” to avoid cross currents. This is achieved by integrating delays in the driver stage of the power outputs to create a dead-time between switching off of one power transistor and switching on of the adjacent power transistor within the half-bridge. The dead times, t_{DHL} and t_{DLH}, as shown in **Figure 9** case 3 and **Figure 10** case 3, have been specified to ensure that the switching slopes do not overlap with each other. This prevents a cross conduction event.

Half-Bridge Outputs

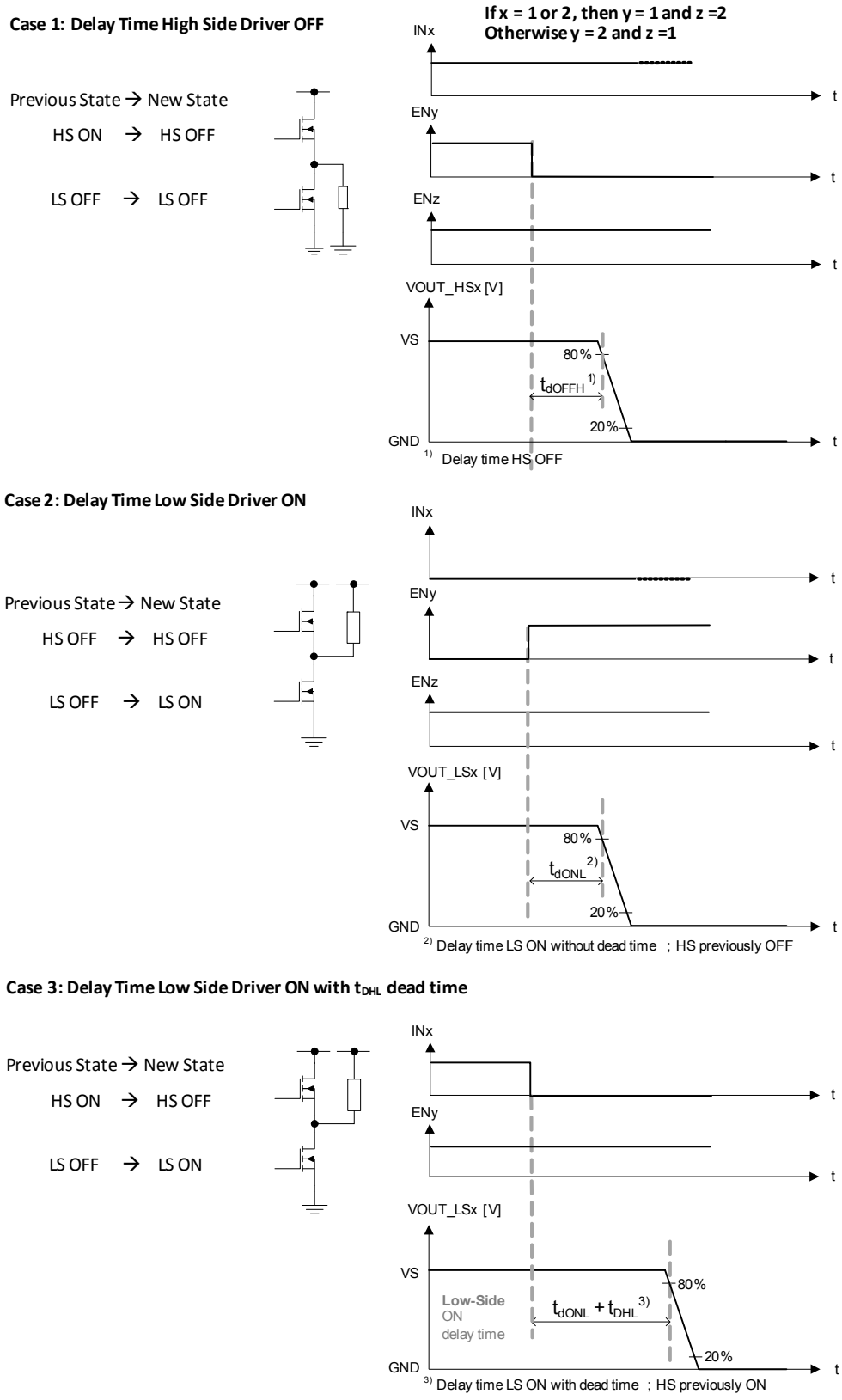


Figure 9 Half bridge outputs switching times - high-side to low-side transition

Half-Bridge Outputs

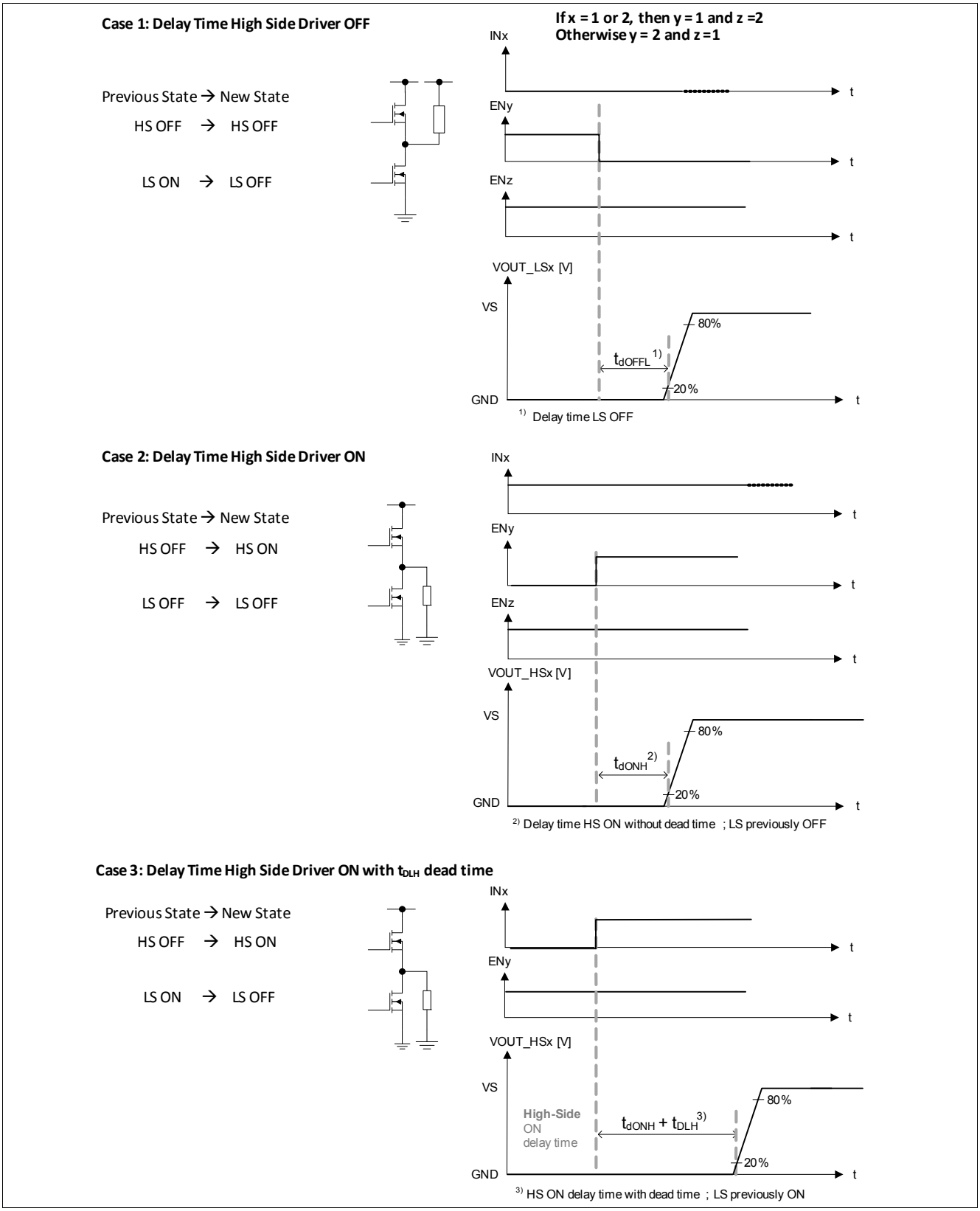


Figure 10 Half bridge outputs switching times- low-side to high-side transition

6.3.3 Temperature monitoring and shutdown

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the shutdown threshold.

Half-Bridge Outputs

If one or more temperature sensors reach the shut-down temperature threshold, **all outputs are latched off**. All outputs remain deactivated as long as EN1 = 1 or EN2 = 1.

To resume normal functionality of the power switch (in the event the overtemperature condition disappears or to verify if the failure still exists) the microcontroller shall:

1. clear the error flag by setting EN1 and EN2 to 0 (see **Table 11**)
2. set EN1 or EN2 to 1 in order to send the device from sleep mode back to normal mode

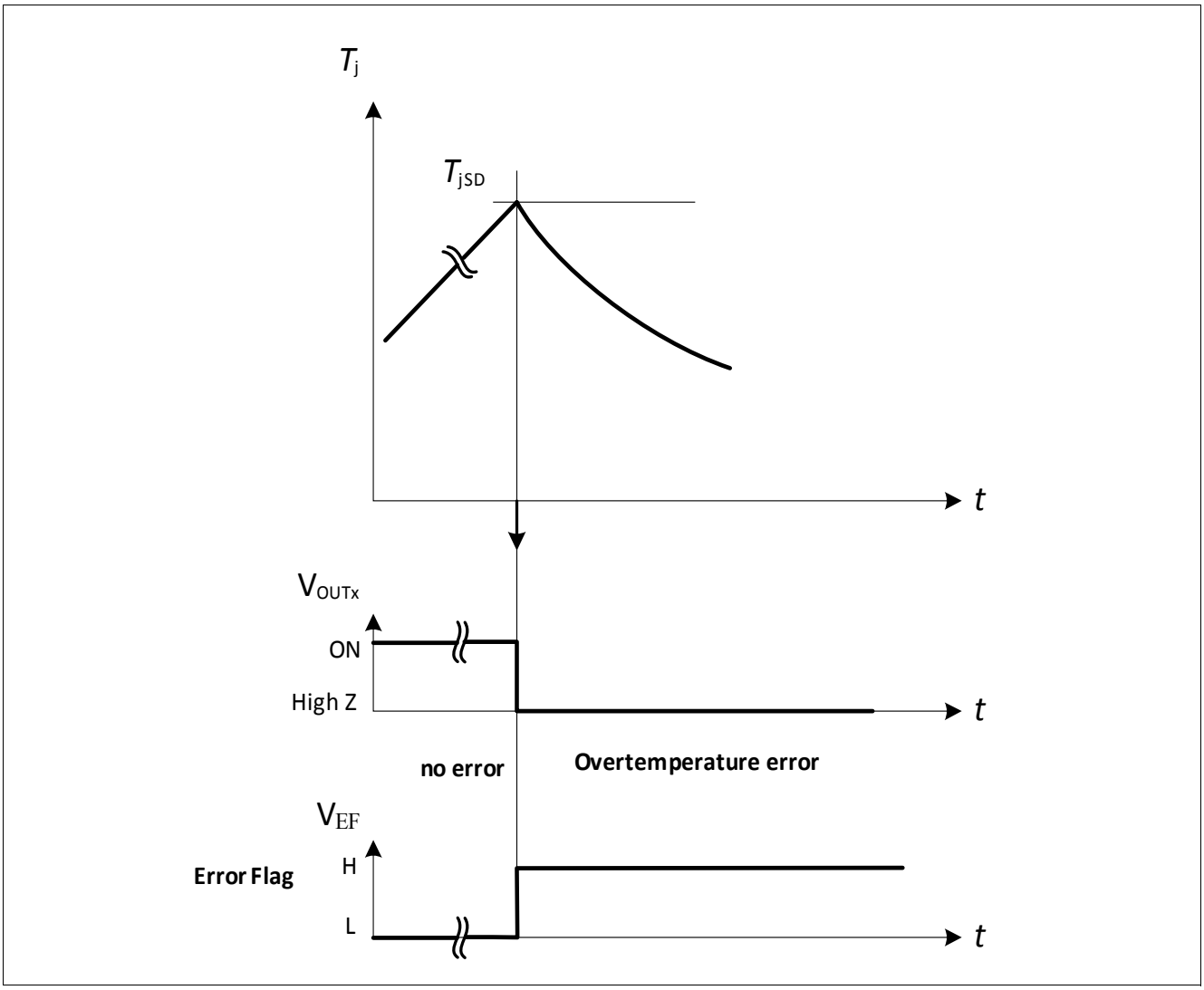


Figure 11 Overtemperature Behaviour

6.3.4 VS Undervoltage Behaviour

If the supply voltage decreases to the undervoltage switch-off threshold, $V_{UV\,OFF}$, then all output switches are switched off, and the error flag EF is set to High (error detection). If V_S rises again and reaches the undervoltage switch-on threshold, $V_{UV\,ON}$, the power-stages are automatically reactivated according to ENx and INx. Refer to **Figure 12**

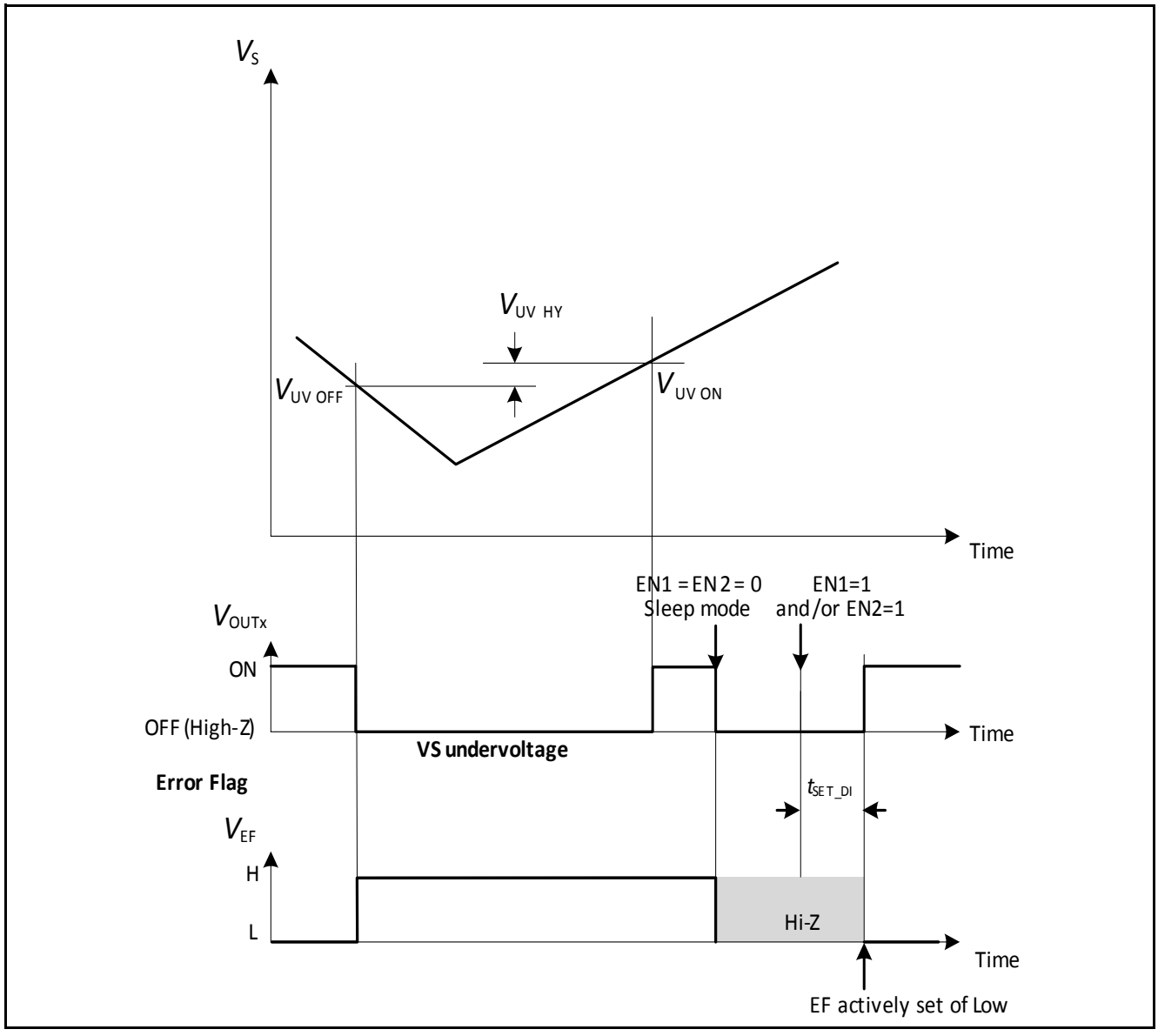


Figure 12 Undervoltage behaviour

6.3.5 VS Overvoltage Behaviour

If the supply voltage increases beyond the overvoltage switch threshold, $V_{OV\ OFF}$, then all output switches are switched off and EF is set High, indicating an overvoltage condition. If V_S decreases again and reaches the overvoltage switch-on threshold, $V_{OV\ ON}$, then the power-stages are automatically reactivated according to ENx and INx. Refer to **Figure 13**.

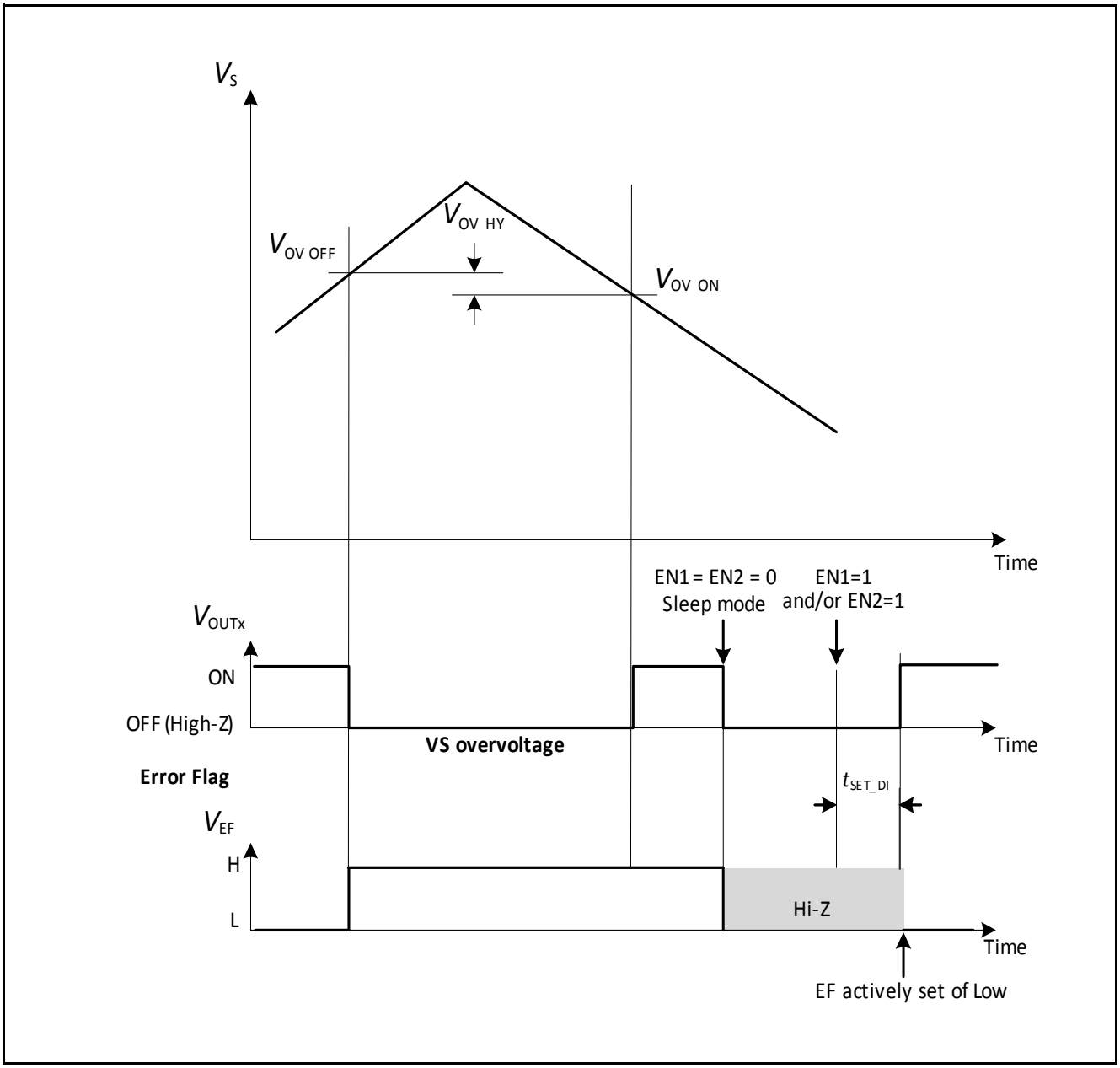


Figure 13 Overvoltage behaviour

6.3.6 V_{DD} Undervoltage

In the event the V_{DD} logic supply decreases below the undervoltage threshold, V_{DD_POFFR}, the TLE94003EP will enter reset. EF is set to high impedance during a V_{DD} undervoltage event.

The digital block will be initialized and the output stages are switched off to High impedance. The undervoltage reset is released once V_{DD} voltage levels are above the undervoltage threshold, $V_{DD\ POR}$.

7 Application Information

Note: The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application.

7.1 Application Diagram

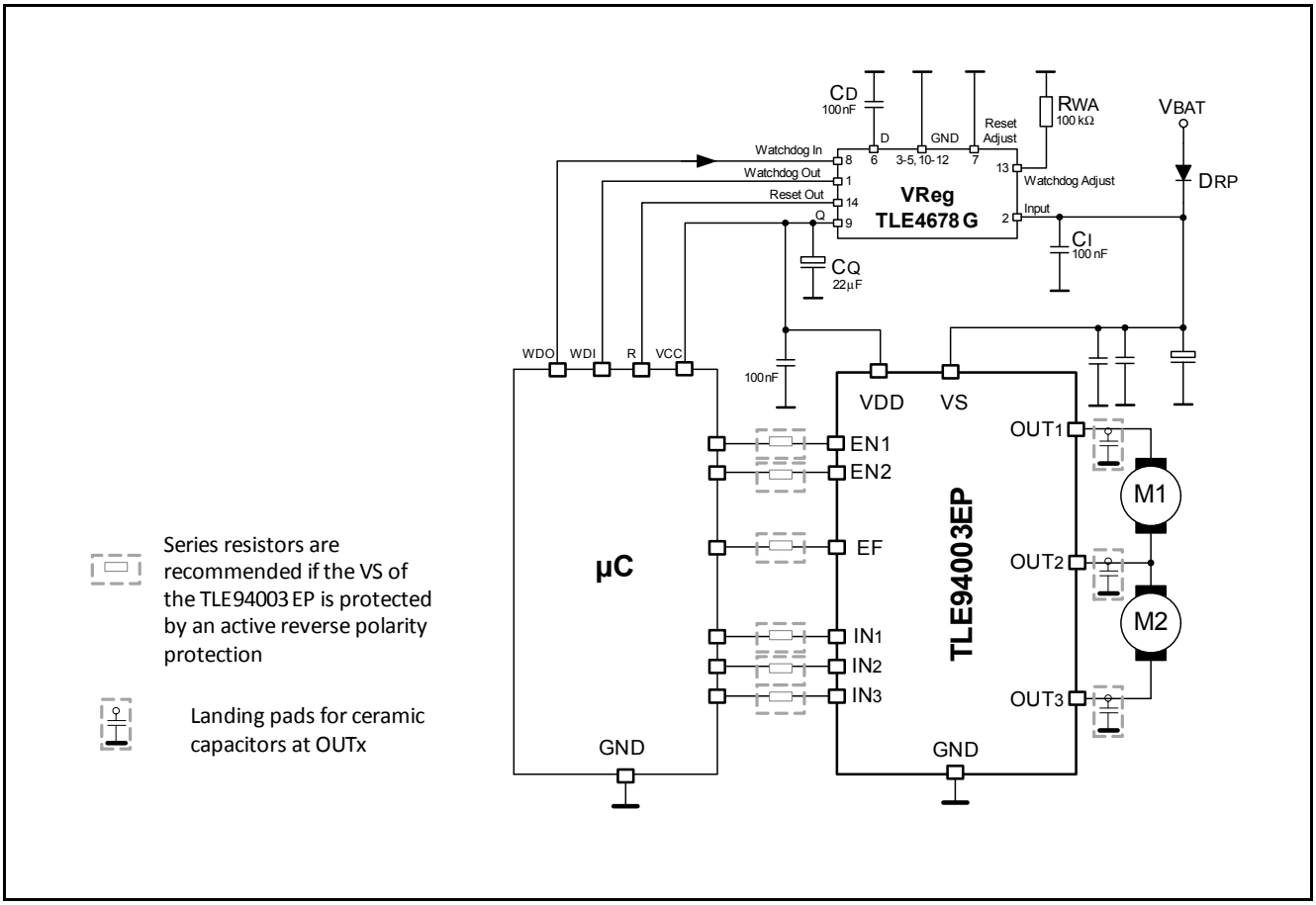


Figure 14 Application example with DC motors

Application Information

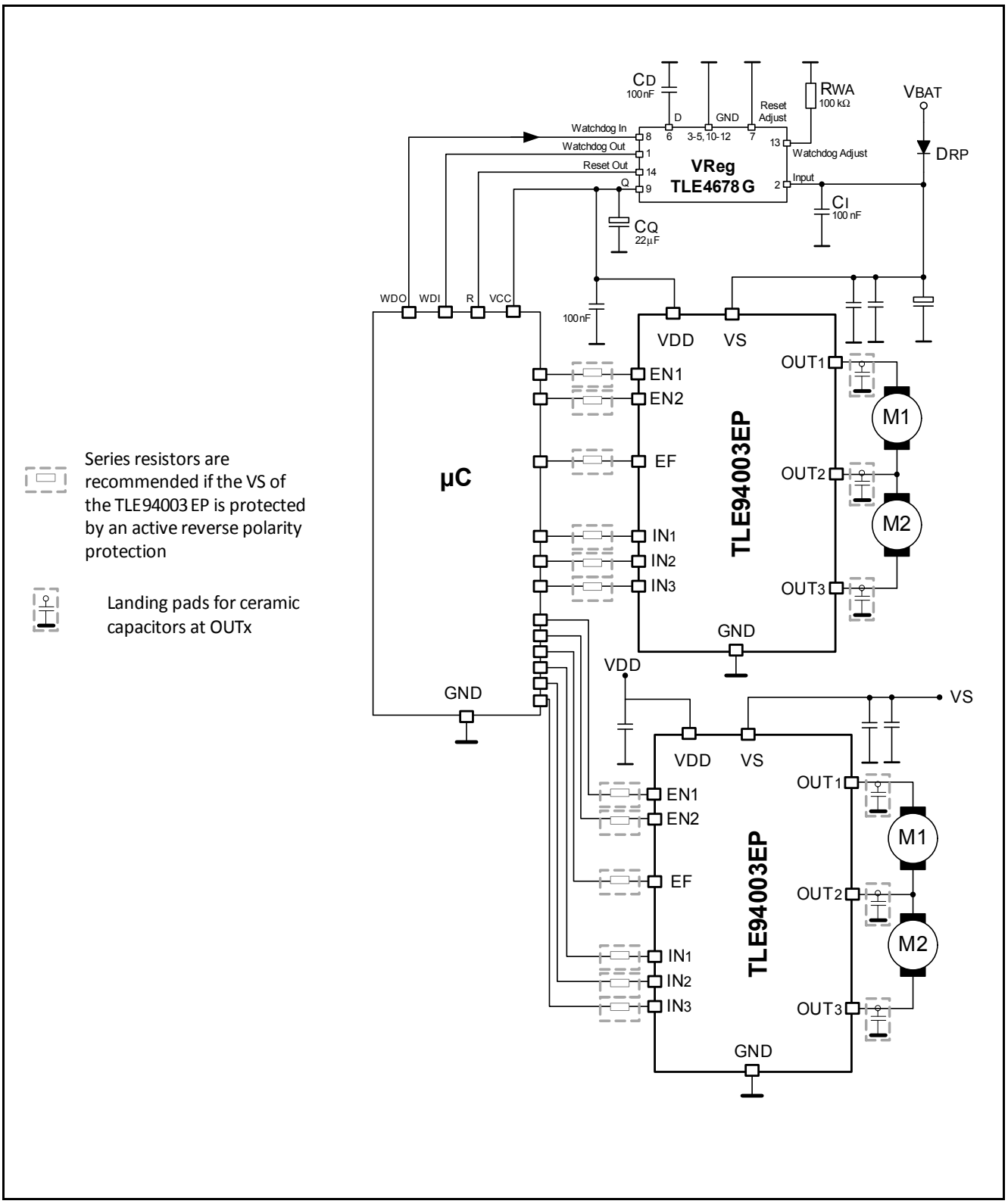


Figure 15 Application Example with two TLE94003EP

Notes on the application example

1. *Series resistors between the microcontroller and the signal pins of the TLE94003EP are recommended if an active reverse polarity protection (MOSFET) is used to protect the VS pin. These resistors limit the current between the microcontroller and the device during negative transients on VBAT (e.g. ISO/TR 7637 pulse 1)*

Application Information

2. *Landing pads for ceramic capacitors at the outputs of the TLE94003EP as close as possible to the connectors are recommended (the ceramic capacitors are not populated if unused). These ceramic capacitors can be mounted if a higher performance in term of ESD capability is required.*
3. *The electrolytic capacitor at the VS pin should be dimensioned in order to prevent the VS voltage from exceeding the absolute maximum rating. PWM operation with a too low capacitance can lead to a VS voltage overshoot, which results in a VS overvoltage detection.*
4. *Not used (NU) pins and unused outputs are recommended to be left unconnected (open) in the application. If NU pins or unused output pins are routed to an external connector which leaves the PCB, then these outputs should have provision for a zero ohm jumper (depopulated if unused) or ESD protection. In other words, NU and unused pins should be treated like used pins.*
5. *Place bypass ceramic capacitors as close as possible to the VS pins, with shortest connections the GND pins and GND layer, for best EMC performance*

7.2 Thermal application information

Ta = -40°C, Ch1 to Ch3 are dissipating a total of 0.6W (0.2W each).

Ta = 85°C, Ch1 to Ch3 are dissipating a total of 0.405W (0.135W each).

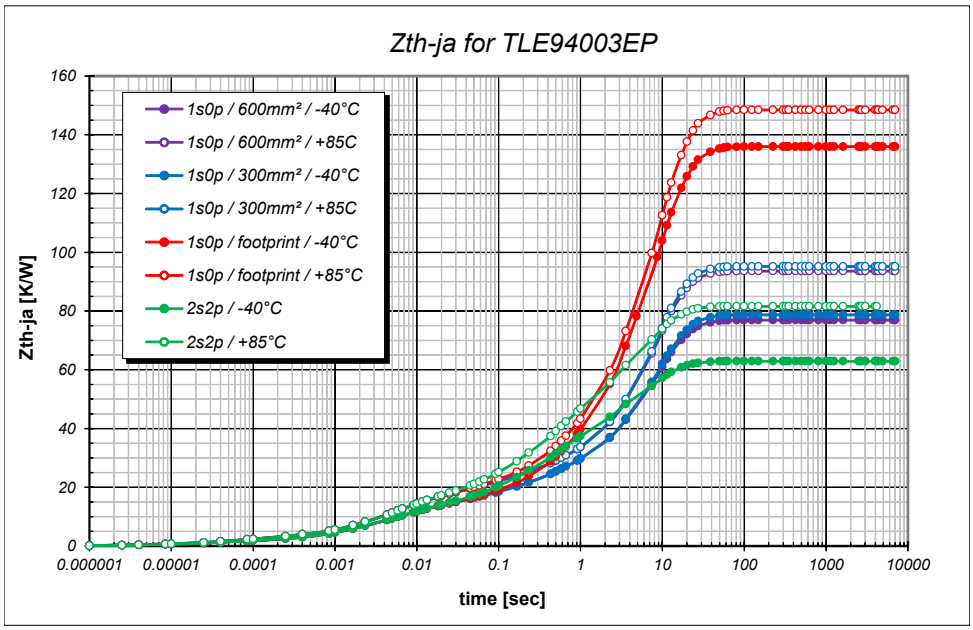


Figure 16 ZthJA Curve for different PCB setups

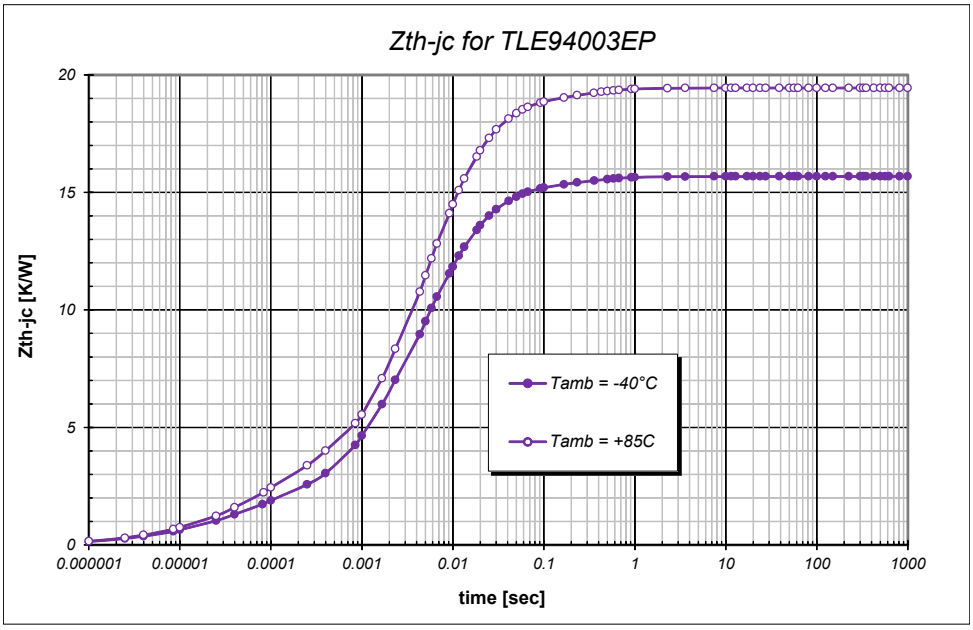


Figure 17 ZthJC Curve

8 Package Outlines

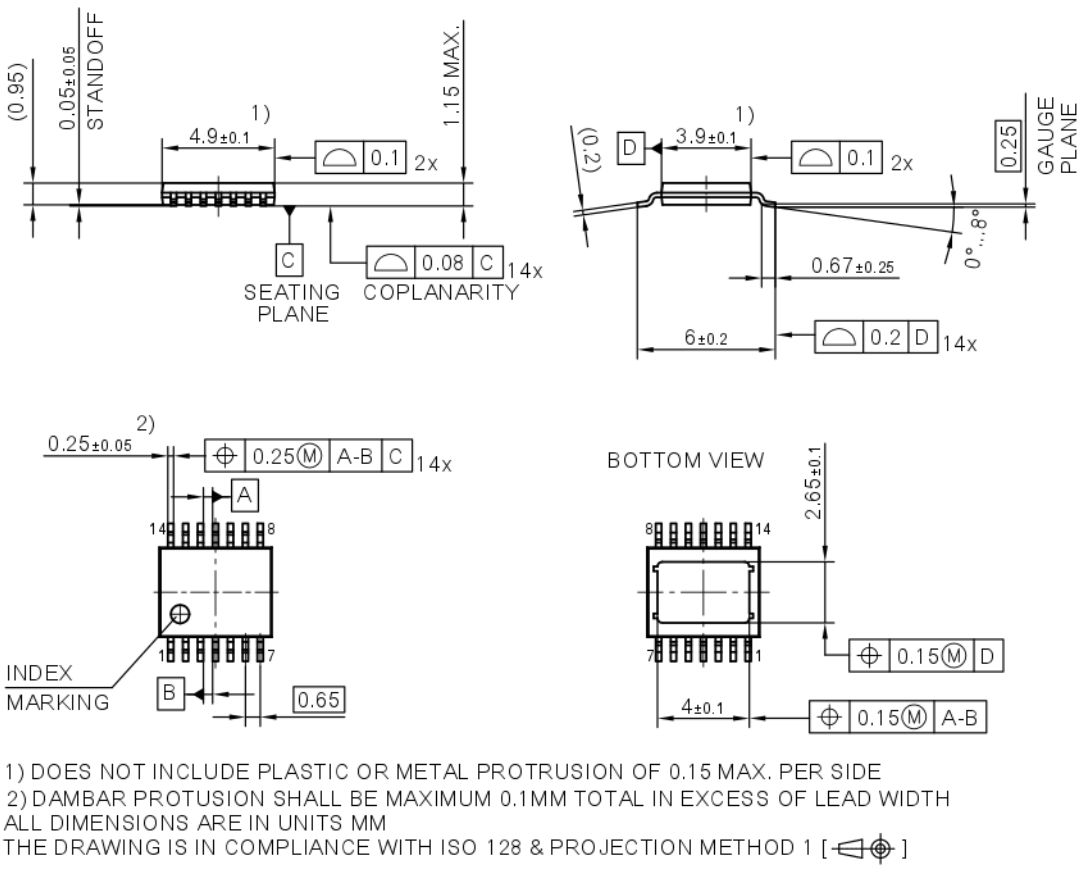


Figure 18 PG-TSDSO-14 (Plastic Green - Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e lead-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
1.0	2017-12-07	Initial release

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