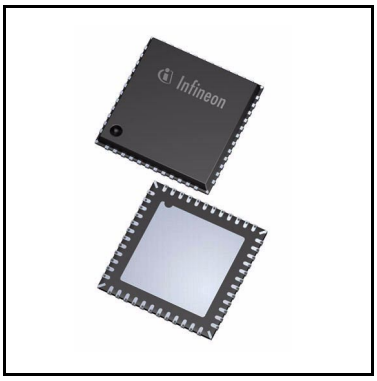
OPTIREG™ PMIC TLF30682QVS01

Power Management IC



Features

- High-efficiency multi-rail power supply chip optimized for the use in Advanced Driver Assistance Systems (ADAS)
- Step-down pre-regulator for wide input voltage range from 3.7 V to 35 V (40 V limited time) with low over-all power loss and fast transient performance. Suitable for operation with ceramic capacitors
- High-efficiency step-down post-regulator for second output voltage generation
- Step-up post-regulator with 5 V output voltage
- Voltage monitoring for two external voltage rails including enable signals
- Configurable window watchdog
- 16-bit SPI
- Green Product (RoHS compliant)

Potential applications

- Automotive applications
- Advanced Driver Assistance Systems (ADAS)
  - 77 GHz radar ECUs
  - Camera ECUs
- Human Machine Interface (HMI) applications

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ PMIC TLF30682QVS01 is a multi-output Power Management IC (PMIC) for automotive applications. The device consists of a battery connected buck regulator (Buck1) providing 3.3 V to external loads and to two low voltage post-regulators. The first post-regulator (Buck2) is a buck regulator providing an output voltage of 1.25 V. The second post-regulator (Boost1) provides an output voltage of 5.0 V and is intended to supply one or two CAN transceivers.

The TLF30682QVS01 supports 16-bit SPI communication to a microcontroller. The SPI commands support reading status information from the device and control of features such as PWM synchronization and control of the power regulators.

The device operates at a nominal switching frequency of 2.2 MHz. The switching frequency can be selected via SPI with an operating range from 1.8 MHz to 2.5 MHz in steps of 100 kHz. The switching regulators can be synchronized to an external clock signal. The TLF30682 can provide a synchronization signal for other DC/DC regulators in the system.

The TLF30682QVS01 provides two voltage monitoring channels with monitoring inputs and enable outputs. The monitoring channels can be used to control and monitor external voltage regulators. The external voltage regulator can be either LDOs or DC/DC switching regulators.

Type	Package	Marking
TLF30682QVS01	PG-VQFN-48	TLF30682 S01

Table of Contents

1 Block diagram

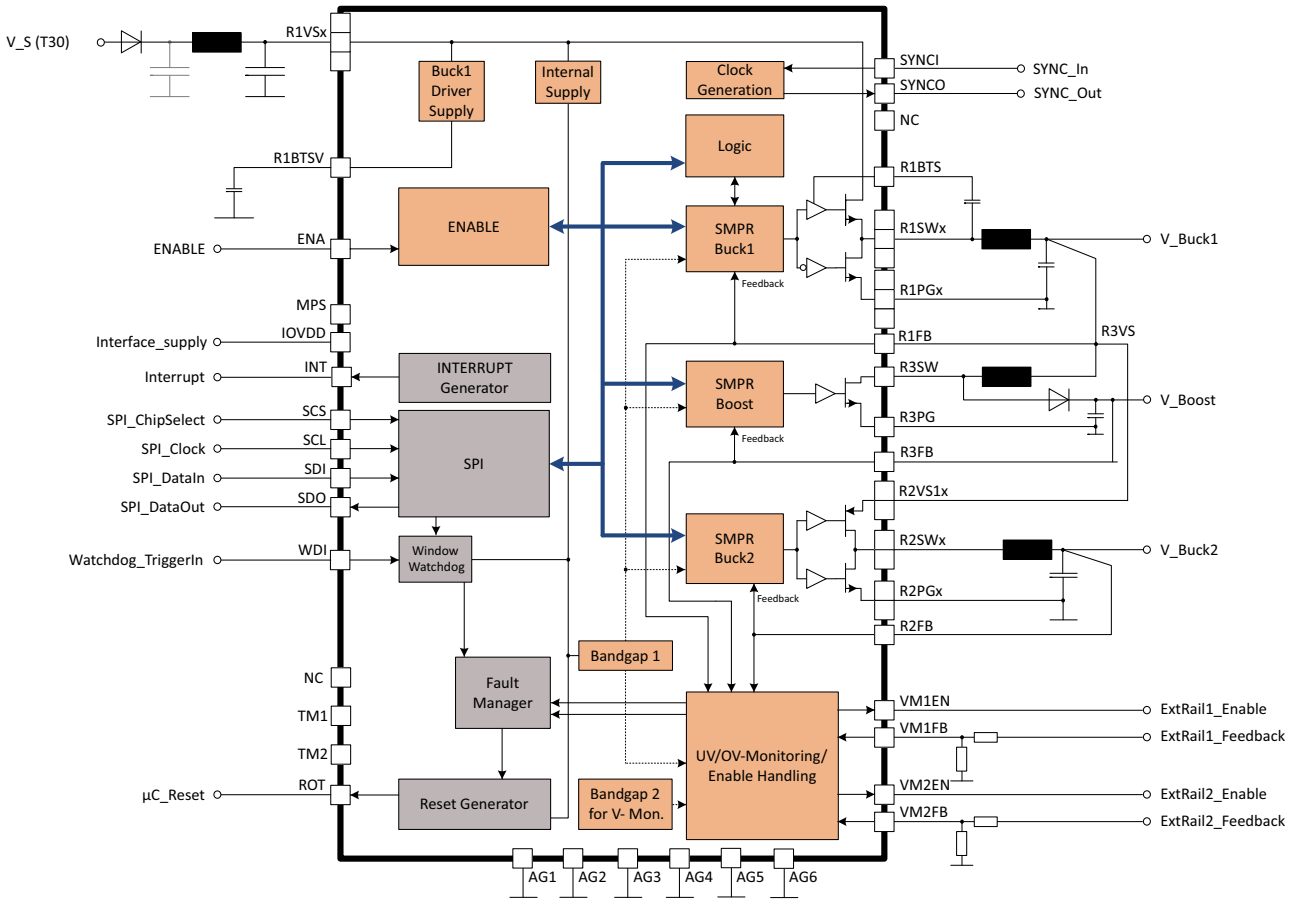


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

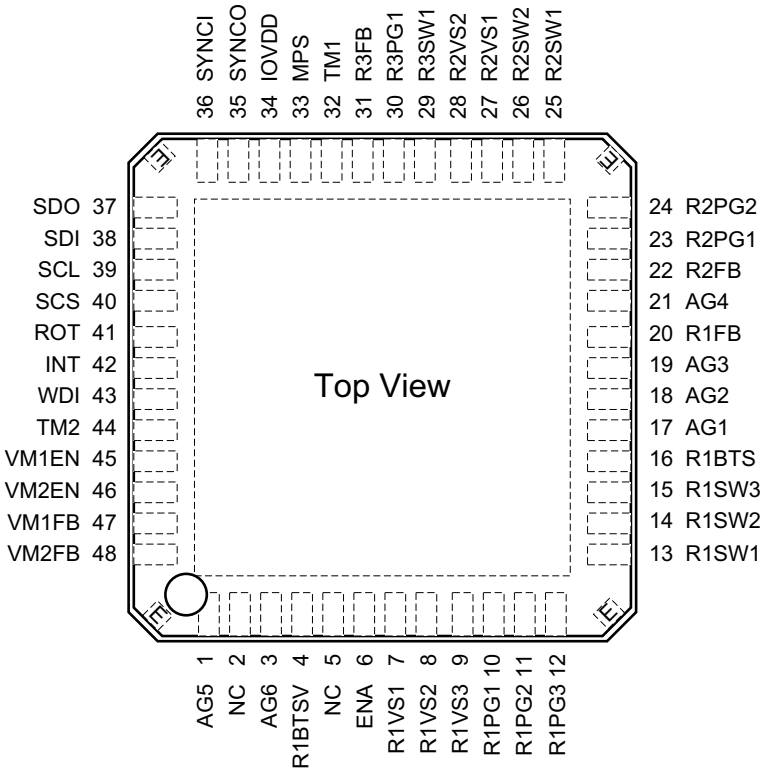


Figure 2 Pin configuration

2.2 Pin definitions and functions PG-VQFN-48

Pin	Symbol	Function
1	AG5	**Analog ground, pin 5:** Connect directly (low ohmic and low inductive) to ground.
2	NC	**Not connected:** Leave the pin floating in the application.
3	AG6	**Analog ground, pin 6:** Connect directly (low ohmic and low inductive) to ground.
4	R1BTSV	**Decoupling pin for internal supply voltage:** Connect a decoupling capacitor between the pin and R1PGx.
5	NC	**Not connected:** Leave the pin floating in the application.
6	ENA	**Enable input:** A valid enable condition at the pin will enable the device.

Pin configuration

Pin	Symbol	Function
7	R1VS1	**High voltage regulator supply voltage, pin 1:** Connect in parallel with R1VS2 and R1VS3 and then to the supply (battery) voltage via a reverse protection diode. Additionally connect a capacitor between the pin and ground. An EMC filter is recommended.
8	R1VS2	**High voltage regulator supply voltage, pin 2:** Connect in parallel with R1VS1 and R1VS3 and then to the supply (battery) voltage via a reverse protection diode. Additionally connect a capacitor between the pin and ground. An EMC filter is recommended.
9	R1VS3	**High voltage regulator supply voltage, pin 3:** Connect in parallel with R1VS1 and R1VS2 and then to the supply (battery) voltage via a reverse protection diode. Additionally connect a capacitor between the pin and ground. An EMC filter is recommended.
10	R1PG1	**High voltage regulator power ground, pin 1:** Connect in parallel with R1PG2 and R1PG3 and then to the Buck1 output capacitor ground terminal to ground.
11	R1PG2	**High voltage regulator power ground, pin 2:** Connect in parallel with R1PG1 and R1PG3 and then to the Buck1 output capacitor ground terminal to ground.
12	R1PG3	**High voltage regulator power ground, pin 3:** Connect in parallel with R1PG1 and R1PG2 and to the Buck1 output capacitor ground terminal to ground.
13	R1SW1	**High voltage regulator power stage output, pin 1:** Connect in parallel with R1SW2 and R1SW3 and then to the pre-regulator (Buck1) output filter inductor.
14	R1SW2	**High voltage regulator power stage output, pin 2:** Connect in parallel with R1SW1 and R1SW3 and then to the pre-regulator output filter inductor.
15	R1SW3	**High voltage regulator power stage output, pin 3:** Connect in parallel with R1SW1 and R1SW2 and then to the pre-regulator output filter inductor.
16	R1BTS	**Bootstrap supply voltage:** Connect via the bootstrap capacitor to the R1SWx pins.
17	AG1	**Analog ground, pin 1:** Connect directly (low ohmic and low inductive) to ground.
18	AG2	**Analog ground, pin 2:** Connect directly (low ohmic and low inductive) to ground.
19	AG3	**Analog ground, pin 3:** Connect directly (low ohmic and low inductive) to ground.
20	R1FB	**High voltage regulator output voltage feedback pin:** Connect to the Buck1 output capacitor.
21	AG4	**Analog ground, pin 4:** Connect directly (low ohmic and low inductive) to ground.
22	R2FB	**Post-regulator output voltage feedback pin:** Connect to the Buck2 output capacitor.

Pin configuration

Pin	Symbol	Function
23	R2PG1	**Pre-regulator power ground, pin 1:** Connect in parallel with R2PG2 and then to the Buck2 output capacitor ground terminal to ground.
24	R2PG2	**Pre-regulator power ground, pin 2:** Connect in parallel with R2PG1 and then to the Buck2 output capacitor ground terminal to ground.
25	R2SW1	**Post-regulator power stage output, pin 1:** Connect in parallel with R2SW2 and then to the Buck2 output filter inductor.
26	R2SW2	**Post-regulator power stage output, pin 2:** Connect in parallel with R2SW1 and then to the Buck2 output filter inductor.
27	R2VS1	**Post-regulator supply voltage, pin 1:** Connect to the Buck1 output capacitor.
28	R2VS2	**Post-regulator supply voltage, pin 2:** Connect to the Buck1 output capacitor.
29	R3SW1	**Regulator 3 power stage output, pin 1:** Connect to Boost1 inductor and external rectifying diode.
30	R3PG1	**Regulator 3 power ground, pin 1:** Connect to Boost1 output capacitor ground terminal to ground.
31	R3FB	**Regulator 3 output voltage feedback pin:** Connect to Boost1 output capacitor.
32	TM1	**Test mode 1 pin:** Not for customer use. Leave the pin floating in the application.
33	MPS	**Microcontroller programming mode pin** Connect to ground for normal operation in the application. Optionally the pin can be used for microcontroller programming purposes. For details please refer to the application information section.
34	IOVDD	**I/O supply voltage:** Connect to the I/O supply voltage of the microcontroller.
35	SYNCO	**Synchronization output signal:** Connect to an optional external switch-mode post-regulator synchronization input. The signal delivers the internal switching frequency either in phase or shifted by 180° (configurable via SPI). The switch-mode post-regulator synchronizes to the rising edge. If the pin is not used, it should be left floating.
36	SYNCI	**Synchronization input signal:** Connect to an optional external synchronization signal to synchronize the switching of the internal switch-mode regulators. The feature needs to be enabled via SPI. If the pin is not used, it should be left floating.
37	SDO	**Serial peripheral interface, signal data output:** SPI signalling port, connect to SPI port "data input" of microcontroller to send status information during SPI communication.
38	SDI	**Serial peripheral interface, signal data input:** SPI signalling port, connect to SPI port "data output" of microcontroller to receive commands during SPI communication.

Pin configuration

Pin	Symbol	Function
39	SCL	**Serial peripheral interface, signal clock:** SPI signalling port, connect to SPI port "clock" of microcontroller to clock the device for SPI communication.
40	SCS	**Serial peripheral interface, signal chip select:** SPI signalling port, connect to SPI port "chip select" of microcontroller to address the device for SPI communication.
41	ROT	**Reset output:** Open drain structure with internal pull up resistor. A "low" signal at this pin indicates a reset event for the microcontroller. Connect to microcontroller reset input.
42	INT	**Interrupt signal:** Push-pull output. A "low" pulse at this pin indicates an interrupt, and the microcontroller reads the SPI status registers. Connect to a non-maskable interrupt port (NMI) of the microcontroller.
43	WDI	**Watchdog input, trigger signal:** Input for trigger signal. Connect the "trigger signal output" of the microcontroller to the pin. If the pin is not used it should be left floating (internal pull-down).
44	TM2	**Test mode 2 pin:** Not for customer use. Connect the pin to GND in the application.
45	VM1EN	**Enable signal for external voltage rails 1:** Connect to the enable pin of a optional external voltage regulator 1. If the optional external regulator is not used, connect to ground.
46	VM2EN	**Enable signal for external voltage rails 2:** Connect to the enable pin of a optional external voltage regulator 2. If the optional external regulator is not used, connect to ground.
47	VM1FB	**Input for optional external voltage monitoring rail 1:** Connect an external resistor divider to adjust the overvoltage threshold and the undervoltage threshold of the monitored external voltage generated by the optional external voltage regulator 1. If the optional external regulator is not used, connect to ground.
48	VM2FB	**Input for optional external voltage monitoring rail 2:** Connect an external resistor divider to adjust the overvoltage threshold and the undervoltage threshold of the monitored external voltage generated by the optional external voltage regulator 2. If the optional external regulator is not used, connect to ground.
Cooling Tab	GND	**Cooling tab:** Internally connected to GND
	EP1	**Edge pin no 1:** Keep the area below the pin free of ground or other signals. Do not solder this pin to ground or any other signal. This pin must be kept free of soldering.
	EP2	**Edge pin no 2:** Keep the area below the pin free of ground or other signals. Do not solder this pin to ground or any other signal. This pin must be kept free of soldering.

Pin configuration

Pin	Symbol	Function
	EP3	**Edge pin no 3:** Keep the area below the pin free of ground or other signals. Do not solder this pin to ground or any other signal. This pin must be kept free of soldering.
	EP4	**Edge pin no 4:** Keep the area below the pin free of ground or other signals. Do not solder this pin to ground or any other signal. This pin must be kept free of soldering.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Pin							
MPS	V_{MPS}	-0.3	–	6.0	V	–	P_3.1.1
IOVDD	V_{IOVDD}	-0.3	–	6.0	V	–	P_3.1.2
SCS	V_{SCS}	-0.3	–	6.0	V	–	P_3.1.3
SCL	V_{SCL}	-0.3	–	6.0	V	–	P_3.1.4
SDI	V_{SDI}	-0.3	–	6.0	V	–	P_3.1.5
SDO	V_{SDO}	-0.3	–	6.0	V	–	P_3.1.6
WDI	V_{WDI}	-0.3	–	6.0	V	–	P_3.1.7
INT	V_{INT}	-0.3	–	6.0	V	–	P_3.1.10
AG1	V_{AG1}	-0.3	–	0.3	V	–	P_3.1.13
AG2	V_{AG2}	-0.3	–	0.3	V	–	P_3.1.14
AG3	V_{AG3}	-0.3	–	0.3	V	–	P_3.1.15
AG4	V_{AG4}	-0.3	–	0.3	V	–	P_3.1.16
AG5	V_{AG5}	-0.3	–	0.3	V	–	P_3.1.17
AG6	V_{AG6}	-0.3	–	0.3	V	–	P_3.1.18
SYNCI	V_{SYNCI}	-0.3	–	6.0	V	–	P_3.1.19
SYNCO	V_{SYNCO}	-0.3	–	6.0	V	–	P_3.1.20
TM1	V_{TM1}	-0.3	–	6.0	V	–	P_3.1.22
ENA	V_{ENA}	-0.3	–	35	V	2)	P_3.1.23
ENA	I_{ENA}	-5.0	–	–	mA	–	P_3.1.24
R1BTS	V_{R1BTS}	V_{R1SWx} - 0.3	–	V_{R1SWx} + 6.0	V	–	P_3.1.25
R1BTSV	V_{R1BTSV}	-0.3	–	6.0	V	–	P_3.1.26
R1VS1	V_{R1VS1}	-0.3	–	35	V	2)	P_3.1.27
R1VS2	V_{R1VS2}	-0.3	–	35	V	2)	P_3.1.28
R1VS3	V_{R1VS3}	-0.3	–	35	V	2)	P_3.1.29
R1SW1	V_{R1SW1}	-0.3	–	V_{R1VSx}+2.0	V	–	P_3.1.30
R1SW2	V_{R1SW2}	-0.3	–	V_{R1VSx}+2.0	V	–	P_3.1.31
R1SW3	V_{R1SW3}	-0.3	–	V_{R1VSx}+2.0	V	–	P_3.1.32
R1PG1	V_{R1PG1}	-0.3	–	0.3	V	–	P_3.1.33
R1PG2	V_{R1PG2}	-0.3	–	0.3	V	–	P_3.1.34

Table 1 Absolute maximum ratings[1)] (cont'd)

T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
R1PG3	V_{R1PG3}	-0.3	–	0.3	V	–	P_3.1.35
R1FB	V_{R1FB}	-0.3	–	7.0	V	–	P_3.1.36
R2VS1	V_{R2VS1}	-0.3	–	7.0	V	–	P_3.1.37
R2VS2	V_{R2VS2}	-0.3	–	7.0	V	–	P_3.1.38
R2SW1	V_{R2SW1}	-0.3	–	7.0	V	–	P_3.1.39
R2SW2	V_{R2SW2}	-0.3	–	7.0	V	–	P_3.1.40
R2PG1	V_{R2PG1}	-0.3	–	0.3	V	–	P_3.1.41
R2PG2	V_{R2PG2}	-0.3	–	0.3	V	–	P_3.1.42
R2FB	V_{R2FB}	-0.3	–	7.0	V	–	P_3.1.43
R3SW1	V_{R3SW1}	-0.3	–	7.0	V	–	P_3.1.44
R3PG1	V_{R3PG1}	-0.3	–	0.3	V	–	P_3.1.45
R3FB	V_{R3FB}	-0.3	–	7.0	V	–	P_3.1.46
VM1FB	V_{VM1FB}	-0.3	–	6.0	V	–	P_3.1.47
VM1EN	V_{VM1EN}	-0.3	–	6.0	V	–	P_3.1.48
VM2FB	V_{VM2FB}	-0.3	–	6.0	V	–	P_3.1.49
VM2EN	V_{VM2EN}	-0.3	–	6.0	V	–	P_3.1.50
ROT	V_{ROT}	-0.3	–	6.0	V	–	P_3.1.51
TM2	V_{TM2}	-0.3	–	6.0	V	–	P_3.1.52
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_3.1.53
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.9
ESD susceptibility							
ESD susceptibility all pins	$V_{ESD,HBM}$	-2	–	2	kV	HBM[3)]	P_4.1.10
ESD susceptibility all pins	$V_{ESD,CDM}$	-500	–	500	V	CDM[4)]	P_4.1.12
ESD susceptibility of corner pins to GND	$V_{ESD,Corner}$	-750	–	750	V	CDM[4)]	P_4.1.13

1) Not subject to production test, specified by design.
2) Maximum rating is extended to 40 V for an overall time of 7 minutes during the lifetime of the product (load dump requirement)
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)
4) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	V_{R1VSx}	5.0	–	35	V	1)	P_3.2.1
Supply Voltage Range for Reduced Operation	V_{R1VSx}	3.7	–	5.0	V	1)2)	P_4.2.5
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.9

1) When first powered up, a proper startup of the device can only be assured by applying minimum 6 V at pins R1VSx for at least 2 ms. The device may start at even lower voltages.

2) The current capability of Buck1 is reduced to limit the current stress in the device.

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	–	12.2	K/W	–	P_4.3.1
Junction to soldering point (pin)	R_{thJSP}	20.1	–	22.1	K/W	JEDEC 2s2p, measured to pin 1, 3, 17, 18, 19, 21	P_3.3.1
Junction to soldering point (pin)	R_{thJSP}	34.9	–	37.6	K/W	JEDEC 1s0p, measured to pin 1, 3, 17, 18, 19, 21	P_3.3.2
Junction to soldering point (soldering pad)	R_{thJSP}	11.0	–	14.7	K/W	JEDEC 2s2p	P_3.3.3
Junction to soldering point (soldering pad)	R_{thJSP}	13.1	–	18.0	K/W	JEDEC 1s0p	P_4.3.2
Junction to ambient	R_{thJA}	–	37	–	K/W	[2)]	P_4.3.3

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip and Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3.4 Quiescent current consumption

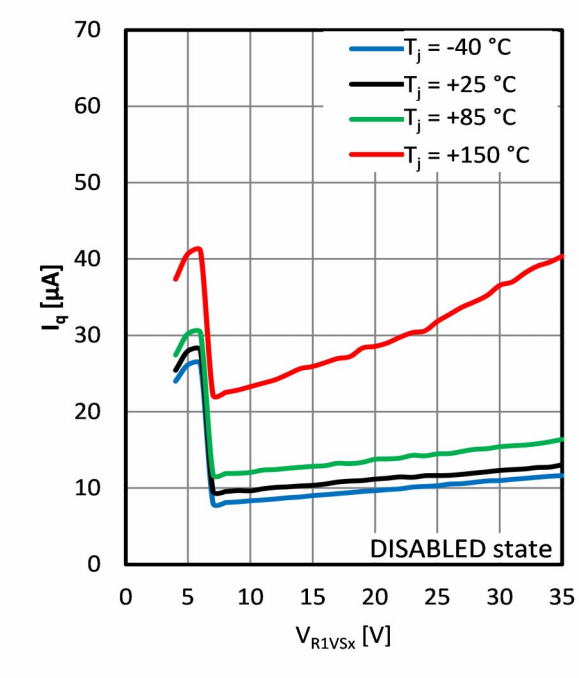
Table 4 Quiescent current consumption

T_j = -40°C to 150°C, V_{R1VSx} = 9 V to 25 V (unless otherwise specified)

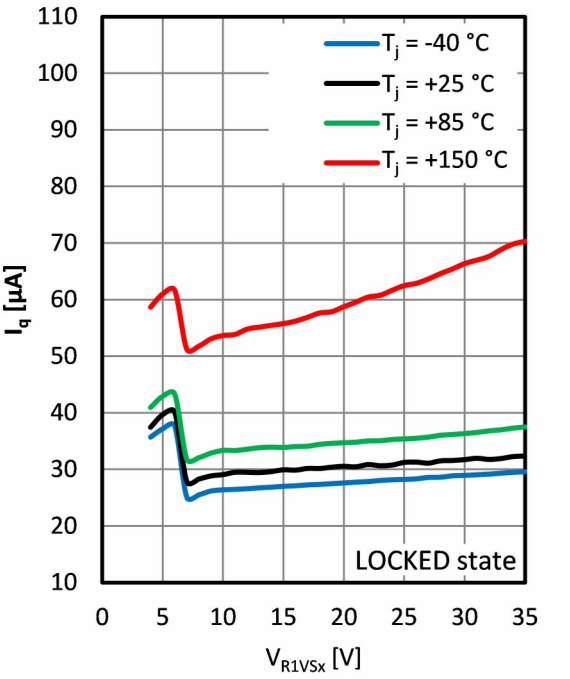
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ACTIVE state	$I_{q,OP}$	–	–	20	mA	$T_j \le 85°C$ $9\ V \le V_{R1VSx} \le 25\ V$ No load, Watchdog disabled	P_3.4.1
DISABLED state	$I_{q,DIS}$	–	13	17.5	µA	$T_j \le 85°C$ $9\ V \le V_{R1VSx} \le 25\ V$	P_3.4.2
DISABLED state	$I_{q,DIS}$	–	11	13.5	µA	$T_j = 25°C$ $V_{R1VSx} = 13.5\ V$	P_3.4.3
FAULT state	$I_{q,FLT}$	–	1	2	mA	$T_j \le 85°C$ $9\ V \le V_{R1VSx} \le 25\ V$	P_3.4.4
LOCKED state	$I_{q,LCK}$	–	35	50	µA	$T_j \le 85°C$ $9\ V \le V_{R1VSx} \le 25\ V$	P_3.4.5

3.4.1 Typical performance characteristics

DISABLED state - Quiescent current consumption I_q versus supply voltage V_{R1VSx}



LOCKED state - Quiescent current consumption I_q versus supply voltage V_{R1VSx}



4 Power converters and power management

4.1 High voltage step-down regulator – Buck1

4.1.1 Functional description Buck1

The high-voltage step-down regulator (Buck1) converts the battery voltage (R1VSx) to the Buck1 voltage.

A synchronous current-mode-controlled buck converter with internal power switches is integrated for this purpose. The output rail VBuck1 can be used as direct supply rail as well as pre-regulated rail for post-regulators.

The N-/N-MOS power stage is driven by an integrated driver circuit supplied by an external boot-strap capacitor. The integrated dead-time optimization prevents cross-conduction, minimizes dead-time and increases system efficiency. The output voltage is set with an internal voltage divider. Internal compensation allows for fast loop performance across a wide range of output capacitance. External tuning of the loop is not required. The design supports both ceramic and electrolytic capacitors. For detailed information on the selection of the external power stage components, namely the inductor and input/output filter capacitors, please refer to **Chapter 10**.

The converter offers various configuration options. It offers a selectable switching frequency, which can be configured via the SPI. Synchronization of the switching frequency with the other integrated converters as well as an external synchronization signal is included. Various protection features, such as overcurrent and overtemperature detection, prevent damage to the converter due to fault conditions.

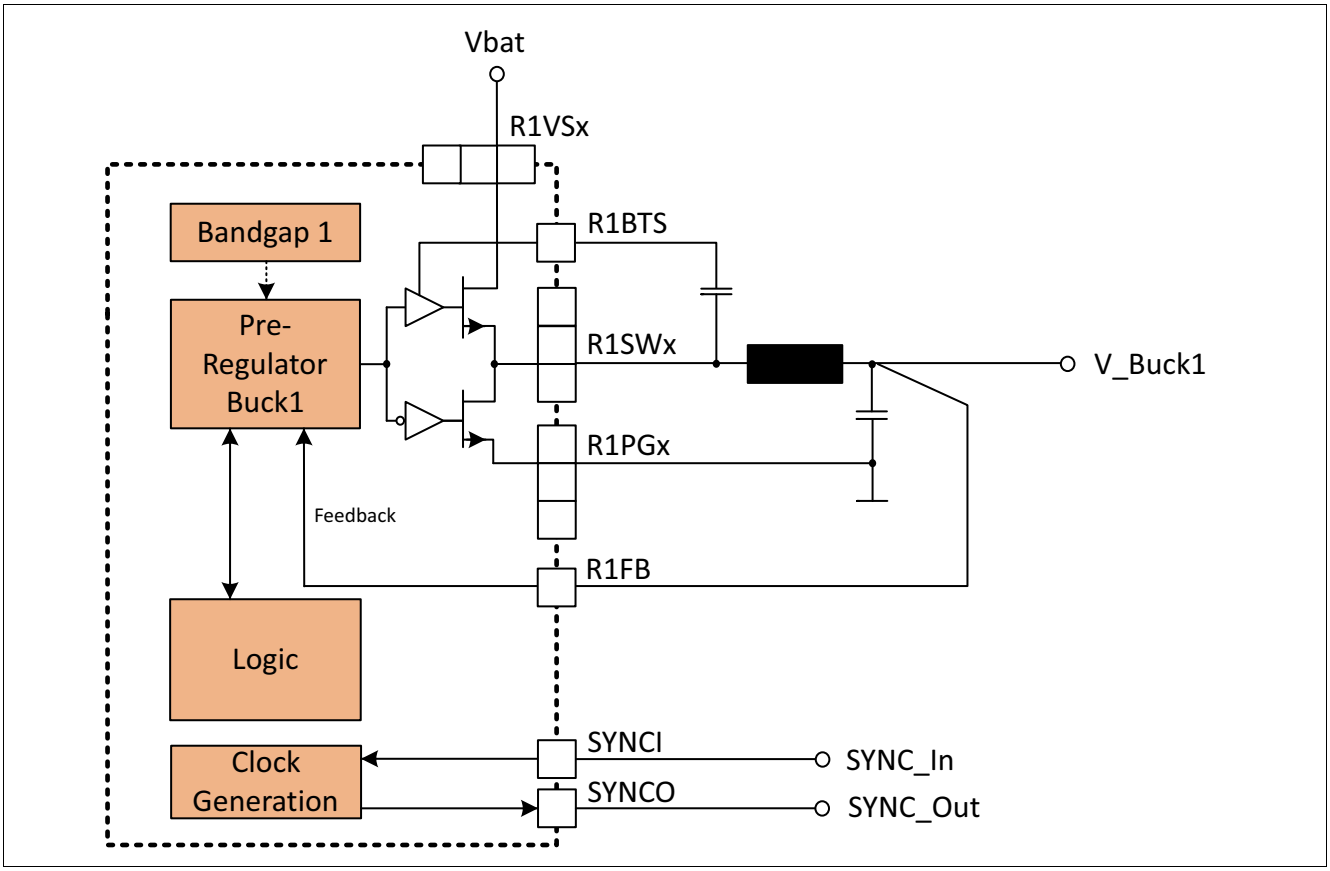


Figure 3 Block Diagram Buck1

Modulation concept

The converter uses several modulation schemes depending on the operation mode. A PWM scheme is used for most of the operating area. It supports synchronization to internal and external clock sources. For light-load and high-line operation, pulse-skipping operation is used. This allows for an improved system efficiency and ensures a minimum turn-on time to ensure correct operation of the switches.

The transition between PWM and pulse-skipping is automatically handled by the converter and does not require any configuration. The current and voltage thresholds for this transition are dependent on the selected power stage components.

Loop compensation

The converter uses a cascaded current-mode, voltage-mode control scheme. The inductor current is controlled by an inner current-loop, while the output voltage is regulated by the external voltage compensation loop. The compensation loop can operate with a range of power stages. For detailed information on the selection of the external components, please refer to **Chapter 10**. The dynamic performance of the system is a function of the power stage components and the internal compensation loop. Follow the design considerations in **Chapter 10** for optimum performance.

Cycle-by-cycle current limitation

The device features cycle-by-cycle current limitation to protect the switches and external components in case of a fault condition. If a defined current threshold is reached, then the peak current monitoring turns off the high-side switch. The device also monitors the current in the low side switch. If the current in the low side switch exceeds the overcurrent threshold at the end of the switching period, then the high side switch is not turned on in the following switching period. This allows the device to work as a constant current source.

If the current in the inductor exceeds the overcurrent protection threshold for a defined time, T_{R1OCP}, then an overcurrent time-out event is signalized with an interrupt (**OCSF1**.**BUCK1OCW**). It is up to the user to decide, how to react in this situation, for example by shutting down the converter.

Overtemperature protection

The converter includes an overtemperature warning and shutdown function to protect the device against damage. If the junction temperature exceeds the overtemperature warning threshold, an overtemperature warning flag is set (**OTSF1**.**BUCK1OTW**) and an interrupt is generated. If the junction temperature continues to rise and exceeds the overtemperature shutdown threshold, then the converter shuts down and generates a thermal shut-down (TSD) event. The **OTSF0**.**BUCK1OT** status flag is set and can be read by the microcontroller after re-entering ACTIVE state.

The current status of the overtemperature warning can be accessed at **OTSTAT0**.**BUCK1OTW**, while **OTSF1**.**BUCK1OTW** contains the latched information.

Soft-start

The integrated soft-start feature limits the in-rush current and allows for smooth start-up of the converter. Power-sequencing together with the other output rails is supported. Please refer to **Chapter 5.3** for more information.

4.1.2 Electrical characteristics Buck1

Table 5 Electrical characteristics Buck1

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage - TLF30682 S01	V_{R1VSx}	3.7	12	35	V	V_{R1FB} = 3.3 V	P_4.1.2.1
Output voltage – TLF30682 S01	V_{R1FB}	–	3.3	–	V	–	P_4.1.2.2
Output voltage tolerance	$V_{R1FB,TOL}$	-2	–	+2	%		P_4.1.2.9
Maximum output current	I_{R1IOUT}	3.5	–	–	A	5.0 V ≤ V_{R1VSx} ≤ 35 V	P_4.1.2.10
Maximum output current – derated	$I_{R1IOUT,DR}$	2.0	–	–	A	3.7 V ≤ V_{R1VSx} < 5.0 V	P_4.1.2.11
High-side switch on-resistance	$R_{DSOn,R1HS}$	45	77	145	mΩ	5.0 V ≤ V_{R1VSx} ≤ 35 V	P_4.1.2.16
High-side switch on-resistance derated	$R_{DSOn,R1HS,DR}$	–	–	160	mΩ	3.7 V ≤ V_{R1VSx} < 5.0 V	P_4.1.2.17
Low-side switch on-resistance	$R_{DSOn,R1LS}$	35	72	135	mΩ	5.0V ≤ V_{R1VSx} ≤ 35 V	P_4.1.2.18
Low-side switch on-resistance derated	$R_{DSOn,R1LS,DR}$	–	–	150	mΩ	3.7V ≤ V_{R1VSx} < 5.0 V	P_4.1.2.19
		–	–	–		–	P_4.1.2.20
Overcurrent protection threshold	I_{R1OCP}	4.1	4.5	6.0	A	–	P_4.1.2.21
Overcurrent time out	t_{R1OCP}	95	100	115	µs	–	P_4.1.2.23
		–	–	–		–	P_4.1.2.24
Minimum ON time		50	58	72	ns	Minimum ON time for internal HS control signal. The actual ON time on the R1SWx pins depends on the application design.	P_4.1.2.25
Overtemperature warning threshold	$T_{j,R1OT,WRN}$	130	145	160	°C	[1] T_j increasing	P_4.1.2.26
Overtemperature warning threshold	$T_{j,R1OT,WRN}$	120	135	150	°C	[1] T_j decreasing	P_4.1.2.27
Overtemperature shutdown threshold	$T_{j,R1OT,FLT}$	175	190	205	°C	[1] T_j increasing	P_4.1.2.28
Overtemperature shutdown threshold	$T_{j,R1OT,FLT}$	165	180	195	°C	[1] T_j decreasing	P_4.1.2.29
Bootstrap capacitor	C_{R1BST}	–	100	–	nF	–	P_4.1.2.30

Table 5 Electrical characteristics Buck1 (cont'd)

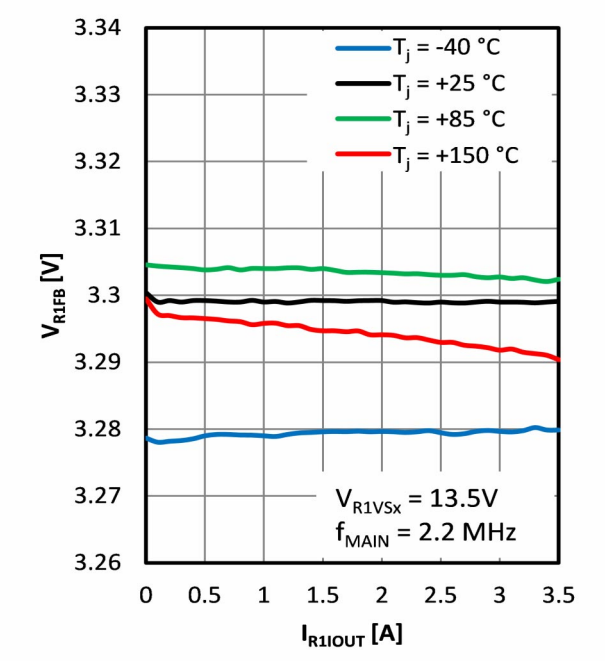
T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
External power stage components							
Effective inductance	L_{R1}	2.64	3.3	4.0	µH	2)	P_4.1.2.33
Effective output capacitance	C_{R1}	75	100	240	µF	2)3)	P_4.1.2.35
ESR of output capacitance	R_{R1C}	1	5	30	mΩ	–	P_4.1.2.36

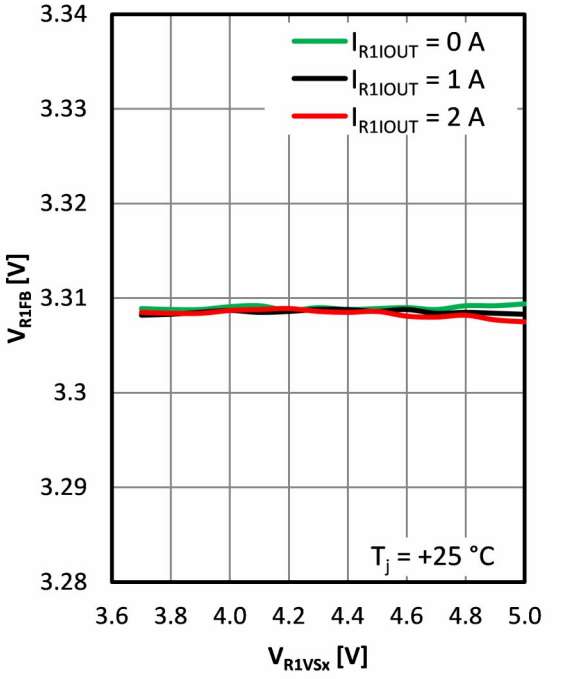
1) Not subject to production test, specified by design.
2) See **Chapter 10** for additional information on the allowed L,C combinations.
3) Effective capacitance including de-rating over the temperature range, bias voltage and aging. Electrolytic and ceramic capacitors are supported.

4.1.2.1 Typical performance characteristics

Buck1 output voltage V_{R1FB} versus load current I_{R1IOUT}



Buck1 output voltage V_{R1FB} versus supply voltage V_{R1VSx} (drop-out region)



4.2 Post-regulator step-down converter – Buck2

4.2.1 Functional description Buck2

The low-voltage step-down regulator (Buck2) converts the output voltage of Buck1 into the VBuck2 voltage.

A synchronous current-mode-controlled buck converter with internal P-/N-MOS power stage is integrated for this purpose. The output voltage is set with an internal voltage divider. Internal compensation allows for fast loop performance across a wide range of output capacitance. External tuning of the loop is not required. The design supports both ceramic and electrolytic capacitors. For detailed information on the selection of the external power stage components, namely the inductor and input/output filter capacitors, please refer to **Chapter 10**.

Synchronization of the switching frequency with the other integrated converters as well as an external synchronization signal is included. Various protection features, for example overcurrent, overtemperature and overvoltage detection, prevent damage to the converter due to fault conditions.

Loop compensation

Due to the integrated loop compensation no external components are required for loop compensation.

The dynamic performance of the system is a function of the power stage components and the internal compensation loop. Follow the design considerations in **Chapter 10** for optimum performance.

Cycle-by-cycle current limitation

The device features cycle-by-cycle current limitation to protect the switches and external components in case of a fault condition. If a defined current threshold is reached, then the peak current monitoring turns off the high-side switch. The device also monitors the current in the low side switch. If the current in the low side switch exceeds the overcurrent threshold at the end of the switching period, then the high side switch is not turned on in the following switching period. This allows the device to work as a constant current source.

If this operation mode persists for a defined time, an overcurrent time-out event, t_{R2OCP}, is signalized with an interrupt (**OCSF1.BUCK2OCW**). It is up to the user to decide how to react in this situation, by, for example shutting down the converter.

Overtemperature protection

The converter includes an overtemperature warning and shutdown function to protect the device against damage. If the junction temperature exceeds the overtemperature warning threshold, an overtemperature warning flag is set (**OTSF1.BUCK2OTW**) and an interrupt is generated. If the junction temperature continues to rise and exceeds the overtemperature shutdown threshold, then the converter shuts down and generates a thermal shut-down (TSD) event. The **OTSF0.BUCK2OT** status flag is set and can be read by the microcontroller after re-entering ACTIVE state.

The current status of the overtemperature warning can be accessed at **OTSTAT0.BUCK2OTW**, while **OTSF1.BUCK2OTW** contains the latched information.

Output voltage adjustment via SPI

The device features output voltage adjustment via SPI. Therefore, the microcontroller can adjust the output voltage during ACTIVE state using SPI registers (**B2VCTRL**, **B2VCTRLN**). Changes of the output voltage must be limited to 50 mV at a time. That means that the register value of **B2VCTRL** and **B2VCTRLN** must only be changed by +1 or -1. This is important to avoid false triggering of a Buck2 UV or Buck2 OV event. The settling time of the output voltage for a 50 mV step is typically 50 µs, but it may be longer depending on the output filter selection and load current condition.

Automatic use detection

The integrated automatic use detection for Buck2 allows the system to detect whether Buck2 is used in the application. Therefore, the input voltage on the R2VSx pins is checked prior to startup of Buck2. If the pins are connected to the output voltage, a voltage above the detection threshold is present at the pins and the device assumes that Buck2 is required in the application. To indicate to the device that Buck2 is not required in the application, the R2VSx pins should be connected to R2PGx.

The result of the detection is stored in **HWDECT0.BUCK2AVA** in order to allow the microcontroller to verify correct detection for the specific application and to differentiate the result from a possible fault present on the PCB.

Soft-start

The integrated soft-start feature limits the in-rush current and allows for smooth start-up of the converter. Power-sequencing together with the other output rails is supported. Please refer to **Chapter 5.3** for more information.

4.2.2 Electrical characteristics Buck2

Table 6 Electrical characteristics Buck2

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_{R2VSx}	2.9	V_{R1FB}	4.0	V		P_4.2.2.1
Output voltage adjustment range	$V_{R2FB,RANGE}$	0.9	–	1.3	V	–	P_4.2.2.3
Output voltage adjustment step size	$V_{R2FB,STEP}$	–	50	–	mV	$V_{R2FB} = V_{R2FB,RANGE}$	P_4.2.2.4
Default output voltage TLF30682 S01	V_{R2FB}	–	1.25	–	V	–	P_4.2.2.5
Output voltage tolerance	$V_{R2FB,TOL}$	-2	–	+2	%	–	P_4.2.2.10
Maximum output current	I_{R2IOUT}	2.0	–	–	A	–	P_4.2.2.11
High-side switch on-resistance	$R_{DSOn,R2HS}$	60	113	180	mΩ	V_{R2VSx} = 3.3 V	P_4.2.2.15
Low-side switch on-resistance	$R_{DSOn,R2LS}$	35	80	140	mΩ	V_{R2VSx} = 3.3 V	P_4.2.2.16
		–	–	–		–	P_4.2.2.17
Overcurrent protection threshold	$I_{R2,OCP}$	2.9	3.45	4.0	A	–	P_4.2.2.18
Overcurrent time out	$t_{R2,OCP}$	95	100	115	µs	–	P_4.2.2.20
		–	–	–		–	P_4.2.2.21
Minimum ON time		64	79	87	ns	Minimum ON time for internal HS control signal. The actual ON time on the R2SWx pins is dependent on the application design.	P_4.2.2.22
Overtemperature warning threshold	$T_{j,R2OT,WRN}$	130	145	160	°C	[1] T_j increasing	P_4.2.2.23
Overtemperature warning threshold	$T_{j,R2OT,WRN}$	120	135	150	°C	[1] T_j decreasing	P_4.2.2.24
Overtemperature shutdown threshold	$T_{j,R2OT,FLT}$	175	190	205	°C	[1] T_j increasing	P_4.2.2.25
Overtemperature shutdown threshold	$T_{j,R2OT,FLT}$	165	180	195	°C	[1] T_j decreasing	P_4.2.2.26
External power stage components							
Effective inductance	L_{R2}	1.2	2.2	4.0	µH	[2]	P_4.2.2.28

Table 6 Electrical characteristics Buck2 (cont'd)

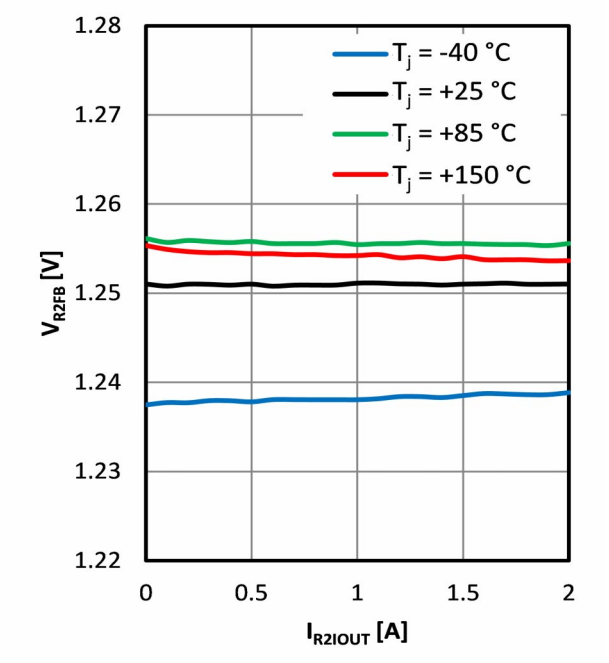
T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Effective output capacitance	C_{R2}	52	66	120	µF	2)3)	P_4.2.2.30
ESR of output capacitance	R_{R2C}	1	5	30	mΩ	–	P_4.2.2.31

1) Not subject to production test, specified by design.
2) See **Chapter 10** for additional information on the allowed L, C combinations.
3) Effective capacitance including de-rating across temperature range, bias voltage and aging. Electrolytic and ceramic capacitors are supported.

4.2.2.1 Typical performance characteristics

Buck2 output voltage V_{R2FB} versus load current I_{R2IOUT}



4.3 Post-regulator step-up converter – Boost1

4.3.1 Functional description Boost1

The device integrates a dedicated step-up converter to generate a 5 V output voltage rail from the Buck1 voltage. An asynchronous boost topology with internal low-side switch and an external diode is used.

Loop compensation

The Boost1 converter uses an internal compensation circuit with no need for external components.

For selection of the required external components please refer to **Chapter 10**.

Synchronization of the switching frequency with the other integrated converters as well as an external synchronization signal is included.

Overcurrent protection

The device incorporates an overcurrent protection to protect the internal low-side switch of the boost converter. Due to the nature of the boost topology the boost output rail is not protected against a short circuit directly. However, indirect protection via an undervoltage protection and current limitation of the front-end converter (Buck1) is available.

Automatic use detection

An automatic use detection is implemented for Boost1 which allows the system to detect if Boost1 is used in the application. Therefore, the input voltage on the R3FB pin is checked prior to startup of Boost1. If the R3FB pin is connected to the output voltage of Buck1 through the boost inductor and rectifying diode, a voltage above the detection threshold is present at the pin and the device assumes that Boost1 is required in the application. To indicate to the device that Boost1 is not required in the application, the R3FB pin should be connected to R3PG. The result of the detection is stored in **HWDECT0.BOOST1AVA** in order to allow the microcontroller to verify correct detection for the specific application and differentiate the result from a possible fault present on the PCB.

4.3.2 Electrical characteristics Boost1

Table 7 Electrical characteristics Boost1

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

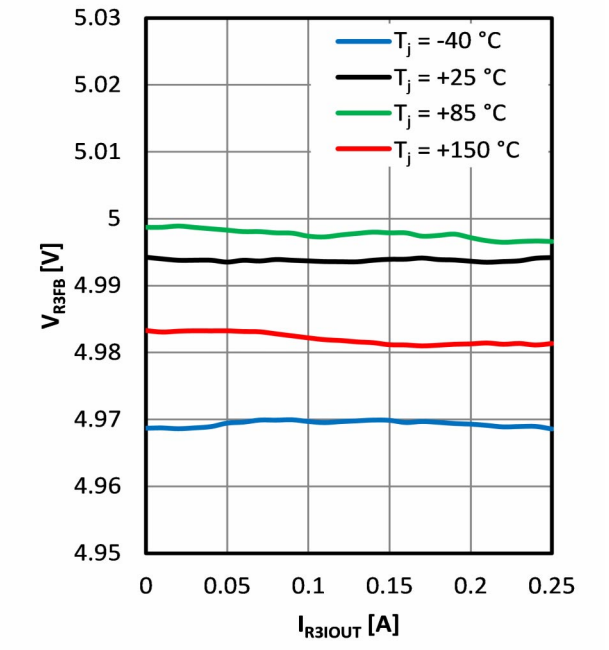
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_{R3VS}	2.7	V_{R1FB}	4.5	V	–	P_4.3.2.1
Output voltage	V_{R3FB}	–	5.0	–	V	–	P_4.3.2.2
Output voltage tolerance	$V_{R3FB,TOL}$	-2	–	2	%	–	P_4.3.2.3
Maximum output current	I_{R3IOUT}	250	–	–	mA	–	P_4.3.2.4
Overcurrent detection threshold	$I_{R3,OCP}$	740	820	900	mA	–	P_4.3.2.5
Overcurrent time out	$t_{R3,OCP}$	170	220	260	µs	–	P_4.3.2.6
External power stage components							
Effective inductance	L_{R3}	3.8	6.8	9.8	µH	1)	P_4.3.2.8
Effective output capacitance	C_{R3}	5.5	10	18	µF	1)2)	P_4.3.2.10
ESR of output capacitance	R_{R3C}	1	20	50	mΩ	–	P_4.3.2.11

1) See **Chapter 10** for additional information on the allowed L, C combinations.

2) Effective capacitance including derating over the temperature range, bias voltage and aging. Electrolytic and ceramic capacitors are supported.

4.3.2.1 Typical performance characteristics

Boost1 output voltage V_{R3FB} versus load current I_{R3IOUT}



4.4 Support of external voltage rails

The device supports monitoring of two externally generated voltage rails via voltage monitors. Each voltage monitor consists of an enable pin (VMxEN) to control the respective regulator and a monitoring input pin (VMxFB) for monitoring the respective voltage rail. The expected voltage on the monitoring input is fixed. If higher voltages should be monitored, an external voltage divider may be used to reduce the voltage to the expected range.

Automatic use detection

The integrated automatic use detection for each voltage monitor allows the system to detect whether it is used in the application.

The device assumes that an external power regulator is connected (and the voltage monitoring is used) when it is possible to drive the respective enable pin "high". Conversely, to indicate to the device that a voltage monitor is not required by the application, the respective enable pin VMxEN should be connected to ground. The result of the detection is stored in **HWDECT0.VM1AVA** and **HWDECT0.VM2AVA** respectively, in order to allow the microcontroller to verify correct detection for the specific application and differentiate the result from a possible fault condition on the PCB.

Table 8 Electrical characteristics external voltage rails

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable signal: VMxEN							
Output level – "high"	$V_{VMxEN,high}$	0.7	–	–	V_{IOVDD}	I_{VMxEN} = -7 mA	P_4.4.0.1
Output level – "low"	$V_{VMxEN,low}$	–	–	0.7	V	I_{VMxEN} = -5.5 mA	P_4.4.0.2
Internal pull-down current	I_{VMxEN}	10	–	–	µA	V_{VMxEN} = 0.8 V	P_4.4.0.3
Monitoring signals: VMxFB							
Nominal input voltage[1)]	$V_{VMxFB,nom}$	–	0.8	–	V	–	P_4.4.0.4
Input pull-up current	I_{VMxFB}	–	100	130	nA	V_{VMxFB} = 0.8 V	P_4.4.0.5

1) For information on the monitoring thresholds please refer to **Table 14** in **Chapter 6.1.3**.

5 Central functions

5.1 Supply voltages

The device generates an internal supply voltage from the voltage supplied at the R1VSx pins. This supply voltage, R1BTSV, is used to power the driver circuit for the power switches of Buck1. It cannot be used to supply any external loads in the system.

To handle the dynamic gate drive current of the power switches, a ceramic capacitor for decoupling must be placed between R1BTSV and the respective ground pin.

In order to operate the digital outputs of the device, a supply voltage is required at the IOVDD pin. Please refer to **Chapter 7.1** for detailed information.

Table 9 Electrical characteristics supply voltages

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Decoupling capacitor for internal supply							
Internal supply decoupling – connect between R1BTSV and GND		0.8	1.0	1.2	µF	–	P_5.1.1

5.2 Enable functionality

The device features an enable functionality which allows powering up the device using the ENA pin. For example, this pin may be connected to the outside of the ECU or to a wake output of a CAN transceiver.

The pin is level-sensitive with a duration-based de-glitching where a "high" signal indicates the "enabled" state. With respect to **Figure 4**, the enable signal is considered "high", when it is above the enable detection threshold $V_{ENA,high}$ for a minimum time of $t_{ENA,det}$. A signal above the detection threshold for a duration shorter than $t_{ENA,filt}$ is not considered a valid "high" signal.

Respectively, the enable signal is considered "low" when it is below $V_{ENA,low}$ for a minimum time of $t_{ENA,det}$. A signal below the detection threshold for a duration shorter than $t_{ENA,filt}$ is not considered a valid "low" signal. The state of the enable signal can be accessed at **VMONSTAT0.ENA**.

The device incorporates an enable event detection where a "low-to-high" transition or a "high-to-low" transition of the enable signal is considered an enable event. Upon detection of an enable event, an interrupt is generated (**SYSSF1.ENA**). Depending on the device state, an enable event may trigger a state transition (refer to **Chapter 8.3**), for example power up the device.

An enable event does not disable the device automatically. It is up to the microcontroller to react to the generated interrupt and react accordingly.

The state of the enable signal can be accessed at **VMONSTAT0.ENA** and may be used by the microcontroller to determine the current state of the enable signal. This information may be used to differentiate between an enable or disable condition on ECU level.

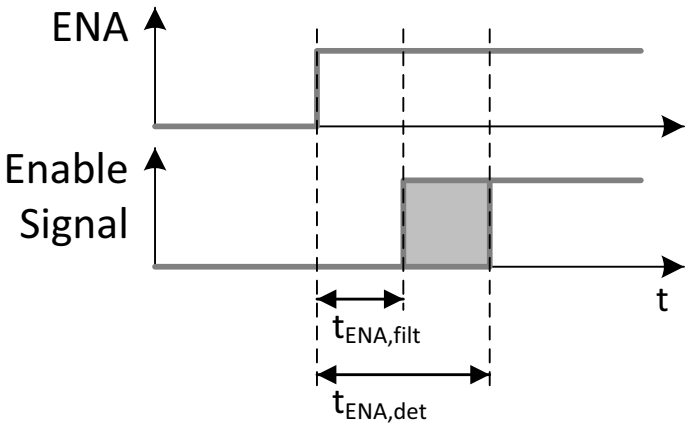


Figure 4 Enable signal – timing enable event

5.2.1 ENA pin configurability

The ENA pin is by default configured to be edge triggered. The device can only detect an ENA event if the voltage on the pin rises from a low level to a high level. The functionality of the ENA pin can be configured by the microcontroller as edge-triggered or level-sensitive in register **DEVCFG0.ENA_CONFIG**.

If the configuration of the ENA pin is set to level-sensitive, then the device automatically re-enters the ACTIVE state from the FAULT state if the ENA pin is high. That means that the device does not enter the LOCKED state after three consecutive faults with the ENA pin configured to level-sensitive as long as the ENA pin is high.

If the device enters the DISABLED state on an SPI request to **DEVCTRL**/**DEVCTRLN**, then the **DEVCFG0** register is reset to the default value. The device can therefore only recognize an ENA event in DISABLED state if the ENA pin has a low to high transition.

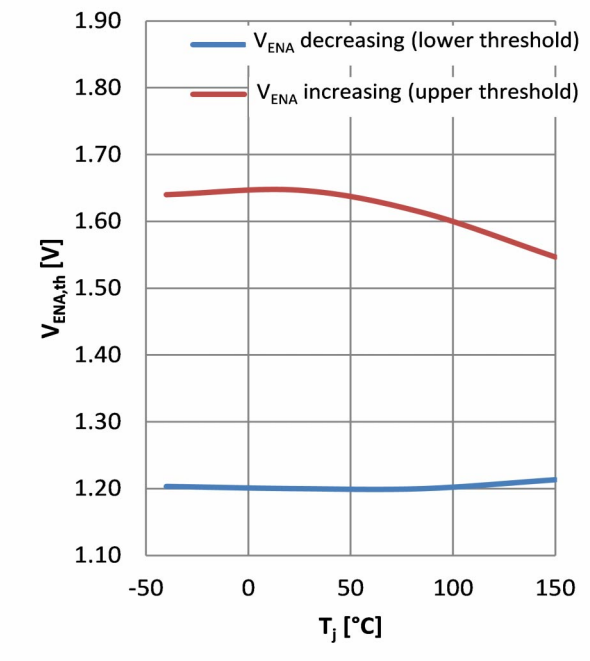
Table 10 Electrical characteristics enable signal

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable signal – pin ENA							
Input level – "high"	$V_{ENA,high}$	1.30	1.60	2.00	V	V_{ENA} increasing	P_5.2.1
Input level – "low"	$V_{ENA,low}$	1.00	1.20	1.40	V	V_{ENA} decreasing	P_5.2.2
Input hysteresis	$V_{ENA,hys}$	250	400	550	mV	–	P_5.2.3
Input current – "high"	$I_{ENA,high}$	–	3	5	µA	$V_{ENA} \geq 2V$	P_5.2.4
Input current – "low"	$I_{ENA,low}$	–	–	0.1	µA	$V_{ENA} \leq 1V$	P_5.2.5
Enable signal, filtering time	$t_{ENA,filt}$	–	–	20	µs	–	P_5.2.6
Enable signal, detection time	$t_{ENA,det}$	40	–	–	µs	–	P_5.2.7

5.2.2 Typical performance characteristics

ENA pin input levels V_{ENA} versus junction temperature T_j



5.3 Power sequencing and soft-start

The individual output rails are power sequenced to reduce the in-rush current during power-up. A passive power sequencing method is used where the individual rails are enabled when the preceding rail is within its total operating band, that is between the respective undervoltage and overvoltage fault thresholds.

Sequence of the output rails:

- Buck1
- Buck2, Boost1
- (VM1), (VM2)

Power sequencing is active any time a power rail is enabled or disabled, for example at the transition into ACTIVE.

In case a rail is not active, that is the automatic use detection has detected that a rail is not used, this rail is skipped during the power sequencing and the subsequent rail is enabled.

Two conditions must to be fulfilled before the power sequence can proceed to the next stage:

- The output voltage on the individual rails must be above the undervoltage threshold
- The rise time must be completed before the next stage is reached

For example when Buck1 is ramped up the device waits until the output voltage is above the undervoltage threshold and the rise time t_{Buck1} has elapsed before it initiates the ramping of Buck2 and Boost1. Under normal operating conditions the output voltage on Buck1, Buck2 and Boost1 will cross their respective undervoltage thresholds before the rise time has elapsed.

The undervoltage monitoring is enabled as soon as the corresponding rail is enabled. However, the undervoltage event is only indicated once the voltage rail has crossed the undervoltage threshold for the first time. The short-to-ground detection is active and used as a time out function for the power sequencing, this means that, if a voltage rail is not valid within the short-to-ground detection time, a fault event is indicated. Depending on the configured response to the short-to-ground event (see **Table 25**), the device may either move into a different state or continue operation and sequencing.

The overvoltage monitoring is active as soon as the corresponding rails is enabled.

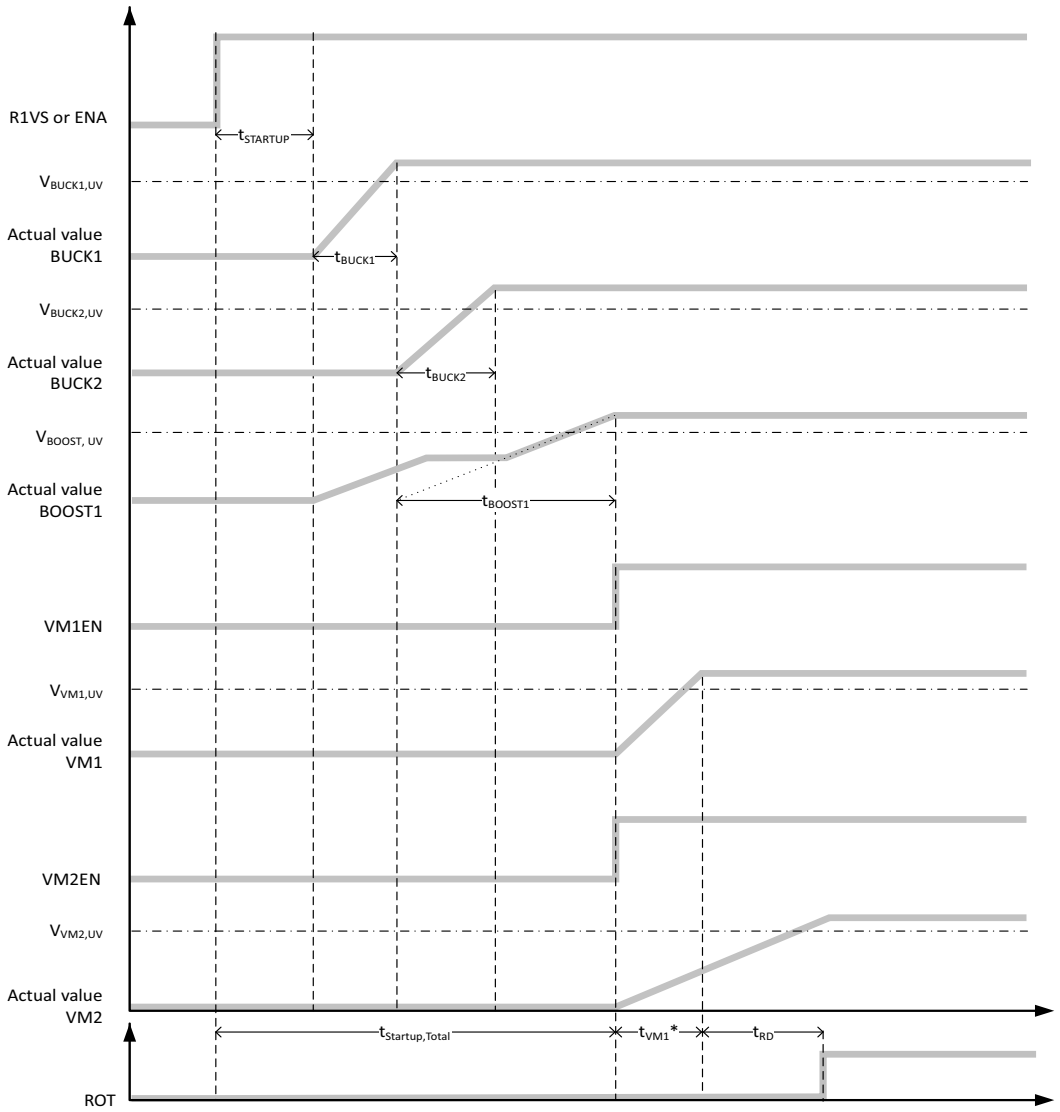


Figure 5 Power sequencing

The microcontroller reset signal is released with a configurable delay once the microcontroller supply voltage is within the operating band for a selectable time period (**DEVCFG0.RESDEL**). For generation of the microcontroller reset signal (ROT), please refer to **Chapter 7.3**.

The external voltage regulator monitored by VM1 must have a rise time, t_{VM1}, that is shorter than the short-to-ground detection time, $t_{VM1,StG}$ (see **Table 14**).

Table 11 Electrical characteristics power sequencing

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal device start up time	$t_{STARTUP}$	–	300	–	µs	–	P_5.3.1
Output voltage rise time Buck1	t_{BUCK1}	–	320	–	µs	V_{BUCK1} = 3.3 V	P_5.3.2

Table 11 Electrical characteristics power sequencing (cont'd)

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage rise time Buck2	t_{BUCK2}	–	320	–	µs	V_{BUCK2} = 1.25 V	P_5.3.4
Output voltage rise time Boost1	t_{BOOST1}	–	640	–	µs	V_{BUCK1} = 3.3 V, V_{BOOST1} = 5.0 V	P_5.3.5

5.4 Switching frequency generation and clock synchronization

The switching frequencies for the different integrated converters are generated by an integrated clock generation and a clock manager. Synchronization to an external clock signal as well as generation of the synchronization signal for external circuits is supported. Spread spectrum modulation for EMC/EMI improvements is available for all converters.

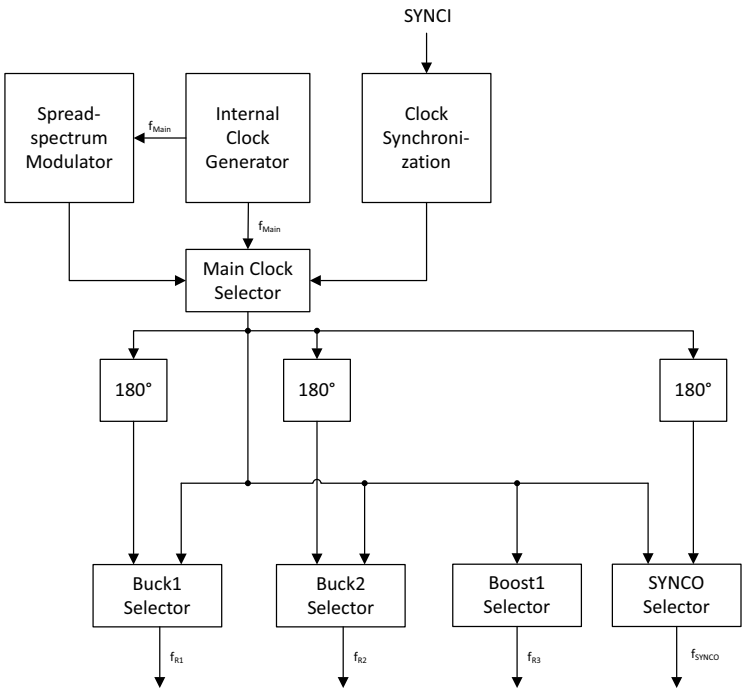


Figure 6 Clock generation and clock manager

Main frequency generation

Figure 6 shows that the internal clock generation uses an internal main frequency to derive the switching frequency for the power converters and the external synchronization signal. The main frequency of the system can be adjusted using **CLKCFG1** within a given range.

Synchronization

The power converters can be synchronized to an external clock signal (SYNCI) to improve EMC/EMI performance and reduce cross-talk to the loads.

Table 12 shows the specification of the signal. The clock manager synchronizes the switching frequency to this signal according to the configuration in the SPI registers. The synchronization functionality is disabled by default.

To enable synchronization of the switching frequency, an external reference signal is required at the SYNCI pin and the synchronization functionality must be enabled via SPI. The external clock source must not be removed while the device is running in synchronized mode.

The device supports a dynamic change of the synchronization frequency during synchronization mode with minimal disturbance of the output voltage. It is recommended to keep the same phase and change the switching frequency with the next rising edge of the synchronization signal to minimize the impact on the output voltage. The output voltage settles within a maximum time of 50 µs.

In addition, the device features a synchronization output signal SYNCO, which can be used to synchronize an external switched-mode post-regulator. The output frequency is equal to the switching frequency of Buck1.

Central functions

The signal has a 50% duty cycle with a selectable phase shift of 0° or 180° with respect to the main clock. The synchronization output is disabled by default. The synchronization output can be enabled via SPI.

In addition, the phase shift between the individual converters can be adjusted using **CLKCFG0**. The phase shift is defined between rising edge of the clock signal and the rising edge of the switch node for the buck converters and the falling edge of the boost converter respectively. Furthermore the converters Buck1 and Buck2, as well as SYNCO can be controlled independently with a phase shift of 0° or 180° with respect to the main clock.

Spread-spectrum modulation

The device incorporates spread-spectrum modulation in order to improve EMC/EMI performance. The spread-spectrum modulation is applied to the main clock source, hence affects all power converters. The spread-spectrum modulation is disabled by default and can be enabled via SPI register **CLKCFG0.SSEN**.

Table 12 Electrical characteristics frequency generation

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal clock source							
Frequency	f_{MAIN}	1800	2200	2500	kHz	Switching frequency selectable via SPI	P_5.4.1
Frequency tolerance	$f_{MAIN,tol}$	-10	–	10	%	–	P_5.4.3
Frequency adjustment step size	$f_{MAIN,step}$	–	100	–	kHz	–	P_5.4.4
Synchronization input signal SYNCI[1)]							
Input level – "high"	$V_{SYNCI, high}$	0.7	–	–	V_{IOVDD}	V_{SYNCI} increasing	P_5.4.5
Input level – "low"	$V_{SYNCI, low}$	–	–	0.8	V	V_{SYNCI} decreasing	P_5.4.6
Input level hysteresis	$V_{SYNCI, hys}$	–	0.06	–	V_{IOVDD}	–	P_5.4.7
Input capacitance	C_{SYNCI}	–	4	15	pF	[2)]	P_5.4.8
Frequency range	f_{Sync}	1600	2200	2800	kHz	–	P_5.4.9
Duty cycle		40	50	60	%	–	P_5.4.10
Phase delay between SYNCIN and switching edges		–	30	–	ns	–	P_5.4.11
Output voltage settling time	t_{Sync}	–	–	50	µs	–	P_5.4.12
Synchronization output signal SYNCO[1)]							
Output level – "high"	$V_{SYNCO, high}$	0.7	–	–	V_{IOVDD}	I_{IOVDD} = -7 mA	P_5.4.13
Output level – "low"	$V_{SYNCO, low}$	–	–	0.7	V	I_{IOVDD} = -5.5 mA	P_5.4.14
Frequency		–	f_{MAIN}	–		–	P_5.4.15
Duty cycle		–	50	–	%	–	P_5.4.16
		–	–	–		–	P_5.4.17
		–	–	–		–	P_5.4.18
		–	–	–		–	P_5.4.19

Table 12 Electrical characteristics frequency generation (cont'd)

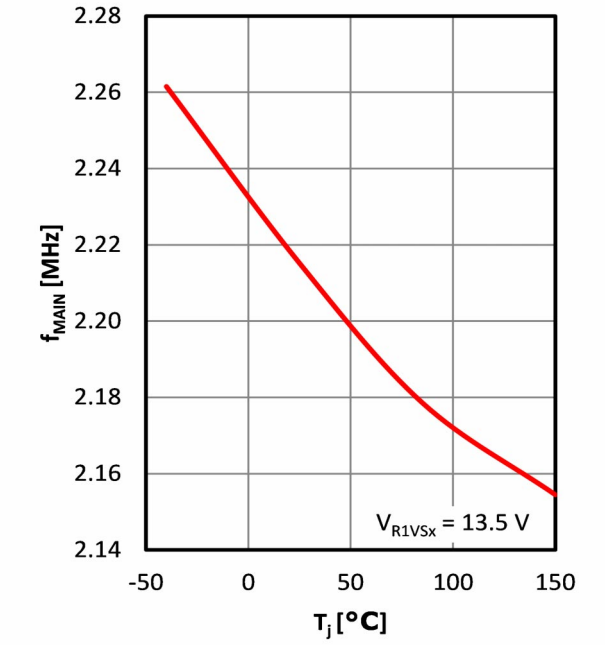
T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Spread spectrum modulation							
Maximum modulation variation from $f_{MAIN,Range}$		-7.5	–	7.5	%	5 steps	P_5.4.22
Modulation frequency		–	9	–	kHz	–	P_5.4.23

1) The voltage levels on this pin are dependent on the IOVDD supply voltage provided (see **Chapter 7.1**)
2) Not subject to production test, specified by design.

5.4.1 Typical performance characteristics

Switching frequency f_{MAIN} versus junction temperature T_j



5.5 IOVDD - Overvoltage and undervoltage detection

The IOVDD pin is the supply voltage input for the communication interface towards to the microcontroller. The pin can be supplied from one of the voltages generated by the TLF30682QVS01.

The TLF30682QVS01 monitors the voltage on the IOVDD pin. An overvoltage event or an undervoltage event triggers a reset and pulls ROT to GND. As long as no reset event occurs, ROT is "high" (V_{IOVDD}) due to an internal pull-up resistor and follows V_{IOVDD}. **Figure 7** shows an example of various events with delay and deglitching times.

In addition to the undervoltage and overvoltage detection the TLF30682QVS01 also features a short-to-ground detection for the IOVDD voltage. If the IOVDD voltage is below the undervoltage threshold for a period longer the short-to-ground detection time, then the device generates a short-to-ground event. A short-to-ground event on IOVDD triggers a hard reset in the device and the **SYSSF0.IOVDDUV**.

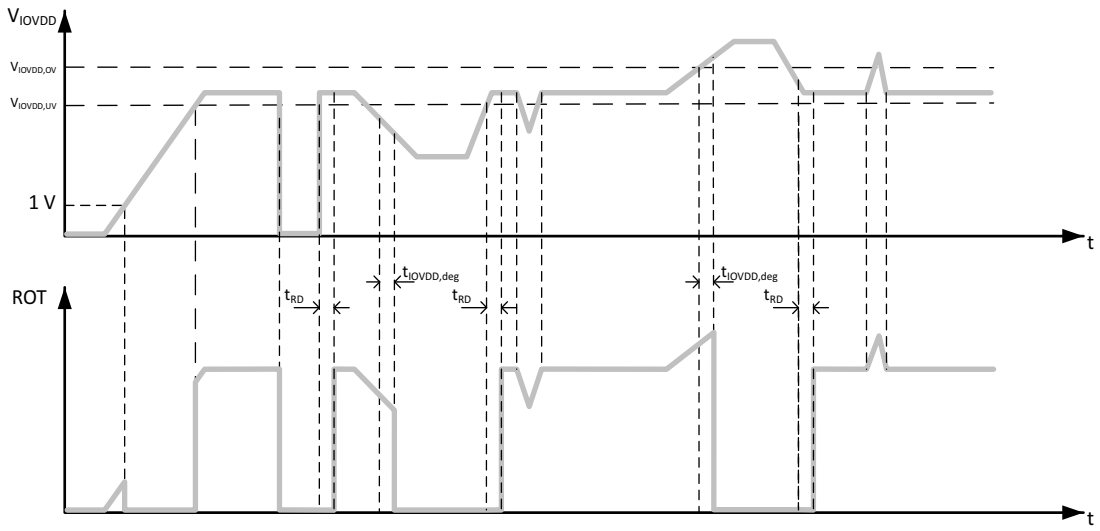


Figure 7 Overvoltage and undervoltage detection

Table 13 Electrical characteristics IOVDD - Overvoltage and undervoltage detection

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
IOVDD - Overvoltage threshold	$V_{IOVDD,OV}$	5.5	–	5.8	V		P_5.6.1
IOVDD - Overvoltage hysteresis	$V_{IOVDD,OV,Hys}$	0.4	–	2.25	%		P_5.6.2
IOVDD - Undervoltage threshold	$V_{IOVDD,UV}$	2.74	–	2.86	V		P_5.6.3
IOVDD - Undervoltage hysteresis	$V_{IOVDD,UV,Hys}$	0.4	–	2.25	%		P_5.6.4
Deglitching time	$t_{IOVDD,deg}$	8	–	20	µs		P_5.6.5
Short-to-ground detection time	$t_{IOVDD,StG}$	3.6	4.0	4.4	ms		P_5.6.6

6 Monitoring functions

The device incorporates various features for using the device as a supply backbone. These features include:

- Integrated voltage monitors for the output voltages, see **Chapter 6.1**.
- Integrated window watchdog for supervising microcontroller timing, see **Chapter 7.5**.

6.1 Voltage monitoring

6.1.1 Monitoring of R1VSx – battery supply

If the battery voltage drops below $V_{R1VSx,UV}$, then the undervoltage monitoring feature for R1VSx sets the SPI status flag **GSF**.**R1VSxUV**.

6.1.2 Monitoring of output voltages

The voltage monitoring function supervises the voltages on the feedback pins R1FB, R2FB and R3FB of the switched-mode converters with respect to the thresholds for undervoltage and overvoltage, see **Table 14**.

Signals exceeding the respective thresholds for a time shorter than the deglitching time are not detected as a fault event. When a signal exceeds a threshold for a duration longer than the deglitching time, an undervoltage event or an overvoltage event is generated. If the voltage is below the undervoltage threshold for a duration longer than the short-to-ground detection time, then the device additionally generates a short-to-ground event. In addition to the long short-to-ground detection time the monitoring also features deep undervoltage detection for Buck1 and Buck2. If the voltage on the feedback pins R1FB or R2FB drops below the deep undervoltage threshold for a duration longer than the deglitching time, then a short-to-ground event is generated.

Depending on the type of fault, the appropriate actions are executed as described in **Chapter 8.3**.

The voltage monitoring is activated automatically when the respective power rail is enabled. For information on the behavior during sequencing, please refer to **Chapter 5.3**.

6.1.3 Monitoring of external voltage rails

The device supports monitoring of two external voltage rails on the pins VM1FB, VM2FB. The external voltages are compared using window comparators against predefined thresholds. These thresholds define levels relative to the assumed nominal input voltage according to **Table 14**. Resistor dividers are to be used to map the output voltage of the respective voltage rail externally.

Signals exceeding the thresholds for a time shorter than the deglitching time are not detected as a fault event. When a signal exceeds the thresholds for a duration longer than the deglitching time, an undervoltage or an overvoltage event is generated. If the voltage is below the undervoltage threshold for a duration longer than the short-to-ground detection time, then the device generates an additional short-to-ground event.

Depending on the type of fault, the appropriate actions are executed as described in **Chapter 8.3**.

Voltage monitoring is enabled when the respective power rail is enabled. For information on the behavior during sequencing, please refer to **Chapter 5.3**.

If an overvoltage event or a short-to-ground event occurs, then the device shuts down the respective voltage rail to protect the load and the device.

6.1.4 Monitoring of internal supply voltages and bandgaps

The integrated voltage monitoring function monitors internal supply voltages in order to ensure proper operation. In case proper operation can not be ensured, the device reacts accordingly, see **Table 26**.

The device features two independent voltage references:

- for the voltage regulators
- for voltage monitoring

The device supervises the difference between the voltage references internally.

In case the difference exceeds a predefined warning threshold, the device generates an interrupt and sets one of the following status flags depending on the internal root cause: **SYSSF1.BGWARN1** or **SYSSF1.BGWARN2**. Based on this information the system can be designed to react appropriately.

In case the difference exceeds a predefined fault threshold the device will shut down and change into FAULT state, as proper operation of the device can not be ensured. **SYSSF0.BGFLT1** or **SYSSF0.BGFLT2** is set depending on the internal root cause.

6.1.5 Electrical characteristics

Table 14 Electrical characteristics voltage monitoring

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage battery supply – (R1VSx-AGx)							
Undervoltage threshold	$V_{R1VSx,UV}$	4.9	5.025	5.15	V	–	P_6.1.5.1
Output voltage Buck1 – (R1FB-AGx)							
Overvoltage threshold	$V_{Buck1,OV}$	+6.0	+8.0	+10	%	Referenced to Buck1 nominal output voltage V_{R1FB}	P_6.1.5.3
Overvoltage hysteresis	$V_{Buck1,OV,Hys}$	0.4	–	2.25	%		P_6.1.5.5
Undervoltage threshold	$V_{Buck1,UV}$	-6.0	-8.0	-10	%	Referenced to Buck1 nominal output voltage V_{R1FB}	P_6.1.5.7
Undervoltage hysteresis	$V_{Buck1,UV,Hys}$	0.4	–	2.25	%	–	P_5.2.1.6
Deep undervoltage threshold	$V_{Buck1,DUV}$	-38	-40	-42	%	–	P_6.1.5.9
Deep undervoltage hysteresis	$V_{Buck1,DUV,Hys}$	0.8		3.15	%	–	P_6.1.5.10
Deglitching time	$t_{Buck1,deg}$	8	-	20	µs	–	P_6.1.5.11
Short-to-ground detection time	$t_{Buck1,StG}$	2.7	3.0	3.3	ms	–	P_6.1.5.12
		–	–	–		–	P_6.1.5.13
		–	–	–		–	P_6.1.5.14

Table 14 Electrical characteristics voltage monitoring (cont'd)

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage Buck2- (R2FB-AGx)							
Overvoltage threshold	$V_{Buck2,OV}$	+6.0	+8.0	+10	%	Referenced to Buck2 nominal output voltage V_{R2FB}	P_6.1.5.16
Overvoltage hysteresis	$V_{Buck2,OV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.18
Undervoltage threshold	$V_{Buck2,UV}$	-6.0	-8.0	-10	%	Referenced to Buck2 nominal output voltage V_{R2FB}	P_6.1.5.20
Undervoltage hysteresis	$V_{Buck2,UV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.22
Deep undervoltage threshold	$V_{Buck2,DUV}$	-38	-40	-42	%	–	P_6.1.5.23
Deep undervoltage hysteresis	$V_{Buck2,DUV,Hys}$	0.8		3.15	%	–	P_6.1.5.24
Deglitching time	$t_{Buck2,deg}$	8	-	20	µs	–	P_6.1.5.25
Short-to-ground detection time	$t_{Buck2,StG}$	2.7	3.0	3.3	ms	–	P_6.1.5.26
Output voltage Boost1 – (R3FB-AGx)							
Overvoltage threshold	$V_{Boost1,OV}$	+6.0	+8.0	+10	%	Referenced to Boost1 nominal output voltage V_{R3FB}	P_6.1.5.28
Overvoltage hysteresis	$V_{Boost1,OV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.30
Undervoltage threshold	$V_{Boost1,UV}$	-6.0	-8.0	-10	%	Referenced to Boost1 nominal output voltage V_{R3FB}	P_6.1.5.32
Undervoltage hysteresis	$V_{Boost1,UV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.34
Deglitching time	$t_{Boost1,deg}$	8	-	20	µs	–	P_6.1.5.35
Short-to-ground detection time	$t_{Boost1,StG}$	2.7	3.0	3.3	ms	–	P_6.1.5.36
External voltage monitors VM1 (VM1FB-AGx)							
Overvoltage threshold	$V_{VM1,OV}$	+6.0	+8.0	+10	%	Referenced to VM1 nominal reference voltage $V_{VM1FB,nom}$	P_6.1.5.38
Overvoltage hysteresis	$V_{VM1,OV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.40

Table 14 Electrical characteristics voltage monitoring (cont'd)

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Undervoltage threshold	$V_{VM1,UV}$	-6.0	-8.0	-10	%	Referenced to VM1 nominal reference voltage $V_{VM1FB,nom}$	P_6.1.5.42
Undervoltage hysteresis	$V_{VM1,UV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.44
Deglitching time	$t_{VM1,deg}$	8	-	20	µs	–	P_6.1.5.45
Short-to-ground detection time	$t_{VM1,StG}$	2.7	3.0	3.3	ms	–	P_6.1.5.46
External voltage monitor VM2 (VM2FB-AGx)							
Overvoltage threshold	$V_{VM2,OV}$	+6.0	+8.0	+10	%	Referenced to VM2 nominal reference voltage $V_{VM2FB,nom}$	P_6.1.5.48
Overvoltage hysteresis	$V_{VM2,OV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.50
Undervoltage threshold	$V_{VM2,UV}$	-6.0	-8.0	-10	%	Referenced to VM2 nominal reference voltage $V_{VM2FB,nom}$	P_6.1.5.52
Undervoltage hysteresis	$V_{VM2,UV,Hys}$	0.4	–	2.25	%	–	P_6.1.5.54
Deglitching time	$t_{VM2,deg}$	8	-	20	µs	–	P_6.1.5.55
Short-to-ground detection time	$t_{VM2,StG}$	2.7	3.0	3.3	ms	–	P_6.1.5.56

6.2 Thermal protection

The device incorporates multiple independent temperature sense elements to monitor its temperature, specifically of the high-voltage regulator Buck1 and the post-regulator Buck2. Please refer to the respective sections for more information on the individual blocks.

A third temperature sensor is located in the monitoring block of the device. **Table 15** shows the temperature thresholds for the sensor in the monitoring block.

While the temperature is monitored in the individual blocks, the thermal shutdown (TSD) events of these measurements are globally collected. For each individual warning and fault event an appropriate bit in the SPI registers **OTSF0** and **OTSF1** is set.

An overtemperature warning event for any of the three temperature sensors generates an interrupt for the microcontroller.

A thermal shutdown event (TSD) for any of the three sensors triggers a move to the FAULT state. If a thermal shutdown event occurs, then the fault time is extended to approximately one second (see **Table 27**) in order to allow the temperature to drop prior to the restart of the device.

Table 15 Electrical characteristics temperature sensor monitoring block

V_{R1VSx} = 3.7 V to 35 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overtemperature warning threshold	$T_{j,MONOT,WRN}$	130	145	160	°C	1) T_j increasing	P_6.2.0.1
Overtemperature warning threshold	$T_{j,MONOT,WRN}$	120	135	150	°C	1) T_j decreasing	P_6.2.0.2
Overtemperature fault threshold	$T_{j,MONOT,FLT}$	175	190	205	°C	1) T_j increasing	P_6.2.0.3
Overtemperature fault threshold	$T_{j,MONOT,FLT}$	165	180	195	°C	1) T_j decreasing	P_6.2.0.4

1) Not subject to production test, specified by design.

7 Microcontroller interface and supervisory functions

This section describes the connections between the device and the microcontroller.

Figure 8 shows that the microcontroller and the device use several signals for communication and for mutual monitoring of correct operation. An SPI configures the device and monitors status information. A dedicated interrupt signal of the device notifies the microcontroller about any interaction required. To ensure safe operation of the microcontroller a watchdog trigger line (WDI) is available. The device can use a reset-output signal (ROT) to reset the microcontroller if required.

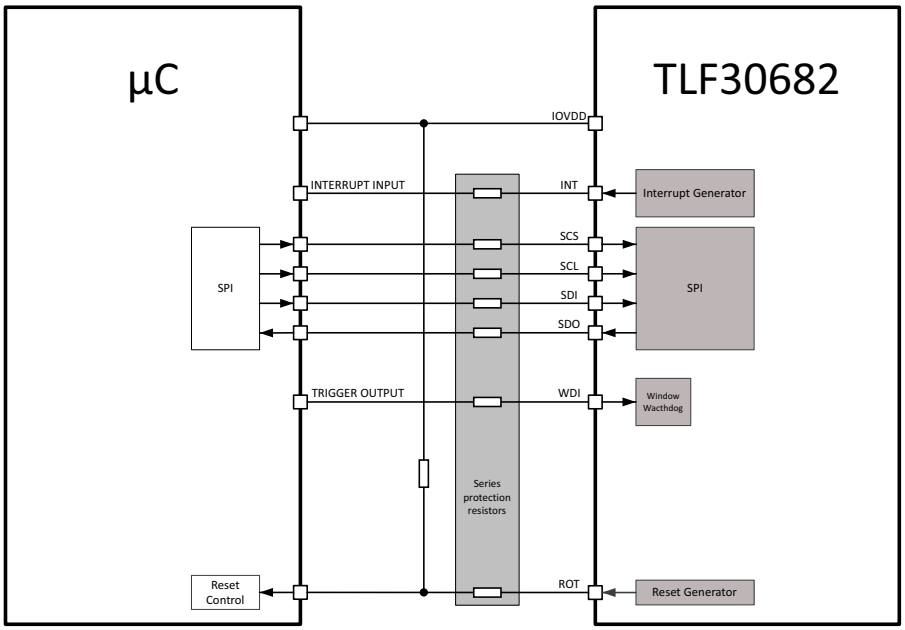


Figure 8 Interface between the TLF30682 and microcontroller

7.1 Microcontroller interface supply – IOVDD pin

The device can handle microcontrollers with different IO supply voltages. This is accommodated by a dedicated supply pin (IOVDD) at which the IO supply voltage is externally supplied to the device. This voltage then drives the logic output pins to the microcontroller. It is also used to determine the input thresholds for the input cells. The affected pins are:

- SCS
- SCL
- SDI
- SDO
- INT
- ROT
- WDI
- SYNCI
- SYNCO

7.1.1 Electrical characteristics

Table 16 Electrical characteristics microcontroller interface supply

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Microcontroller interface							
Supply voltage	V_{IOVDD}	3.0	–	5.5	V	–	P_7.1.1.1
Supply current	I_{IOVDD}	–	2.5	–	mA	V_{IOVDD}= 3.3 V SDO, SDI and SCL switching at 10 MHz SYNCI and SYNCO switching at 2.5 MHz SCS, ROT, INT and WDI are static signals	P_7.1.1.2

7.2 Serial peripheral interface (SPI)

7.2.1 SPI introduction

The serial peripheral interface (SPI) is a synchronous serial data link that operates in full duplex mode. The SDI pin receives data and the SDO pin transmits data.

The device communicates in slave mode where the master, for example the microcontroller, provides a clock on the SCL pin and initiates the data frame. The device is addressed via a dedicated chip select line (SCS pin).

Functional description SPI

The data on pin SDI is captured on the falling edge of the SPI clock signal (pin SCL) and shifted on the rising edge of the SPI clock signal. The data on pin SDO is set on the falling edge of SPI clock signal (pin SCL) and shifted on the rising edge of the SPI clock signal. The SPI master should capture the data on the falling edge of the SPI clock signal.

An SPI command consists of the following (**Figure 9**):

- command bit CMD
- 6 address bits A0-A5
- 8 data bits D0-D7
- parity bit P

The SPI response for read operations consists of the following:

- command bit CMD
- 6 status bits S0-S5
- 8 data bits D0-D7
- parity bit P

For a write operation, the data read on SDI is looped back via SDO.

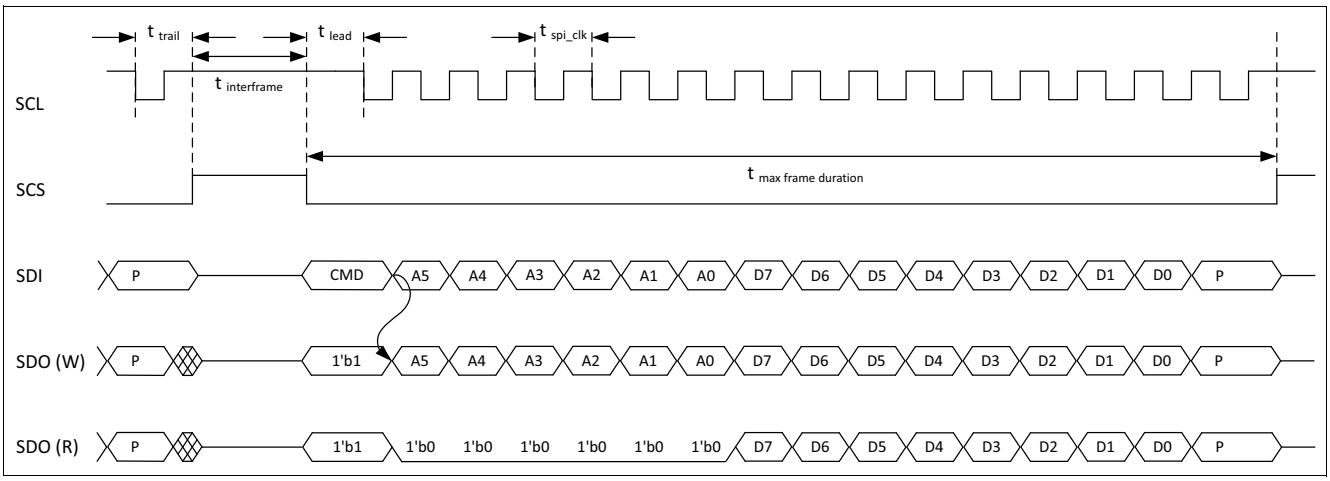


Figure 9 SPI frame format

The command bit in the SPI command is set to 1’b0 for a read and 1’b1 for a write operation. In the reply, the command bit is always set to 1’b1.

The parity bit P is calculated from the 15 data bits of the SPI message consisting of the CMD bit, the 6 address and 8 data bits. The parity bit is set to ‘1’, if the number of ‘1’s in the data bits is odd, that is it is a XOR function of the 15 data bits. The receiver of the SPI message should verify the parity bit prior processing the payload of the message.

The SPI performs several checks on the communication to ensure proper behavior:

- If a parity fault is detected, then the device ignores the data, sets the SPI status bit **SPISF.PAR** and generates an interrupt.
- If a write operation to an invalid address occurs, then the device ignores the data, sets the SPI status **SPISF.ADDR** and generates an interrupt.
- If a read operation from an invalid address occurs, then the device reads all data bits as zero and sets the parity bit to a wrong value to indicate an incorrect message to the SPI master. In addition the device sets the SPI status bit **SPISF.ADDR** and generates an interrupt.
- If a write operation with an incorrect number of SPI clock cycles occurs while SCS is "low", then the device ignores the data, sets the SPI status **SPISF.LEN** and generates an interrupt.
- If a read operation with an incorrect number of SPI clock cycles occurs, then the device sets the SPI status **SPISF.LEN** and generates an interrupt to indicate an invalid data message to the SPI master. The SDO pin provides the data during this operation. At the end of the message it indicates its correctness.
- If the frame duration exceeds the maximum frame time t_{SPI_fl}, then the device terminates communication by disabling the output driver of the SDO pin. In addition the device sets the SPI status bit **SPISF.DUR** and generates an interrupt.

Interrupts on SPI errors are initiated only after SCS is driven "high" or after a frame time-out occurs.

7.2.2 SPI write access to protected registers

Certain registers are protected against accidental write operations.

These so-called protected registers are implemented in pairs where a protected register (for example **PWDCFG0**) is used to store a configuration request, while an associated read-only register (for example **RWDCFG0**) is used to store the currently active configuration.

By default, write access to protected registers is disabled. The status of the protection can be checked using **PROTSTAT**.**LOCK**.

Write access must be enabled using the UNLOCK sequence prior to updating the registers. After completing the register update, the configuration must be activated using the LOCK sequence. This disables the write access to the protected register and copies the data to the read-only registers.

After the LOCK sequence an internal configuration time of maximum of 60 µs has to be considered to ensure that the new configuration is applied in the device.

Read access to protected configuration registers is always possible. Read operations invert the data.

The device does not support updating a single protected register. The microcontroller must ensure that all protected registers are configured properly by writing a new value into particular registers and by verifying the content of unchanged registers.

UNLOCK sequence

An UNLOCK sequence consists of four consecutive key bytes (1: AB_H; 2: EF_H; 3: 56_H; 4: 12_H) written into the **PROTCFG** register. The respective SPI write operations must be atomic, so that they are not interrupted by an SPI write operation to a different register. Read operations to any register are permitted. The progress of the UNLOCK sequence can be monitored in the **PROTCFG** register where the respective key bit is set for each correctly written key byte. If an incorrect UNLOCK sequence occurs due to a wrong key or an SPI write operation to a different address, then the device resets the UNLOCK sequence and clears all key bits. The device sets the **SPISF**.**LOCK** bit and generates an interrupt. The microcontroller must restart the UNLOCK sequence.

LOCK sequence

A LOCK sequence consists of four consecutive key bytes (1: DF_H; 2: 34_H; 3: BE_H; 4: CA_H) written into the **PROTCFG** register. The respective SPI write operations must be atomic, so that they are not interrupted by an SPI write operation to a different register. Read operations to any register are permitted. The progress of the LOCK sequence can be monitored in the **PROTCFG** register where the respective key bit is set for each correctly written key byte. In case of an incorrect LOCK sequence, that is a wrong key or an SPI write operation to a different address, then the device resets the LOCK sequence and clears all key bits. The device sets the **SPISF**.**LOCK** bit and generates an interrupt. The microcontroller must restart the LOCK sequence.

7.2.3 SPI write initiated state transition request and regulator configuration

State machine transitions and configuration of output rails can be performed with direct write access to dedicated registers. A defined protocol protects the registers from unintended changes.

In order to request a state transition and/or a change of the configuration of an output rail the request data must be written to two separate, inverted registers (**DEVCTRL** and **DEVCTRLN**). The write operation must be atomic with no other SPI write operation to a different address interrupting the initial write. The data is applied on the rising edge of the CS at the end of the second command.

If an invalid protocol occurs, the device rejects the request, sets the SPI status flag **SPISF**.**DEVCTRL** and generates an interrupt.

The following items are invalid requests:

- An SPI write operation to another address interrupting the write operation to **DEVCTRL** and **DEVCTRLN**.
- The data in **DEVCTRL** and **DEVCTRLN** is not consistent.

If an invalid state transition request occurs, according to the state machine in **Chapter 8**, the device ignores the transition request without generating an interrupt. The device executes the change in configuration of output rails.

7.2.4 Configuration of Buck2 output voltage via SPI

The output voltage of Buck2 can be configured with direct write access to dedicated registers. A specific protocol is used to avoid unintentional changes to the registers.

In order to request a change of the Buck2 output voltage the configuration data must be written to two separate, inverted registers (**B2VCTRL** and **B2VCTRLN**). The write operation must be atomic with no other SPI write operation to a different address interrupting the initial write. The data is applied on the rising edge of the CS at the end of the second command.

If an invalid protocol occurs, the device rejects the request, sets the SPI status flag **SPISF**.**B2VCTRL** and generates an interrupt.

The following items are invalid requests:

- An SPI write operation to another address interrupting the write operation to **B2VCTRL** and **B2VCTRLN**.
- The data in **B2VCTRL**.**B2VOUTF** and **B2VCTRLN**.**B2VOUTF** is not consistent.

If a Buck2 output voltage configuration request is invalid, the device ignores the request without generating an interrupt.

7.2.5 Electrical characteristics

Table 17 Electrical characteristics SPI

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI chip select – SCS							
Valid input level – "high"	$V_{SCS, high}$	0.7	–	–	V_{IOVDD}	V_{SCS} increasing	P_7.2.5.1
Valid input level – "low"	$V_{SCS, low}$	–	–	0.8	V	V_{SCS} decreasing	P_7.2.5.2
Input hysteresis	$V_{SCS, hys}$	–	0.06	–	V_{IOVDD}		P_7.2.5.3
Pull-up current	I_{SCS}	-180	-55	–	µA	$V_{IOVDD} \leq 5.0$ V	P_7.2.5.4
Input capacitance	C_{SCS}	–	4	15	pF	1)	P_7.2.5.5
SPI clock, pin SCL							
Valid input level – "high"	$V_{SCL, high}$	0.7	–	–	V_{IOVDD}	V_{SCL} increasing	P_7.2.5.6
Valid input level – "low"	$V_{SCL, low}$	–	–	0.8	V	V_{SCL} decreasing	P_7.2.5.7
Input hysteresis	$V_{SCL, hys}$	–	0.06	–	V_{IOVDD}		P_7.2.5.8
Pull-up current	I_{SCL}	-180	-55	–	µA	$V_{IOVDD} \leq 5.0$ V	P_7.2.5.9
Input capacitance	C_{SCL}	–	4	15	pF	1)	P_7.2.5.10
SPI data input, pin SDI							
Valid input level – "high"	$V_{SDI, high}$	0.7	–	–	V_{IOVDD}	V_{SDI} increasing	P_7.2.5.11
Valid input level – "low"	$V_{SDI, low}$	–	–	0.8	V	V_{SDI} decreasing	P_7.2.5.12
Input hysteresis	$V_{SDI, hys}$	–	0.06	–	V_{IOVDD}		P_7.2.5.13
Pull-down current	I_{SDI}	–	135	330	µA	$V_{SDI} = V_{IOVDD}$	P_7.2.5.14
Input capacitance	C_{SDI}	–	4	15	pF	1)	P_7.2.5.15
SPI data output, pin SDO							
Output level – "high"	$V_{SDO, high}$	0.7	–	–	V_{IOVDD}	I_{SDO} = -7 mA	P_7.2.5.16
Output level – "low"	$V_{SDO, low}$	–	–	0.7	V	I_{SDO} = -5.5 mA	P_7.2.5.17
Output rise time	$t_{SDO,rise}$	–	–	25	ns	$C_{SDO,Load}$ = 50 pF	P_7.2.5.18
Output fall time	$t_{SDO,fall}$	–	–	25	ns	$C_{SDO,Load}$ = 50 pF	P_7.2.5.19
Output tristate capacitance	$C_{SDO,tri}$	–	4	15	pF	1)	P_7.2.5.20
Output tristate leakage	$I_{SDO,tri}$	-10	–	10	µA	–	P_7.2.5.21

1) Not subject to production test, specified by design.

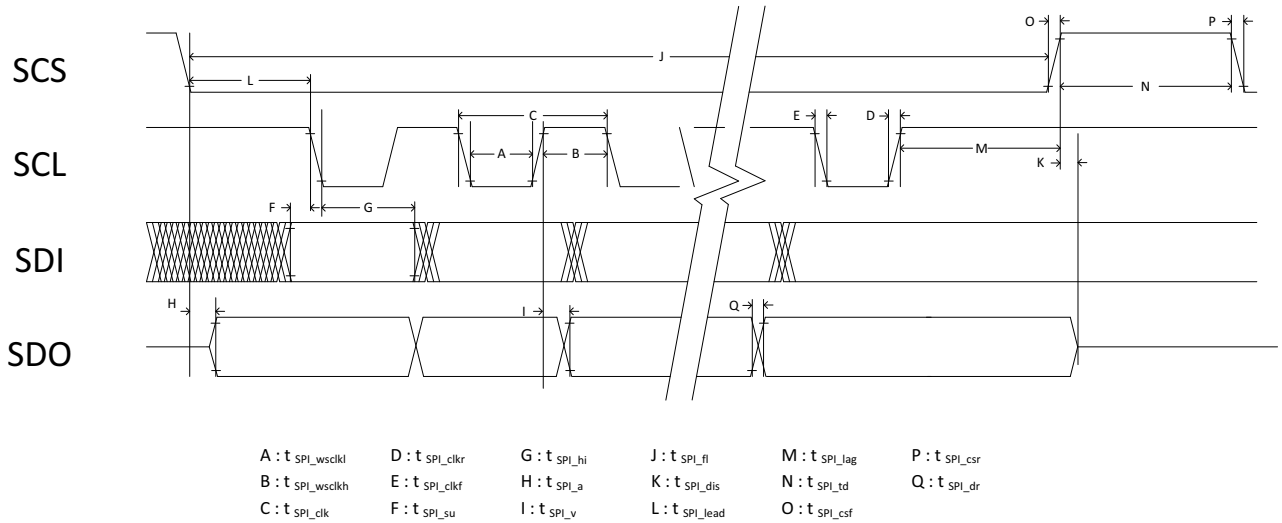


Figure 10 SPI timing

Table 18 Electrical characteristics SPI timing

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CLK_SPI operating frequency	f_{SPI_clk}	–	–	10	MHz	–	P_7.2.5.22
CLK signal duty cycle	D_{SCL}	45	50	55	%	–	P_7.2.5.23
CLK_SPI "high" time	t_{SPI_wsclkh}	45	–	–	ns	–	P_7.2.5.24
CLK_SPI "low" time	t_{SPI_wsclkl}	45	–	–	ns	–	P_7.2.5.25
CLK_SPI fall time	t_{SPI_clkf}	–	–	100	ns	f_{SPI_clk} < 1 MHz	P_7.2.5.26
CLK_SPI fall time	t_{SPI_clkf}	–	–	$0.1/f_{SPI\_clk}$	ns	f_{SPI_clk} ≥ 1 MHz	P_7.2.5.27
CLK_SPI rise time	t_{SPI_clkr}	–	–	100	ns	f_{SPI_clk} < 1 MHz	P_7.2.5.28
CLK_SPI rise time	t_{SPI_clkr}	–	–	$0.1/f_{SPI\_clk}$	ns	f_{SPI_clk} ≥ 1 MHz	P_7.2.5.29
CLK_SPI lead time	t_{SPI_lead}	100	–	–	ns		P_7.2.5.30
CLK_SPI lag time	t_{SPI_lag}	50	–	–	ns		P_7.2.5.31
SPI chip select (SCS) rise time	t_{SPI_csr}	–	–	200	ns	t_{SPI_lead} = 100 ns	P_7.2.5.32
SPI chip select (SCS) rise time	t_{SPI_csr}	–	–	$0.2 \times t_{SPI\_lead}$	ns	t_{SPI_lead} > 100 ns	P_7.2.5.33
SPI chip select (SCS) rise time	t_{SPI_csf}	–	–	200	ns	t_{SPI_lead} = 100 ns	P_7.2.5.34
SPI chip select (SCS) fall time	t_{SPI_csf}	–	–	$0.2 \times t_{SPI\_lead}$	ns	t_{SPI_lead} > 100 ns	P_7.2.5.35
SPI data input (SDI) setup	t_{SPI_su}	10	–	–	ns	–	P_7.2.5.36

Table 18 Electrical characteristics SPI timing (cont'd)

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI data input (SDI) hold time	t_{SPI_hi}	10	–	–	ns	–	P_7.2.5.37
SPI data output (SDO) valid after CLK_SPI	t_{SPI_v}	–	–	36 + (0.1/f_{SPI_clk})	ns	$C_{SDO,load}$ = 50 pF f_{SPI_clk} > =1 MHz	P_7.2.5.38
SPI data output (SDO) valid after CLK_SPI	t_{SPI_v}	–	–	136	ns	$C_{SDO,load}$ = 50 pF f_{SPI_clk} < 1 MHz	P_7.2.5.39
SPI write propagation delay SDI to SDO	t_{SPI_wpd}	–	–	35	ns	–	P_7.2.5.40
SPI data output (SDO) access	t_{SPI_a}	–	–	50	ns	$C_{SDO,load}$ = 50 pF	P_7.2.5.41
SPI data output (SDO) lag	t_{SPI_lag}	50	–	–	ns	–	P_7.2.5.42
SPI data output (SDO) disable time	t_{SPI_dis}	–	–	100	ns	$C_{SDO,load}$ = 50 pF	P_7.2.5.43
Sequential transfer delay	t_{SPI_td}	350	–	–	ns	–	P_7.2.5.44
Frame duration (SCS "low")	t_{SPI_fl}	–	–	1.85	ms	–	P_7.2.5.45

7.3 Reset signal ROT

Reset output pin ROT

The reset output pin ROT is an open drain structure. As soon as a reset condition occurs, the ROT pin is pulled below $V_{ROT,low}$. Once the internal reset signal is released, an internal pull-up current pulls the ROT pin towards the microcontroller supply voltage V_{IOVDD}. An external pull-up resistor may be connected between the ROT and IOVDD pins to speed up the transition. As soon as all events leading to the reset are cleared and the reset delay time expires, the device releases the internal reset signal.

Reset events

Several different internal events can trigger an activation of the reset signal. Please refer to **Table 26** for detailed information on the respective events. Additionally the reset signal is activated when voltage supply rails are out of their total operating band. Information on the respective voltage rails can be found in **Table 25**.

Sometimes the activation of the reset is coupled with a deactivation of the supply signals to generate a hard reset. During a hard reset the ROT pin is forced "low" and the supply rails of the microcontroller are turned off. During a soft reset the ROT pin is forced "low", while the supply voltages remain in operation.

7.3.1 Electrical characteristics – ROT pin

Table 19 Electrical characteristics ROT pin

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reset output pin ROT							
Pull-up current	$I_{ROT,high}$	-180	-120	–	µA	$V_{ROT} \leq 2.0V$	P_7.3.1.1
Output level – "low"	$V_{ROT,low}$	–	–	0.4	V	V_{IOVDD} = 5.0 V I_{ROT} = 3.5 mA	P_7.3.1.2
Output level – "low"	$V_{ROT,low}$	–	–	0.4	V	V_{IOVDD} = 3.3 V I_{ROT} = 3.5 mA	P_7.3.1.3
Output fall time	$t_{ROT,fall}$	–	–	25	ns	$C_{ROT,load}$ = 50 pF	P_7.3.1.5
Reset timing							
Reset cycle time	t_{cycle}	–	10	–	µs	–	P_7.3.1.6
Reset delay time – adjustment range	t_{RD}	20	–	2000	t_{cycle}	–	P_7.3.1.7
Reset delay time – default value		–	100	–	t_{cycle}	1)	P_7.3.1.8

1) The default configuration for the reset contributor might not generate a reset at the first start up of the device.

7.4 Interrupt signal INT

An interrupt is generated to inform the connected microcontroller that a non-severe event has occurred. This allows the microcontroller to perform proper action based on the source of the interrupt. A single low-active interrupt line is used.

If one or more new flags in the interrupt flag registers (**Chapter 9.1.5**) are set, then the device indicates an interrupt to the microcontroller.

Interrupt pin INT

The interrupt pin INT is a push-pull output using the microcontroller supply voltage V_{IOVDD}.

The device indicates an interrupt by pulling the INT pin "low". If all register flags are cleared via SPI, then the device drives the interrupt line "high".

The interrupt signal is subject to a minimum "low" time, t_{INT}, which means that the interrupt pin will remain "low" for this time even if the interrupt is serviced faster. The implemented interrupt minimum "high" timing keeps the interrupt "high" for a minimum time of $t_{INT,high}$. If a new interrupt is triggered during this time period, the interrupt signal remains "high" and indicates the interrupt after the minimum "high" time, $t_{INT,high}$, elapses.

The interrupt time-out, t_{INTTO}, is implemented after which the device drives the interrupt signal "high", regardless of whether the interrupt is serviced or not. In this case the device generates a missed interrupt event and sets **GSF.INTMISS**. This does not generate another interrupt. The microcontroller must read this flag autonomously.

7.4.1 Electrical characteristics – INT pin

Table 20 Electrical characteristics INT pin

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Interrupt signal INT							
Output level – "high"	$V_{INT,high}$	0.7	–	–	V_{IOVDD}	I_{INT} = -7 mA	P_7.4.1.1
Output level – "low"	$V_{INT,low}$	–	–	0.7	V	I_{INT} = -5.5 mA	P_7.4.1.2
Output rise time	$t_{INT,rise}$	–	–	25	ns	$C_{INT,load}$ = 50 pF	P_7.4.1.3
Output fall time	$t_{INT,fall}$	–	–	25	ns	$C_{INT,load}$ = 50 pF	P_7.4.1.4
Minimum interrupt "low" time	$t_{INT,low}$	90	100	110	µs	–	P_7.4.1.5
Interrupt "low" time-out	t_{INTTO}	270	300	330	µs	ROT signal for the microcontroller must be released: ROT = “high”	P_7.4.1.6
Minimum interrupt "high" time	$t_{INT,high}$	270	300	330	µs	–	P_7.4.1.7

7.5 Window watchdog

Principle of operation

The integrated window watchdog (WWD) can monitor the microcontroller. The monitored microcontroller must provide periodical triggering during the "open window". A trigger signal can consist of a falling edge on the WDI pin or an SPI write operation to the register **WWDSCMD**, depending on the configuration. Failure to provide correct trigger signals will lead to an increase of the window watchdog failure counter, which is used to monitor the fault events. If the window watchdog failure counter reaches a configurable threshold, it then triggers an appropriate response.

Normal operation

Within the "open window" a trigger signal is expected. If the device receives a trigger signal during the "open window", the window watchdog then terminates the "open window" cycle and starts the "closed window" cycle with a duration of $t_{WD,CW}$, followed by another "open window" cycle. If the window watchdog error counter is greater than zero, any valid window watchdog trigger signal decrements the window watchdog error counter by 1. This does not generate an interrupt.

In normal operation no trigger signal is allowed during the "closed window". If the device receives a trigger signal within the "closed window", the window watchdog recognizes an invalid WWD trigger signal. The window watchdog terminates the "closed window" cycle with an invalid trigger signal and starts another "open window" cycle. Any invalid WWD trigger signal increments the window watchdog error counter by 2. This then generates an interrupt.

If the device does not receive any valid trigger signal during the "open window" cycle, then the window watchdog recognizes invalid WWD triggering, increments the window watchdog error counter by 2 and starts another "open window". This also generates an interrupt.

Configuration

The following parameters of the window watchdog can be configured via SPI in ACTIVE:

- The trigger signal can be configured as either pin triggering (pin WDI) or triggering via SPI command (register **WWDSCMD**). The default configuration is the triggering via SPI.
- The duration of the "open window" and "closed window" cycles can be modified according to the application needs (combination of cycle time **WDCYC** and number of cycles for open window **OW** and closed window **CW**).
- The threshold for the window watchdog error counter overflow can be configured.

Initialization

As soon as the device releases the microcontroller reset output (ROT) it enables the window watchdog in ACTIVE state. After activation the watchdog opens a so-called "long open window" (LOW) cycle of duration of $t_{WD,LOW}$. During the "long open window" cycle the window watchdog expects a valid trigger signal (or a change of configuration).

The default configuration expects watchdog triggering via SPI. Therefore, glitches at the microcontroller output connected to the WDI have no effect during startup and initialization.

The microcontroller can change the configuration of the window watchdog during the "long open window" cycle. After a reconfiguration the window watchdog restarts with the new configuration. The window watchdog starts a regular "open window" cycle accordingly, expecting a valid trigger signal by the selected triggering input.

Watchdog trigger signals

Two different trigger sources can be selected as watchdog trigger signal. This can be either an SPI write operation to **WWDSCMD** or a valid trigger event on the watchdog input pin WDI.

The WDI pin has an integrated pull-down current source. A falling edge (transition from $V_{WDI,high}$ to $V_{WDI,low}$) on the pin is considered a trigger signal for the watchdog. The rising edge can occur at any time and is not considered a trigger signal. For calculation of the external provided WDI the watchdog sampling time (t_{WDI_filter}) has to be considered. For SPI watchdog trigger the positive edge of signal chip select (SCS) must be considered.

Watchdog error counter and event generation

The window watchdog includes a watchdog error counter for invalid watchdog trigger events. The device compares the watchdog error counter to the window watchdog error threshold continuously. If the counter exceeds the threshold, it generates a window watchdog error event. The window watchdog error threshold is configurable via SPI.

7.5.1 Electrical characteristics

Table 21 Electrical characteristics window watchdog function

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Watchdog cycle time, configuration option 0	t_{WDCYC}	9.5	10	10.5	µs	–	P_7.5.1.1
Watchdog cycle time, configuration option 1	t_{WDCYC}	95	100	105	µs	–	P_7.5.1.2
Long open window time	t_{LOW}	570	600	630	ms	–	P_7.5.1.3
Watchdog input, pin WDI							
Watchdog sampling time	t_{WDI_filter}	380	400	420	µs	–	P_7.5.1.4
Valid input level – "high"	$V_{WDI, high}$	0.7	–	–	V_{IOVDD}	V_{WDI} increasing	P_7.5.1.5
Valid input level – "low"	$V_{WDI, low}$	–	–	0.8	V	V_{WDI} decreasing	P_7.5.1.6
Input hysteresis	$V_{WDI, hyst}$	–	0.06	–	V_{IOVDD}	–	P_7.5.1.7
Pull-down current	I_{WDI}	–	135	330	µA	–	P_7.5.1.8
Input capacitance	C_{WDI}	–	4	15	pF	1)	P_7.5.1.9

1) Not subject to production test, specified by design.

7.6 Microcontroller programming support

The device includes a feature to support programming of microcontroller's firmware during production or in the field by preventing periodic reset triggering during the initialization period.

Programming mode can be enabled by pulling the MPS pin "high". In programming mode the reset generation to the microcontroller is modified, so that fault events of microcontroller monitoring features do not generate a microcontroller reset. All other monitoring features that generate a microcontroller reset are still active (see **Table 25**). The interrupt generation and the state transitions are still active. However, the initialization timer is disabled, so that the device can remain in ACTIVE state.

Operation of the internal state machine and the programming mode are independent, which allows the transition to any state while the microcontroller programming mode is active. However, the microcontroller monitoring is still active and will move the device into ACTIVE state. Therefore, leave the device in ACTIVE state during a programming operation.

Voltage monitoring is active and generates the respective fault events. This may generate interrupts or move the device into FAULT state depending on the nature of the event.

Table 22 Electrical characteristics microcontroller programming mode

T_j = -40°C to 150°C, V_{R1VSx} = 3.7 V to 35 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

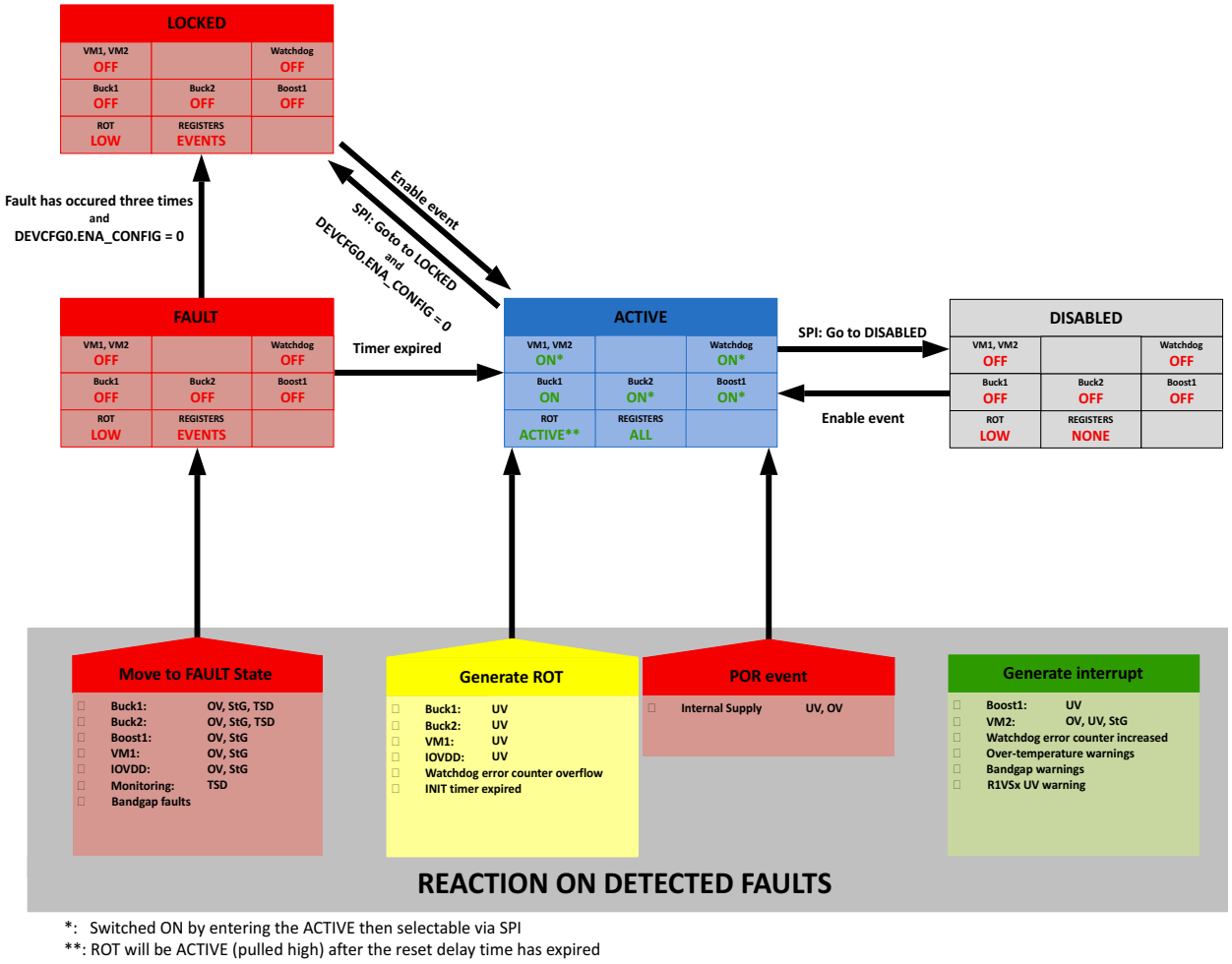
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
MPS pin							
Valid input level – "high"	$V_{MPS, high}$	2.4	–	–	V	V_{MPS} increasing	P_7.8.0.1
Valid input level – "low"	$V_{MPS, low}$	–	–	0.8	V	V_{MPS} decreasing	P_7.8.0.2
Input hysteresis	$V_{MPS, hys}$	–	350	–	mV	1)	P_7.8.0.3
Pull-down current	I_{MPS}	–	140	330	µA	V_{MPS}=5.0V	P_7.8.0.4
Input capacitance	C_{MPS}	–	4	15	pF	1)	P_7.8.0.5

1) Not subject to production test, specified by design.

8 State machine

8.1 Introduction

The integrated state machine controls operation in different situations. **Figure 11** shows the complete state-diagram. **Table 23** and **Table 24** describe each state and the transitions.



*: Switched ON by entering the ACTIVE then selectable via SPI
**: ROT will be ACTIVE (pulled high) after the reset delay time has expired

Figure 11 State machine

8.2 Operation states

ACTIVE

The ACTIVE state is the first state that the device enters after power-on. The device powers up all voltage rails and expects configuration from the microcontroller within the initialization time window according to the INIT timer.

On deactivation of the microcontroller reset the INIT timer starts. If the following conditions are fulfilled, then the INIT timer stops:

- The device receives valid SPI communication from the microcontroller.
- The window watchdog is serviced once according to its configuration.

If the INIT timer is not stopped and expires, then an initialization error is detected. The first initialization error triggers a soft reset, which activates the reset signal ROT, but no state transition. The second initialization error triggers a hard reset, which activates the reset signal ROT and shuts down the supply rails, thus the device enters FAULT state and the system restarts.

The microcontroller can request a transition from ACTIVE state to either DISABLED or LOCKED state with an SPI command. On an SPI request to change the state to DISABLED or LOCKED the TLF30682QVS01 enters the FAULT state for 20 ms before it enters the requested state. This is done to ensure a proper discharge of the output voltages of all switching regulators before the device can be re-enabled.

DISABLED

During DISABLED state the device is powered off and it only monitors the enable signal (ENA) for a valid enable condition. Once a valid enable event is detected, the device enters ACTIVE state and expects configuration from the microcontroller. In DISABLED state the register content of all registers is reset. The device needs to be configured again during the ACTIVE state.

FAULT

On detection of a severe fault the device enters FAULT state. In FAULT state all regulators are switched off and the microcontroller reset (ROT) is asserted. The device remains in FAULT state for the specified fault time prior to a transition into ACTIVE state. In FAULT state the event registers are retained to store the reason for entering the FAULT state. All other device registers are reset.

A soft reset condition on the first detection of a fault condition triggers the reset signal ROT, but no state transition. If the device detects the same soft reset fault condition again, then it increases the severity of the fault to a severe fault. In this case the device enters the FAULT state. This applies for all soft reset faults except the Window Watchdog error counter overflow.

LOCKED

The device enters LOCKED state after three severe faults, brought on by expiration of the initialization counter or by request of the microcontroller. The power consumption in LOCKED state is reduced. The device remains in LOCKED state until it detects the next valid enable event. In LOCKED state only a limited set of the event registers are retained to store the reason for entering the LOCKED state. All other device registers are reset.

Table 23 Operational states functional overview.

	ACTIVE		FAULT		LOCKED		DISABLED	
Block or function								
Buck1	ON	R	OFF	R	OFF	R	OFF	R
Buck2	ON	RW	OFF	R	OFF	R	OFF	R
Boost1	ON	RW	OFF	R	OFF	R	OFF	R
VM1	ON	RW	OFF	R	OFF	R	OFF	R
VM2	ON	RW	OFF	R	OFF	R	OFF	R
Window watchdog	ON	RW	OFF	R	OFF	R	OFF	R
Microcontroller reset – ROT	ACTIVE	R	"low"	R	"low"	R	"low"	R
Persistent registers	All registers	-	Event registers	-	Event registers	-	-	-

- ON: Function is automatically activated when entering the state . Function may be configured via SPI within the current state.
- SEL: Function is operating as configured via SPI (during the mode transition or within the current operation mode).
- OFF: Function is automatically deactivated when entering the operation mode.
- R: The state of the feature cannot be changed in the current operation mode.
- RW: The state of the feature can be changed in the current operation mode.
- "high": The signal is "high" in this operation mode.
- "low": The signal is "low" in this operation mode.
- ACTIVE: The reset signal may generate a reset event (edge) in this operation mode.

8.3 State transitions and trigger signals

This section describes the state transitions of the integrated state machine.

Table 24 shows the static state transitions with the respective source and destination states, the condition required to trigger the state transition and a transition specific action executed during the transition.

Each row refers to one state transition. With multiple conditions in the same row all of the conditions must be met.

Table 24 State Transitions

Source	Destination	Condition	Action
Unpowered	ACTIVE	Device supplied First POR event	
ACTIVE	DISABLED	SPI command	
ACTIVE	LOCKED	SPI command	
ACTIVE	FAULT	Hard reset fault detected	
DISABLED	ACTIVE	Enable event	Generate MCU reset
FAULT	ACTIVE	FAULT timer expired	Generate MCU reset
FAULT	LOCKED	Hard reset fault has occurred three times.[1)]	
LOCKED	ACTIVE	Enable event	Generate MCU reset

1) ENA pin must be configured as edge-triggered or the ENA pin must be low to trigger the transition from FAULT to LOCKED state

Table 25 and **Table 26** show the mapping between the fault events and the associated actions.

Table 25 Event response mapping – voltage rails

Event	Move to FAULT	Move to ACTIVE Generate RESET	Move to DISABLED	No transition Generate interrupt
Buck1: OV	X	–	–	–
Buck1: UV	–	X	–	–
Buck1: StG	X	–	–	–
Buck2: OV	X	–	–	–
Buck2: UV	–	X	–	–
Buck2: StG	X	–	–	–
Boost1: OV	X	–	–	–
Boost1: UV	–	–	–	X
Boost1: StG	X	–	–	–
VM1: OV	X	–	–	–
VM1: UV	–	X	–	–
VM1: StG	X	–	–	–
VM2: OV	–	–	–	X
VM2: UV	–	–	–	X
VM2: StG	–	–	–	X

Table 26 Event response mapping – other events

Event	Move to FAULT	Move to ACTIVE Generate RESET	Move to DISABLED	No transition Generate interrupt
WWD: counter increase	–	–	–	X
WWD: counter overflow	–	X	–	–
INIT timer expired – first time	–	X	–	–
INIT timer expired – second time	X	–	–	–
Internal protection: band gap warning	–	–	–	X
Internal protection: band gap fault	X	–	–	–
IOVDD: OV	X	–	–	–
IOVDD: UV	–	X	–	–
IOVDD: StG	X	–	–	–
Internal protection: internal supplies (UV,OV)	–	X[1)]	–	–
Buck1: OT warning	–	–	–	X
Buck1: OT fault	X	–	–	–
Buck2: OT warning	–	–	–	X
Buck2: OT fault	X	–	–	–
Monitoring: OT warning	–	–	–	X
Monitoring: OT fault	X	–	–	–

1) If the TLF30682QVS01an detects an UV or OV fault condition on the internal supplies, then it turns of completely. The TLF30682QVS01 enters the ACTIVE state when the UV or OV condition is no longer present.

8.4 Electrical characteristics

Table 27 Electrical characteristics state machine

T_j = -40°C to 150°C; V_{R1VSx} = 3.7 V to 35 V; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Initialization time-out (INIT timer)	t_{INIT}	550	600	650	ms	–	
Fault time	t_{Fault}	–	20	–	ms	–	
Fault time TSD	$t_{Fault,TSD}$	–	1000	–	ms	–	
State transition time	t_{trans}	–	–	100	µs	–	

9 SPI registers

Table 28 Abbreviations

R0	Register is reset on a POR event and on a transition into DISABLE state.
R1	Register is reset with reset class R0 and additionally on a transition into LOCKED state.
R2	Register is reset with reset class R1 and additionally on a microcontroller reset.
r	Bit is readable (read-only).
rw	Bit is readable and writable (read-write).
rw1p	Bit is protected. Read data is inverted. Write via LOCK/UNLOCK mechanism only.
rw1c	Bit is readable and can be cleared by a write operation with 1. Bit is updated based on hardware inputs (flags).
rwhc	Bit is readable and writable. After a write operation with 1 an operation is triggered which upon its completion sets the bit to 0.
rwhu	Bit is readable and writable. Bit is updated based on hardware inputs (flags).

Table 29 Register overview

Register ID	Description	Address	Reset Value	Reset Class	Page
DEVCFG0	Device configuration 0	00H	F3H	R0	Page 65
CLKCFG0	Clock configuration 0	01H	00H	R2	Page 66
CLKCFG1	Clock configuration 1	02H	04H	R2	Page 67
PROTCFG	Configuration protection	03H	00H	R2	Page 74
PWDCFG0	Protected watchdog configuration 0	06H	9BH	R2	Page 67
RWDCFG0	Read-only watchdog configuration 0	07H	9BH	R2	Page 69
PWDCFG1	Protected watchdog configuration 1	08H	46H	R2	Page 68
RWDCFG1	Read-only watchdog configuration 1	09H	46H	R2	Page 69
PWDCFG2	Protected Watchdog Configuration 2	0AH	78H	R2	Page 68
RWDCFG2	Read-only watchdog configuration 2	0BH	78H	R2	Page 70
B2VCTRL	Buck2 output voltage control	10H	02H	R1	Page 73
B2VCTRLN	Buck2 output voltage control inverted	11H	0DH	R1	Page 73
GSF	Global status flags	1AH	00H	R0	Page 76
SYSSF0	System status flags – faults	1BH	00H	R0	Page 77
SYSSF1	System status flags – interrupts	1CH	00H	R1	Page 78
MCUSF0	Microcontroller status flags 0 – faults	1DH	00H	R0	Page 79
MCUSF1	Microcontroller status flags 1 – warnings	1EH	00H	R1	Page 79
SPISF	SPI status flags	1FH	00H	R1	Page 80
MONSF0	Voltage monitoring status flags 0 – short to ground	20H	00H	R0	Page 81
MONSF1	Voltage monitoring status flags 1 – overvoltage	21H	00H	R0	Page 82

Table 29 Register overview (cont'd)

Register ID	Description	Address	Reset Value	Reset Class	Page
MONSF2	Voltage monitoring status flags 2 – undervoltage	22H	00H	R0	Page 83
OTSF0	Overtemperature events 0 – faults	23H	00H	R0	Page 84
OTSF1	Overtemperature flags 1 – warnings	24H	00H	R1	Page 84
OCSF1	Overcurrent flags – warnings	25H	00H	R1	Page 85
OTSTAT0	Overtemperature status 0 – warnings	26H	00H	R1	Page 86
VMONSTAT0	Voltage monitoring	27H	00H	R1	Page 86
DEVSTAT	Device state information	28H	00H	R1	Page 87
PROTSTAT	Protection status information	29H	01H	R2	Page 88
WWDSTAT	Window watchdog status information	2AH	00H	R2	Page 89
WWDSCMD	Window watchdog service command	33H	00H	R2	Page 74
DEVCTRL	Device state control	34H	00H	R1	Page 71
DEVCTRLN	Device state control inverted	35H	00H	R1	Page 72
MPSSTAT0	Microcontroller programming support status information	37H	03H	R1	Page 89
B2VSTAT	Buck2 output voltage status	39H	02H	R1	Page 90
HWDECT0	Hardware option information	3BH	D3H	R1	Page 91
DEVID	Device identification	3CH	10H	R1	Page 92

9.1 SPI register definition

9.1.1 Device configuration registers (device start-up default configuration)

DEVCFG0
Device configuration 0 **(00_H)** **Reset Value:$F3_H$**

7	6	5	4	3	2	1	0
VM2ENAS	VM1ENAS	BOOST1ENAS	BUCK2ENAS	ENA_CONFIG	RESDEL		
r	r	r	r	rw	rw		

Field	Bits	Type	Description
VM2ENAS	7	r	**External voltage monitoring 2 enable at start up** 0_H disabled 1_H enabled Reset: 1_H
VM1ENAS	6	r	**External voltage monitoring 1 enable at start up** 0_H disabled 1_H enabled Reset: 1_H
BOOST1ENAS	5	r	**Boost1 enable at start up** 0_H disabled 1_H enabled Reset: 1_H
BUCK2ENAS	4	r	**Buck2 enable at start up** 0_H disabled 1_H enabled Reset: 1_H
ENA_CONFIG	3	rw	**ENA pin configuration** 0_H edge triggered 1_H level sensitive Reset: 0_H
RESDEL	2:0	rw	**Reset release delay time** 00_H 200 µs 01_H 400 µs 02_H 800 µs 03_H 1 ms 04_H 2 ms 05_H 4 ms 06_H 10 ms 07_H 20 ms Reset: 3_H

SPI registers

CLKCFG0

Clock configuration 0 **(01_H)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
nu	**PHBUCK2**	**PHBUCK1**	**PHSO**	**nu**	**SSEN**	**SIEN**	**SOEN**
r	rw	rw	rw	r	rw	rwhc	rw

Field	Bits	Type	Description
nu	7	r	**Not used**
PHBUCK2	6	rw	**Buck2 phase alignment** 0_H 0° phase shift 1_H 180° phase shift Reset: 0_H
PHBUCK1	5	rw	**Buck1 phase alignment** 0_H 0° phase shift 1_H 180° phase shift Reset: 0_H
PHSO	4	rw	**External clock synchronization phase alignment** 0_H 0° phase shift 1_H 180° phase shift Reset: 0_H
nu	3	r	**Not used**
SSEN	2	rw	**Spread spectrum modulation enable** 0_H disabled 1_H enabled Reset: 0_H
SIEN	1	rwhc	**External clock synchronization input enable** 0_H disabled 1_H enabled Reset: 0_H
SOEN	0	rw	**External clock synchronization output enable** 0_H disabled 1_H enabled Reset: 0_H

CLKCFG1
Clock configuration 1 **(02_H)** **Reset Value:04_H**

7	6	5	4	3	2	1	0
nu					FREQSEL		
r					rw		

Field	Bits	Type	Description
nu	7:3	r	**Not used**
FREQSEL	2:0	rw	**Main switching frequency** 0_H 1.8 MHz 1_H 1.9 MHz 2_H 2.0 MHz 3_H 2.1 MHz 4_H 2.2 MHz 5_H 2.3 MHz 6_H 2.4 MHz 7_H 2.5 MHz Reset: 4_H

PWDCFG0
Protected watchdog configuration 0 **(06_H)** **Reset Value:$9B_H$**

7	6	5	4	3	2	1	0
WWDETHR				WWDEN	nu	WWDTSEL	WDCYC
rwp				rwp	r	rwp	rwp

Field	Bits	Type	Description
WWDETHR	7:4	rwp	**Window watchdog error threshold** 0_H 0 1_H 1 ... F_H 15 Reset: 9_H
WWDEN	3	rwp	**Window watchdog enable** 0_B disabled 1_B enabled Reset: 1_H
nu	2	r	**Not used**
WWDTSEL	1	rwp	**Window watchdog trigger selection** 0_B external WDI input used as WWD trigger 1_B WWD is triggered by SPI write to WWDSCMD register Reset: 1_H

SPI registers

Field	Bits	Type	Description
WDCYC	0	rwp	**Watchdog cycle time** 0_B 10 µs tick period 1_B 100 µs tick period Reset: 1_H

PWDCFG1
Protected watchdog configuration 1 **(08_H)** **Reset Value: 46_H**

7	6	5	4	3	2	1	0
nu				**CW**			
r				rwp			

Field	Bits	Type	Description
nu	7	r	**Not used**
CW	6:0	rwp	**Window watchdog closed window size** 00_H 0 watchdog cycles 01_H 50 watchdog cycles 02_H 100 watchdog cycles ... $7F_H$ 6350 watchdog cycles Reset: 46_H

PWDCFG2
Protected Watchdog Configuration 2 **($0A_H$)** **Reset Value: 78_H**

7	6	5	4	3	2	1	0
nu				**OW**			
r				rwp			

Field	Bits	Type	Description
nu	7	r	**Not used**
OW	6:0	rwp	**Window watchdog open window size** 00_H 50 watchdog cycles 01_H 50 watchdog cycles 02_H 100 watchdog cycles ... $7F_H$ 6350 watchdog cycles Reset: 78_H

9.1.2 Read-only registers for protected configuration registers

RWDCFG0

Read-only watchdog configuration 0 **(07_H)** **Reset Value:$9B_H$**

7	6	5	4	3	2	1	0
WWDETHR				WWDEN	nu	WWDTSEL	WDCYC
r				r	r	r	r

Field	Bits	Type	Description
WWDETHR	7:4	r	**Window watchdog error threshold ACTIVE** 0_H 0 1_H 1 ... F_H 15 Reset: 9_H
WWDEN	3	r	**Window watchdog enable STATUS** 0_B disabled 1_B enabled Reset: 1_H
nu	2	r	**Not used**
WWDTSEL	1	r	**Window watchdog trigger selection ACTIVE** 0_B external WDI input used as WWD trigger 1_B WWD is triggered by SPI write to WWDSCMD register Reset: 1_H
WDCYC	0	r	**Watchdog cycle time ACTIVE** 0_B 10 µs tick period 1_B 100 µs tick period Reset: 1_H

RWDCFG1

Read-only watchdog configuration 1 **(09_H)** **Reset Value:46_H**

7	6	5	4	3	2	1	0
nu	CW						
r	r						

Field	Bits	Type	Description
nu	7	r	**Not used**

SPI registers

Field	Bits	Type	Description
CW	6:0	r	**Window watchdog closed window size ACTIVE** 00_H 0 watchdog cycles 01_H 50 watchdog cycles 02_H 100 watchdog cycles ... $7F_H$ 6350 watchdog cycles Reset: 46_H

RWDCFG2

Read-only watchdog configuration 2 **($0B_H$)** **Reset Value: 78_H**

7	6	5	4	3	2	1	0
nu	**OW**						
r	r						

Field	Bits	Type	Description
nu	7	r	**Not used**
OW	6:0	r	**Window watchdog open window size ACTIVE** 00_H 50 watchdog cycles 01_H 50 watchdog cycles 02_H 100 watchdog cycles ... $7F_H$ 6350 watchdog cycles Reset: 78_H

9.1.3 Special device configuration registers

The registers in this section are specially protected by a defined access procedure. This procedure is based on the access to two individual registers writing inverted information. For detailed information please refer to **Chapter 7.2.3**.

DEVCTRL
Device state control **(34_H)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
VM2EN	**VM1EN**	**BOOST1EN**	**BUCK2EN**	**nu**	**STATEREQ**		
rw	rw	rw	rw	r	rw		

Field	Bits	Type	Description
VM2EN	7	rw	**External voltage monitoring 2 enable request** 0_H disable 1_H enable Reset: 0_H
VM1EN	6	rw	**External voltage monitoring 1 enable request** 0_H disable 1_H enable Reset: 0_H
BOOST1EN	5	rw	**Boost1 enable request** 0_H disable 1_H enable Reset: 0_H
BUCK2EN	4	rw	**Buck2 enable request** 0_H disable 1_H enable Reset: 0_H
nu	3	r	**Not used**
STATEREQ	2:0	rw	**Device state request** 00_H Reserved 01_H ACTIVE state 02_H Reserved 03_H DISABLED state 04_H Reserved 05_H Reserved 06_H Reserved 07_H LOCKED state Reset: 0_H

DEVCTRLN

Device state control inverted **(35_H)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
VM2EN	**VM1EN**	**BOOST1EN**	**BUCK2EN**	**nu**	**STATEREQ**		
rw	rw	rw	rw	r	rw		

Field	Bits	Type	Description
VM2EN	7	rw	**External voltage monitoring 2 enable request** 0_H enable 1_H disable Reset: 0_H
VM1EN	6	rw	**External voltage monitoring 1 enable request** 0_H enable 1_H disable Reset: 0_H
BOOST1EN	5	rw	**Boost1 enable request** 0_H enable 1_H disable Reset: 0_H
BUCK2EN	4	rw	**Buck2 enable request** 0_H enable 1_H disable Reset: 0_H
nu	3	r	**Not used**
STATEREQ	2:0	rw	**Device state request** 07_H Reserved 06_H ACTIVE state 05_H Reserved 04_H DISABLED state 03_H Reserved 02_H Reserved 01_H Reserved 00_H LOCKED state Reset: 0_H

B2VCTRL

Buck2 output voltage control **(10_H)** **Reset Value:02_H**

7	6	5	4	3	2	1	0
nu				**B2VOUTF**			
r				rwhu			

Field	Bits	Type	Description
nu	7:4	r	**Not used**
B2VOUTF	3:0	rwhu	**Buck2 output voltage setting fine resolution** 0_H 1.30 V 1_H 1.20 V 2_H 1.25 V 3_H 1.15 V 4_H 1.10 V 5_H 1.00 V 6_H 1.05 V 7_H 0.95 V 8_H 0.90 V Reset: 02_H

B2VCTRLN

Buck2 output voltage control inverted **(11_H)** **Reset Value:$0D_H$**

7	6	5	4	3	2	1	0
nu				**B2VOUTF**			
r				rwhu			

Field	Bits	Type	Description
nu	7:4	r	**Not used**
B2VOUTF	3:0	rwhu	**Buck2 output voltage setting fine resolution** F_H 1.30 V E_H 1.20 V D_H 1.25 V C_H 1.15 V B_H 1.10 V A_H 1.00 V 9_H 1.05 V 8_H 0.95 V 7_H 0.90 V Reset: $0D_H$

9.1.4 General registers

PROTCFG
Configuration protection **(03_H)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
KEY							
rw							

Field	Bits	Type	Description
KEY	7:0	rw	**Protection key** Reset: 00_H

WWDSCMD
Window watchdog service command **(33_H)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
TRIG_STATUS	nu						TRIG
r	r						rw

Field	Bits	Type	Description
TRIG_STATUS	7	r	**Window watchdog last trigger received via SPI** Reset: 00_H
nu	6:1	r	**Not used**
TRIG	0	rw	**Window watchdog trigger command** Reset: 00_H

9.1.5 Event status registers

The event status registers of the device are organized hierarchically. The global status register is used to collect information of the status flags set in other registers to enable the user to speed up the event source determination.

A bit in the global status register is automatically set, when a bit in the respective status register is set (event based, not level based).

If a bit in the global status register is set, the user should read out the corresponding status register for the detailed information on the event source.

The bits in the global status flag register can be cleared without effect on the other status registers. Clearing a bit in any of the other status registers does not reset the corresponding bit in the global status register.

GSF
Global status flags **($1A_H$)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
INTMISS	**nu**	**R1VSxUV**	**OT**	**MON**	**SPI**	**MCU**	**SYS**
r	r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
INTMISS	7	r	**Interrupt time out event** 0_H no event 1_H event occurred, cleared by hardware when all other flags in IF are cleared. Reset: 0_H
nu	6	r	**Not used**
R1VSxUV	5	rw1c	**Battery voltage undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
OT	4	rw1c	**Overtemperature or overcurrent monitoring event flag: OTSF0,OTSF1, OCSF1** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
MON	3	rw1c	**Voltage monitoring event flag: MONSF0, MONSF1, MONSF2** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
SPI	2	rw1c	**SPI event flag: SPISF** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
MCU	1	rw1c	**MCU event flag: MCUSF0,MCUSF1** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
SYS	0	rw1c	**System event flag: SYSSF0,SYSSF1** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

SYSSF0

System status flags – faults **($1B_H$)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
BGFLT2	**BGFLT1**	**IOVDDOV**	**IOVDDUV**	**nu**			**FUSEERR**
rw1c	rw1c	rw1c	rw1c		r		rw1c

Field	Bits	Type	Description
BGFLT2	7	rw1c	**Bandgap fault event 2** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BGFLT1	6	rw1c	**Bandgap fault event 1** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
IOVDDOV	5	rw1c	**IOVDD overvoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
IOVDDUV	4	rw1c	**IOVDD undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	3:1	r	**Not used**
FUSEERR	0	rw1c	**Double bit error in fuse memory** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

SYSSF1
System status flags – interrupts **($1C_H$)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
BGWARN2	**BGWARN1**	**ENA_PWRUP**	**nu**	**SYNC**	**ENA**	**CFG2**	**CFG**
rw1c	rw1c	rw1c	r	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
BGWARN2	7	rw1c	**Bandgap warning event 2** (VBG1+4%>VBG2) 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BGWARN1	6	rw1c	**Bandgap warning event 1** (VBG1-4%<VBG2) 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
ENA_PWRUP	5	rw1c	**Device wake-up condition** 0_H device wake-up on a power-on-reset event, write 0 – no action 1_H device wake-up on ENA event, write 1 to clear the flag Reset: 0_H
nu	4	r	**Not used**
SYNC	3	rw1c	**External clock synchronization fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
ENA	2	rw1c	**Enable interrupt event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
CFG2	1	rw1c	**Output voltage configuration change fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
CFG	0	rw1c	**Supervision functions configuration change fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

MCUSF0

Microcontroller status flags 0 – faults **($1D_H$)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
HARDRES	**SOFTRES**	**nu**		**WWDF**	**nu**		**INITF**
rw1c	rw1c	rw1c		rw1c	r		rw1c

Field	Bits	Type	Description
HARDRES	7	rw1c	**Hard reset event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
SOFTRES	6	rw1c	**Soft reset event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	5:4	rw1c	**Not used**
WWDF	3	rw1c	**Window watchdog fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	2:1	r	**Not used**
INITF	0	rw1c	**INIT timer error event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

MCUSF1

Microcontroller status flags 1 – warnings **($1E_H$)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
nu				**WWDMISS**	**nu**		
r				rw1c	r		

Field	Bits	Type	Description
nu	7:4	r	**Not used**
WWDMISS	3	rw1c	**Window watchdog missed trigger event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	2:0	r	**Not used**

SPISF
SPI status flags **($1F_H$)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
nu	**B2VCTRL**	**DEVCTRL**	**LOCK**	**DUR**	**ADDR**	**LEN**	**PAR**
r	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c	rw1c

Field	Bits	Type	Description
nu	7	r	**Not used**
B2VCTRL	6	rw1c	**SPI protocol B2VCTRL access error event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
DEVCTRL	5	rw1c	**SPI protocol DEVCTRL access error event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
LOCK	4	rw1c	**SPI protocol LOCK or UNLOCK access error event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
DUR	3	rw1c	**SPI duration error event** Chip select signal CS "low" for more than 2 ms 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
ADDR	2	rw1c	**SPI invalid address error event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
LEN	1	rw1c	**SPI frame length error event** Number of detected SPI clock cycles different than 16 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
PAR	0	rw1c	**SPI parity error event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

MONSF0

Voltage monitoring status flags 0 – short to ground(20_H) **Reset Value:00_H**

7	6	5	4	3	2	1	0
VM2STG	**VM1STG**	**nu**	**BOOST1STG**	**nu**		**BUCK2STG**	**BUCK1STG**
rw1c	rw1c	r	rw1c	r		rw1c	rw1c

Field	Bits	Type	Description
VM2STG	7	rw1c	**External voltage monitoring 2 short to ground event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
VM1STG	6	rw1c	**External voltage monitoring 1 short to ground event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	5	r	**Not used**
BOOST1STG	4	rw1c	**Boost1 short to ground event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	3:2	r	**Not used**
BUCK2STG	1	rw1c	**Buck2 short to ground event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BUCK1STG	0	rw1c	**Buck1 short to ground event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

MONSF1
Voltage monitoring status flags 1 – overvoltage (21$_H$) **Reset Value:00$_H$**

7	6	5	4	3	2	1	0
VM2OV	**VM1OV**	**nu**	**BOOST1OV**	**nu**		**BUCK2OV**	**BUCK1OV**
rw1c	rw1c	r	rw1c	r		rw1c	rw1c

Field	Bits	Type	Description
VM2OV	7	rw1c	**External voltage monitoring 2 overvoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
VM1OV	6	rw1c	**External voltage monitoring 1 overvoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	5	r	**Not used**
BOOST1OV	4	rw1c	**Boost1 overvoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	3:2	r	**Not used**
BUCK2OV	1	rw1c	**Buck2 overvoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BUCK1OV	0	rw1c	**Buck1 overvoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

MONSF2

Voltage monitoring status flags 2 – undervoltage (22_H) **Reset Value: 00_H**

7	6	5	4	3	2	1	0
VM2UV	**VM1UV**	**nu**	**BOOST1UV**	**nu**		**BUCK2UV**	**BUCK1UV**
rw1c	rw1c	r	rw1c	r		rw1c	rw1c

Field	Bits	Type	Description
VM2UV	7	rw1c	**External voltage monitoring 2 undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
VM1UV	6	rw1c	**External voltage monitoring 1 undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	5	r	**Not used**
BOOST1UV	4	rw1c	**Boost1 undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	3:2	r	**Not used**
BUCK2UV	1	rw1c	**Buck2 undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BUCK1UV	0	rw1c	**Buck1 undervoltage event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

OTSF0
Overtemperature events 0 – faults **(23_H)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
MONOT	**nu**					**BUCK2OT**	**BUCK1OT**
rw1c	r					rw1c	rw1c

Field	Bits	Type	Description
MONOT	7	rw1c	**Monitoring overtemperature fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	6:2	r	**Not used**
BUCK2OT	1	rw1c	**Buck2 overtemperature fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BUCK1OT	0	rw1c	**Buck1 overtemperature fault event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

OTSF1
Overtemperature flags 1 – warnings **(24_H)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
MONOTW	**nu**					**BUCK2OTW**	**BUCK1OTW**
rw1c	r					rw1c	rw1c

Field	Bits	Type	Description
MONOTW	7	rw1c	**Monitoring overtemperature warning event** 0_H no event, write 0 – no action 1_B event detected – write 1 to clear flag Reset: 0_H
nu	6:2	r	**Not used**
BUCK2OTW	1	rw1c	**Buck2 overtemperature warning event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BUCK1OTW	0	rw1c	**Buck1 overtemperature warning event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

OCSF1

Overcurrent flags – warnings **(25_H)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
nu			BOOST1OCW	nu		BUCK2OCW	BUCK1OCW
r			rw1c	r		rw1c	rw1c

Field	Bits	Type	Description
nu	7:5	r	**Not used**
BOOST1OCW	4	rw1c	**Boost1 overcurrent warning event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
nu	3:2	r	**Not used**
BUCK2OCW	1	rw1c	**Buck2 overcurrent warning event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H
BUCK1OCW	0	rw1c	**Buck1 overcurrent warning event** 0_H no event, write 0 – no action 1_H event occurred, write 1 to clear the flag Reset: 0_H

9.1.6 Device status information registers

The device status information registers reflect the current status of the device irrespective of the latched status information in the interrupt flag registers. Therefore, reading these registers reflects the current status of the device, for example the currently active power rails or the temperature warnings.

OTSTAT0
Overtemperature status 0 – warnings **(26_H)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
MONOTW	**nu**					**BUCK2OTW**	**BUCK1OTW**
r	r					r	r

Field	Bits	Type	Description
MONOTW	7	r	**Monitoring overtemperature warning STATUS** 0_H no overtemperature warning 1_B overtemperature warning present Reset: 0_H
nu	6:2	r	**Not used**
BUCK2OTW	1	r	**Buck2 overtemperature warning STATUS** 0_H no overtemperature warning 1_B overtemperature warning present Reset: 0_H
BUCK1OTW	0	r	**Buck1 overtemperature warning STATUS** 0_H no overtemperature warning 1_B overtemperature warning present Reset: 0_H

VMONSTAT0
Voltage monitoring **(27_H)** **Reset Value:00_H**

7	6	5	4	3	2	1	0
VM2OK	**VM1OK**	**R1VSxUV**	**BOOST1OK**	**SYNCOK**	**ENA**	**BUCK2OK**	**BUCK1OK**
r	r	r	r	r	r	r	r

Field	Bits	Type	Description
VM2OK	7	r	**External voltage monitoring 2 STATUS** 0_H output rail disabled or not in total operation band 1_H output rail enabled and in total operation band Reset: 0_H
VM1OK	6	r	**External voltage monitoring 1 STATUS** 0_H output rail disabled or not in total operation band 1_H output rail enabled and in total operation band Reset: 0_H

SPI registers

Field	Bits	Type	Description
R1VSxUV	5	r	**Battery undervoltage STATUS** 0_H battery voltage undervoltage not present. 1_H battery voltage undervoltage present. Reset: 0_H
BOOST1OK	4	r	**Boost1 STATUS** 0_H output rail disabled or not in total operation band 1_H output rail enabled and in total operation band Reset: 0_H
SYNCOK	3	r	**External clock synchronization STATUS** 0_H clock synchronization is not operating 1_H clock synchronization is operating. Reset: 0_H
ENA	2	r	**Enable signal level** 0_H enable signal is "low" 1_H enable signal is "high" Reset: 0_H
BUCK2OK	1	r	**Buck2 STATUS** 0_H output rail disabled or not in total operation band 1_H output rail enabled and in total operation band Reset: 0_H
BUCK1OK	0	r	**Buck1 STATUS** 0_H output rail disabled or not in total operation band 1_H output rail enabled and in total operation band Reset: 0_H

DEVSTAT
Device state information **(28_H)** **Reset Value: 00_H**

7	6	5	4	3	2	1	0
VM2EN	**VM1EN**	**BOOST1EN**	**BUCK2EN**	**nu**	**STATE**		
r	r	r	r	r		r	

Field	Bits	Type	Description
VM2EN	7	r	**External voltage monitoring 2 enable STATUS** 0_H voltage is disabled 1_H voltage is enabled Reset: 0_H
VM1EN	6	r	**External voltage monitoring 1 enable STATUS** 0_H voltage is disabled 1_H voltage is enabled Reset: 0_H
BOOST1EN	5	r	**Boost 1 enable STATUS** 0_H voltage is disabled 1_H voltage is enabled Reset: 0_H

SPI registers

Field	Bits	Type	Description
BUCK2EN	4	r	**Buck 2 enable STATUS** 0_H voltage is disabled 1_H voltage is enabled Reset: 0_H
nu	3	r	**Not used**
STATE	2:0	r	**Device state** 0_H reserved 1_H ACTIVE state 2_H reserved 3_H reserved 4_H reserved 5_H reserved 6_H reserved 7_H reserved Reset: 0_H

PROTSTAT
Protection status information **(29_H)** **Reset Value: 01_H**

7	6	5	4	3	2	1	0
KEY4OK	**KEY3OK**	**KEY2OK**	**KEY1OK**		**nu**		**LOCK**
r	r	r	r		r		r

Field	Bits	Type	Description
KEY4OK	7	r	**Fourth protection key valid STATUS** 0_H key not valid 1_H key valid Reset: 0_H
KEY3OK	6	r	**Third protection key valid STATUS** 0_H key not valid 1_H key valid Reset: 0_H
KEY2OK	5	r	**Second protection key valid STATUS** 0_H key not valid 1_H key valid Reset: 0_H
KEY1OK	4	r	**First protection key valid STATUS** 0_H key not valid 1_H key valid Reset: 0_H
nu	3:1	r	**Not used**
LOCK	0	r	**Lock STATUS** 0_H access to protected registers is unlocked. 1_H access to protected registers is locked. Reset: 0_H

WWDSTAT

Window watchdog status information (2A$_H$) Reset Value:00$_H$

7	6	5	4	3	2	1	0
nu				WWDECNT			
r				r			

Field	Bits	Type	Description
nu	7:4	r	**Not used**
WWDECNT	3:0	r	**Window watchdog error counter level** 0_H 0 1_H 1 ... F_H 15 Reset: 0_H

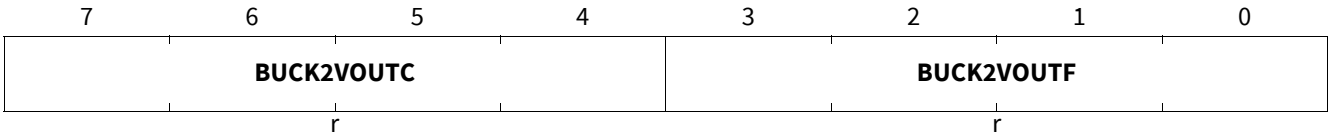
MPSSTAT0

Microcontroller programming support status information(37$_H$) Reset Value:03$_H$

7	6	5	4	3	2	1	0
nu				MPSSTAT			
r				r			

Field	Bits	Type	Description
nu	7:4	r	**Not used**
MPSSTAT	3:0	r	**MPS STATUS** 3_H device in operating mode 6_H device in programming mode 9_H device in test mode (production test mode, read-back only) Reset: 3_H

B2VSTAT
Buck2 output voltage status **(39_H)** **Reset Value:02_H**



Field	Bits	Type	Description
BUCK2VOUTC	7:4	r	**Buck2 output voltage setting coarse resolution STATUS** 0_H Range 0.9 – 1.3 V. Fine resolution is evaluated. 1_H 1.5 V 2_H 1.8 V 3_H 2.45 V 4_H 3.3 V Reset: 00_H
BUCK2VOUTF	3:0	r	**Buck2 output voltage setting fine resolution STATUS** 0_H 1.30 V 1_H 1.20 V 2_H 1.25 V 3_H 1.15 V 4_H 1.10 V 5_H 1.00 V 6_H 1.05 V 7_H 0.95 V 8_H 0.90 V Reset: 02_H

9.1.7 Device information registers

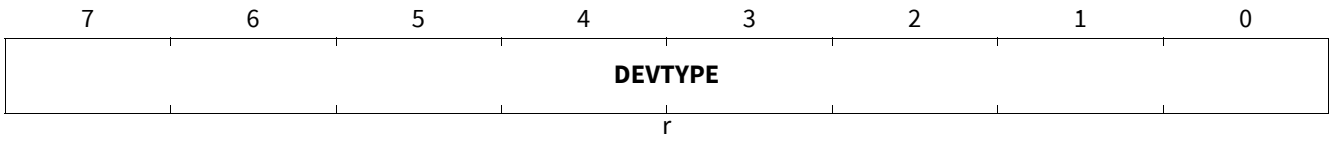
HWDECT0
Hardware option information **($3B_H$)** **Reset Value:$D3_H$**

7	6	5	4	3	2	1	0
VM2AVA	VM1AVA	nu	BOOST1AVA	nu		BUCK2AVA	FRE
r	r	r	r	r		r	r

Field	Bits	Type	Description
VM2AVA	7	r	**External voltage monitoring 2 automatic use detection** 0_H VM2 is not used in this application. 1_H VM2 is used in this application. Reset: 1_H
VM1AVA	6	r	**External voltage monitoring 1 automatic use detection** 0_H VM1 is not used in this application. 1_H VM1 is used in this application. Reset: 1_H
nu	5	r	**Not used**
BOOST1AVA	4	r	**Boost1 automatic use detection** 0_H Boost1 is not used in this application. 1_H Boost1 is used in this application. Reset: 1_H
nu	3:2	r	**Not used**
BUCK2AVA	1	r	**Buck2 automatic use detection** 0_H Buck2 is not used in this application. 1_H Buck2 is used in this application. Reset: 1_H
FRE	0	r	**Frequency selection information** 0_H LF frequency setting 1_H HF frequency setting Reset: 1_H

SPI registers

DEVID
Device identification **($3C_H$)** **Reset Value: 10_H**



Field	Bits	Type	Description
DEVTYPE	7:0	r	**Device family** 10_H TLF30682 device Reset: 10_H

10 Application information

The component values recommended in this section are typical values. The component names in **Table 30** refer to the application diagram in **Figure 12**.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

- Please contact us for additional supportive documentation.
- For further information you may contact **http://www.infineon.com/**

Table 30 Recommended values for the passive components in the application diagram (see Figure 12)

Name	Value	Comments
L_{Buck1}	3.3 µH	Buck1 inductor It is recommended to chose an inductor with a saturation current which is greater than the Buck1 over-current protection threshold $I_{R1,OCP}$.
C_{Buck1_1}	10 µF	Buck1 output capacitor #1 This capacitor should be placed close to the R2VSx input of Buck2 and connected between the R2VSx and R2PGx pins directly. It is recommended to use a ceramic capacitor in X7R material with a voltage rating of 6.3 V or higher.
C_{Buck1_2} C_{Buck1_3}	47 µF	Buck1 output capacitors #2 and #3 It is recommended to use a ceramic capacitor in X7R material with a voltage rating of 6.3 V or higher.
C_{Buck1_BST}	100 nF	Buck1 bootstrap capacitor It is recommended to use a ceramic capacitor in X7R material with a voltage rating of 16 V or higher.
L_{Buck2}	2.2 µH	Buck2 inductor It is recommended to choose an inductor with a saturation current which is greater than the Buck2 over-current protection threshold $I_{R2,OCP}$.
C_{Buck2_1} C_{Buck2_2} C_{Buck2_3}	22 µF	Buck2 output capacitors #1 to #3 It is recommended to use a ceramic capacitor in X7R material with a voltage rating of 6.3 V or higher.
L_{Boost1}	6.8 µH	Boost1 inductor It is recommended to chose an inductor with a saturation current which is greater than the Boost1 over-current protection threshold $I_{R3,OCP}$.
C_{Boost1_1}	100nF	Boost1 output capacitor #1 It is recommended to use a ceramic capacitor in X7R material with a voltage rating of 10 V or higher.
C_{Boost1_2}	10 µF	Boost1 output capacitor #2 It is recommended to use a ceramic capacitor in X7R material with a voltage rating of 10 V or higher.

Note: This following figure is a very simplified example of an application circuit. The function must be verified in the real application.

Application information

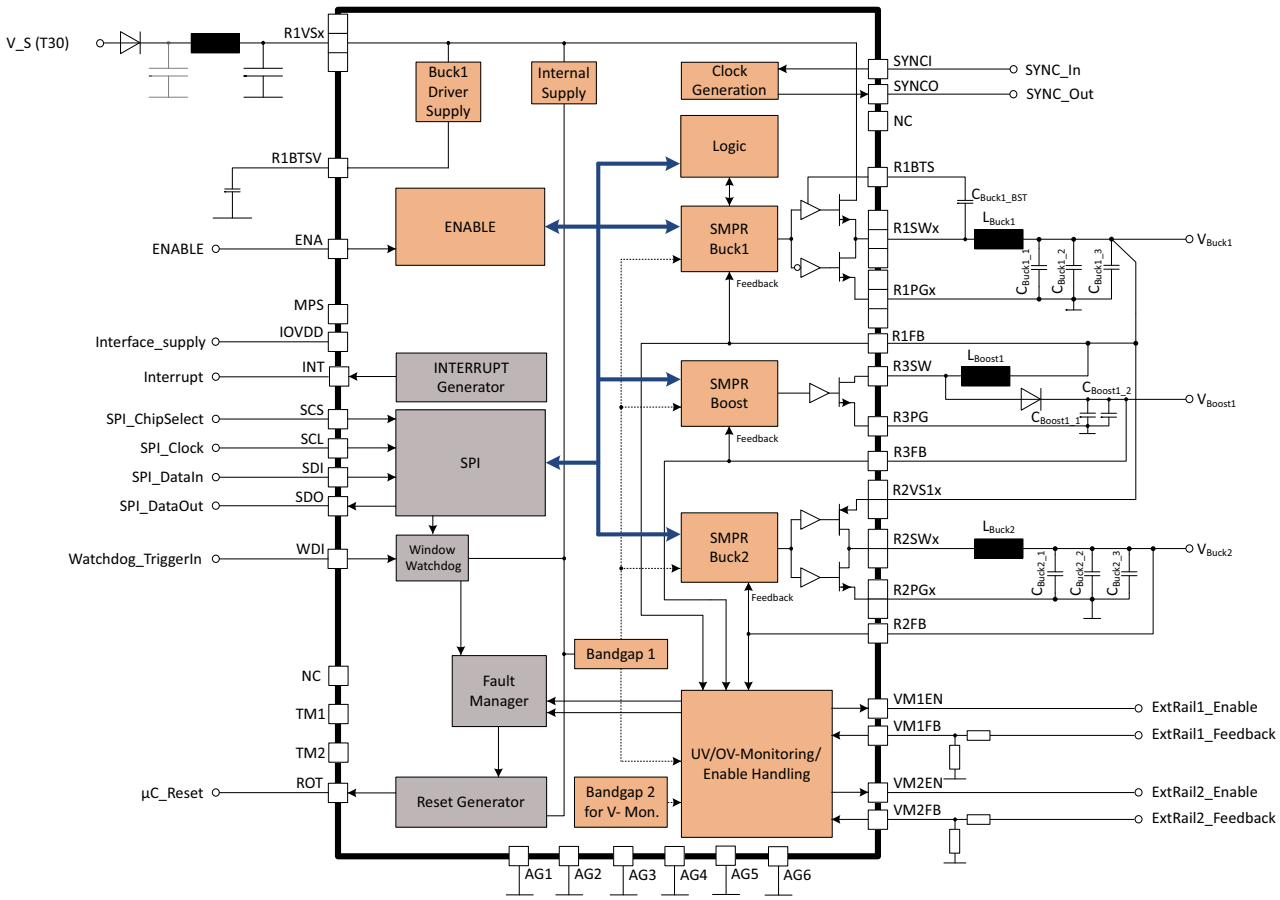


Figure 12 Application diagram

11 Package information

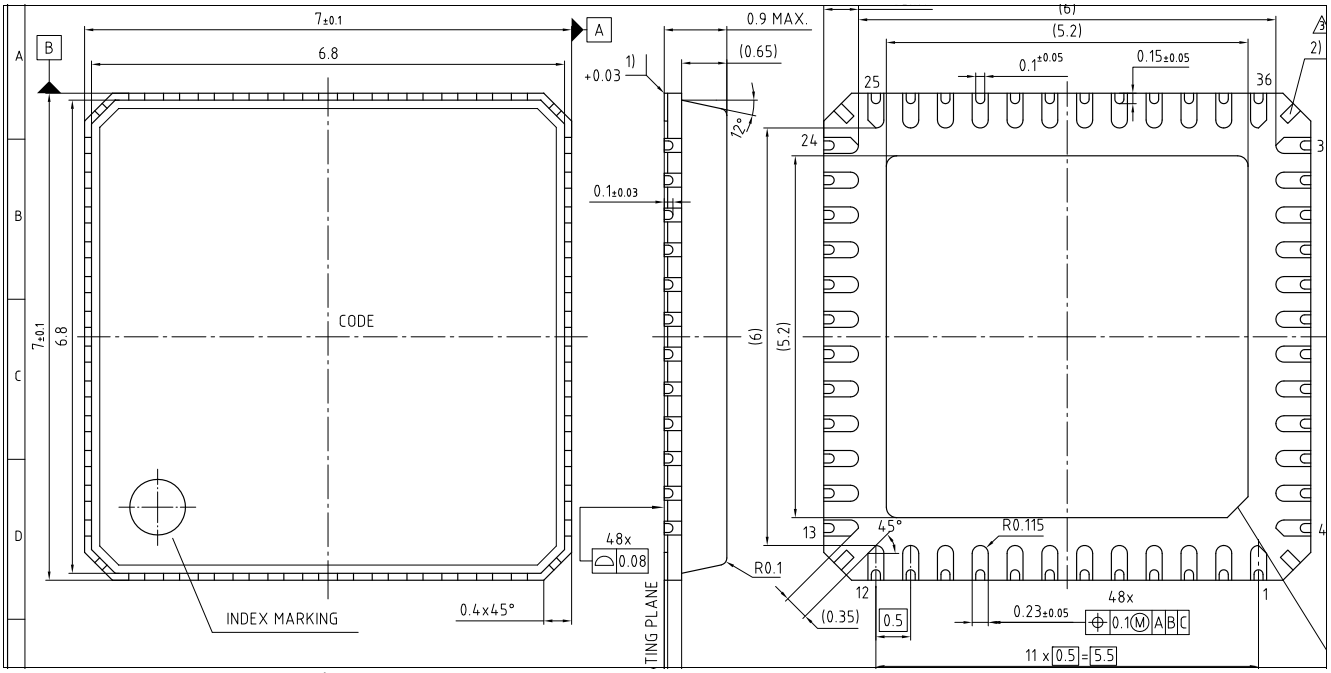


Figure 13 PG-VQFN-48[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

12 Revision History

Revision	Date	Changes
1.01	2019-07-03	Updated meta data.
1.0	2019-04-05	Initial release of data sheet.

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