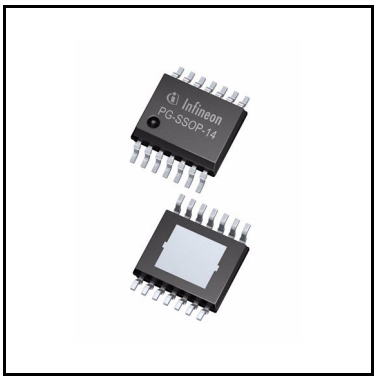
OPTIREG™ linear TLF4277EL

Low drop out linear voltage regulator



Features

- Integrated current monitor
- Adjustable current limitation
- Adjustable output voltage
- Overvoltage detection
- Output current up to 200 mA
- Very low current consumption
- Very low dropout voltage
- Wide input voltage range up to 40 V
- Reverse polarity protection
- Short circuit protected
- Overtemperature shutdown
- Automotive temperature range -40°C ≤ T_j ≤ 150°C
- Green Product (RoHS and WEEE compliant)

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100/101.

Description

The OPTIREG™ linear TLF4277EL is the ideal companion IC to supply active antennas for car infotainment applications. The adjustable output voltage makes the TLF4277EL capable of supplying the majority of standard active antennas such as:

- FM/AM
- DAB
- XM
- SIRIUS

The TLF4277EL is a monolithic integrated low drop out voltage regulator capable of supplying loads up to 200 mA. For an input voltage up to 40 V the TLF4277EL provides an adjustable output voltage in a range from

5 V up to 12 V. The integrated current monitor function is a unique feature that provides diagnosis and system protection functionality. Fault conditions such as overtemperature and output overvoltage are monitored and indicated at the current sense output. The maximum output current limit of the device is adjustable to provide additional protection to the connected load.

Via the enable function the IC can be disabled to lower the power consumption. The PG-SSOP14 EP package provides an enhanced thermal performance within a SO8 body size.

Type	Package	Marking
TLF4277EL	PG-SSOP14 EP	TLF4277

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1 Block diagram

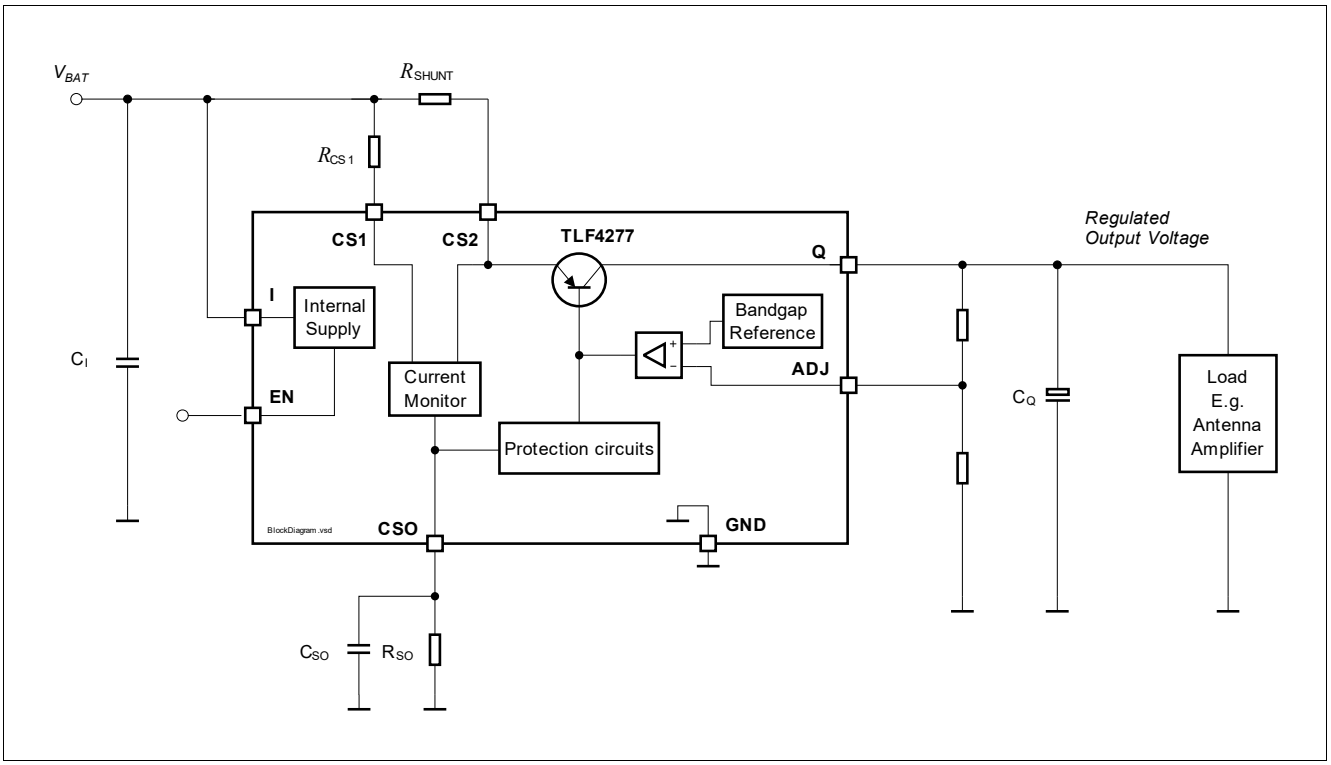


Figure 1 Block and simplified application diagram TLF4277EL (Package PG-SSOP14 EP)

2 Pin configuration

2.1 Pin assignment

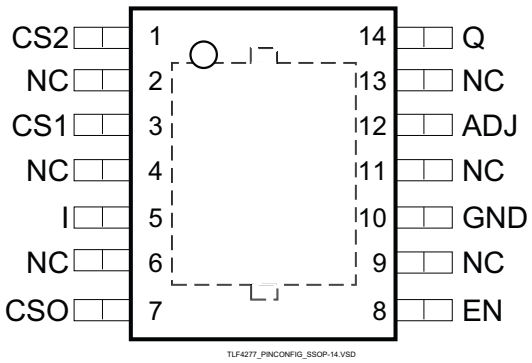


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin no.	Symbol	Function
1	CS2	**Current sense in 2** Current monitor and power stage input.
3	CS1	**Current sense in 1** Current monitor input.
5	I	**IC supply** Place a capacitor from I (pin 5) to GND close to the IC for compensating line influences.
7	CSO	**Current sense out** Current monitor and status output.
8	EN	**Enable** High signal enables the regulator; Low signal disables the regulator; Connect to I, if the enable function is not needed.
10	GND	**Ground** Connect pin to PCB and heat sink area.
12	ADJ	**Voltage adjust** Connect an external voltage divider to configure the output voltage.
14	Q	**Regulator output** Connect a capacitor between Q (pin 8) and GND close to the IC pins, respecting the values given for its capacitance C_Q and ESR in **Table 3**.

Pin configuration

Table 1 Pin definitions and functions (cont'd)

Pin no.	Symbol	Function
–	PAD	**Heat sink** Connect to PCB heat sink area and GND.
2, 4, 6, 9, 11, 13	NC	**Not connected** Internally not connected; Connect to PCB GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage ratings							
IC supply I	V_I	-42	–	45	V	1)	P_4.1.1
Enable input EN	V_{EN}	-42	–	45	V	1)	P_4.1.2
Voltage adjust input ADJ	V_{ADJ}	-0.3	–	10	V	1)	P_4.1.3
Regulator output Q	V_Q	-1	–	40	V	1)	P_4.1.4
Current monitor input CS1	V_{CS1}	-42	–	45	V	1)	P_4.1.5
Current monitor input CS2	V_{CS2}	-42	–	45	V	1)	P_4.1.6
Current monitor out CSO	V_{CSO}	-0.3	–	5	V	1)	P_4.1.7
Temperatures							
Junction temperature	T_j	-40	–	150	°C	1)	P_4.1.8
Storage temperature	T_{stg}	-55	–	150	°C	1)	P_4.1.9
ESD susceptibility							
ESD resistivity to GND	V_{ESD}	-2	–	2	kV	HBM 1)2)	P_4.1.10
ESD resistivity	V_{ESD}	-1	–	1	kV	CDM 1)3)	P_4.1.11

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to AEC-Q-100-002-JESD22-A114.
3) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1.

Notes

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*
2. *Stresses above the ones listed her may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	5	–	40	V	–	P_4.2.1
Input voltage power stage	V_{CS2}	V_Q + 0.5	–	40	V	$V_Q = V_{CS2} - V_{Dr}$	P_4.2.2
Differential input voltage	V_{SHUNT}	0	–	0.5	V	$V_{SHUNT} = V_{BAT} - V_{CS2}$	P_4.2.3
Output voltage range	V_Q	5	–	12	V	–	P_4.2.4
Reference Resistor	R_{CS1}	100	–	1000	Ω	–	P_4.2.5
Current sense output resistor	R_{CSO}	1	–	5	kΩ	–	P_4.2.6
Current sense output capacitor	C_{CSO}	1	–	4.7	µF	–	P_4.2.7
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.8
Output capacitor requirements	C_Q	10	–	–	µF	1)	P_4.2.9
	ESR_{CQ}	–	–	3	Ω	2)	P_4.2.10

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
2) Relevant ESR value at f = 10 kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	–	10	K/W	Measured to the exposed pad 1)	P_4.3.1
Junction to ambient	R_{thJA}	–	150	–	K/W	Footprint only 1)2)	P_4.3.2
		–	64	–	K/W	300 mm² PCB heat sink area 2)	P_4.3.3
		–	55	–	K/W	600 mm² PCB heat sink area 2)	P_4.3.4
		–	50	–	K/W	2s2p PCB 3)	P_4.3.5

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 × 70 µm Cu).
3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4 Voltage regulator

4.1 Description voltage regulator

The output voltage V_Q is controlled by comparing the feedback voltage (V_{ADJ}) to an internal reference voltage and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the output capacitor ESR, the load current and the chip temperature. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the **Table 3.2** have to be maintained. For stability details please refer to the typical performance graph **Output capacitor series resistivity ESRCQ vs. output current IQ**. In addition the output capacitor may need to be sized larger to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals. In general a buffered supply voltage is recommended for the device. For details see **Chapter 8.1**.

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. The integrated safeguards consist of output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, an integrated safe operation monitor lowers the maximum output current input voltages above V_{BAT} = 22 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150°C are outside the maximum ratings and therefore significantly reduce the IC lifetime.

The TLF4277EL allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This reverse current has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

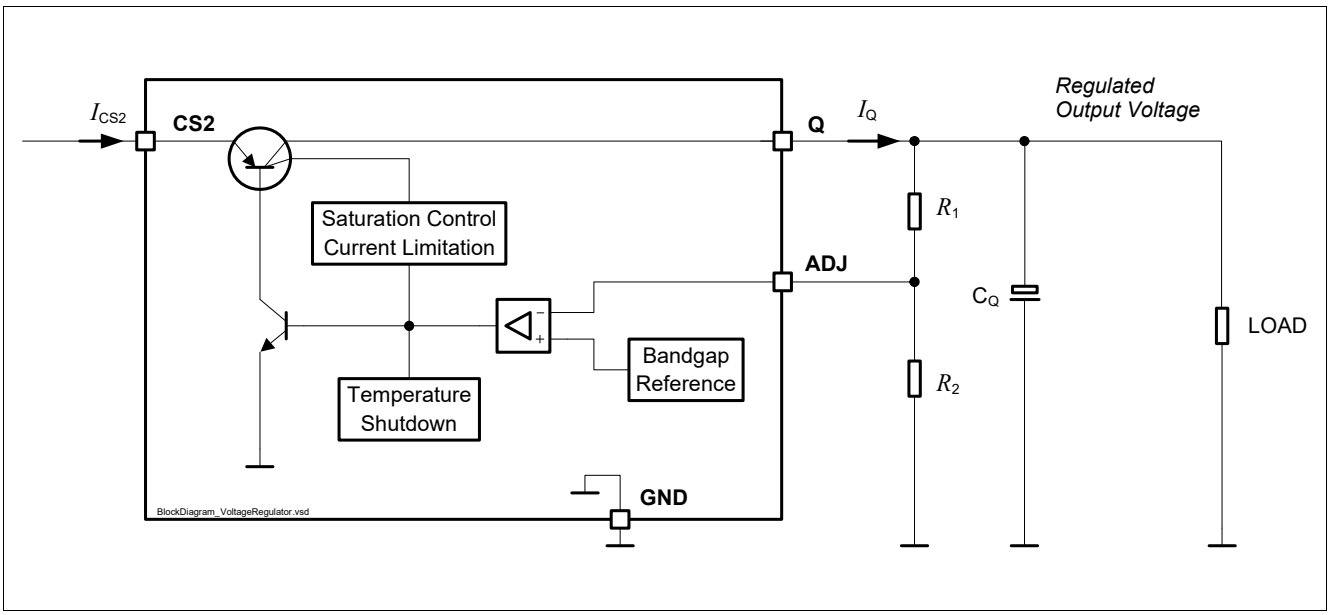


Figure 3 Block diagram voltage regulator circuit

4.2 Electrical characteristics voltage regulator

Table 5 Electrical characteristics: voltage regulator

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference voltage	$V_{REF,int}$	–	1.22	–	V	1)	P_5.2.1
Output voltage tolerance	V_Q	-2	–	2	%	1 mA ≤ I_Q ≤ 200 mA; 9 V ≤ V_{BAT} ≤ 16 V 2)	P_5.2.2
		-2	–	2	%	1 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_{BAT} ≤ 16 V 2)	P_5.2.3
		-2	–	2	%	1 mA ≤ I_Q ≤ 100 mA; 16 V ≤ V_{BAT} ≤ 32 V 2)3)	P_5.2.4
		-2	–	2	%	1 mA ≤ I_Q ≤ 10 mA; 32 V ≤ V_{BAT} ≤ 45 V 2)3)	P_5.2.5
Load regulation steady-state	$\Delta V_{Q,load}$	-30	-5	–	mV	I_Q = 1 mA to 150 mA; V_{BAT} = 6 V V_Q = 5 V	P_5.2.6
Line regulation steady-state	$\Delta V_{Q,line}$	–	5	20	mV	V_{BAT} = 6 V to 32 V; I_Q = 5 mA V_Q = 5 V	P_5.2.7
Power supply ripple rejection	*PSRR*	60	65	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp	P_5.2.8
Dropout voltage $V_{Dr} = V_{CS2} - V_Q$	V_{Dr}	–	120	250	mV	I_Q = 50 mA 4)	P_5.2.9
		–	250	500	mV	I_Q = 150 mA 4)	P_5.2.10
Output current limitation	$I_{Q,max}$	300	–	600	mA	0 V ≤ V_Q ≤ 0.95 × $V_{Q,nom}$; CSO pin connected to GND	P_5.2.11
Reverse current	I_Q	-2	-1	–	mA	V_{BAT} = V_{CS2} = 0 V; V_Q = 5 V	P_5.2.12
Reverse current at negative input voltage	I_{BAT}	-10	-6	–	mA	V_{BAT} = -16 V; V_Q = 0 V	P_5.2.13
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing 1)	P_5.2.14
Overtemperature shutdown threshold hysteresis	$T_{j,hy}$	–	25	–	K	T_j decreasing 1)	P_5.2.15

1) Parameter not subject to production test; specified by design.
2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.
3) See typical performance graph for details.
4) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

4.3 Application information for the setting the variable output voltage

The output voltage of the TLF4277EL can be adjusted between 5 V and 12 V by an external output voltage divider, closing the control loop to the voltage adjust pin ADJ.

The voltage at pin ADJ is compared to the internal reference of typical 1.22 V in an error amplifier. It controls the output voltage.

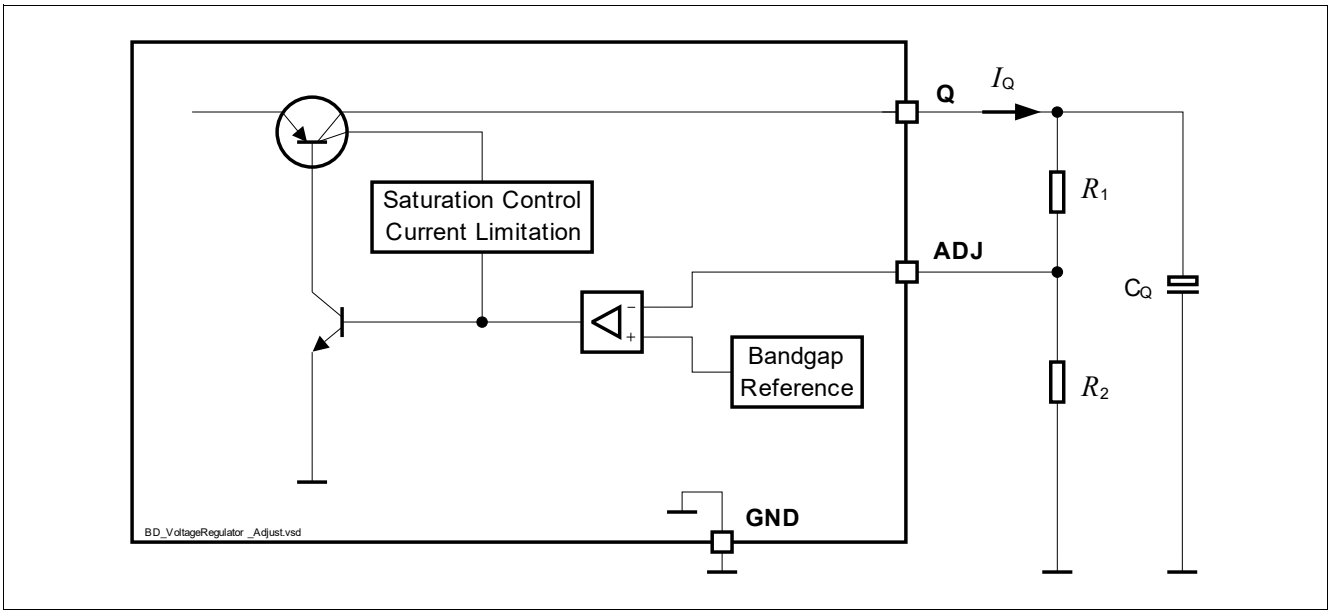


Figure 4 Application detail external components at output for variable voltage regulator

The output voltage is calculated according to **Equation (4.1)**:

$$V_Q = (R_1 + R_2)/R_2 \times V_{REF,int}, \text{ neglecting } I_{ADJ} \quad (4.1)$$

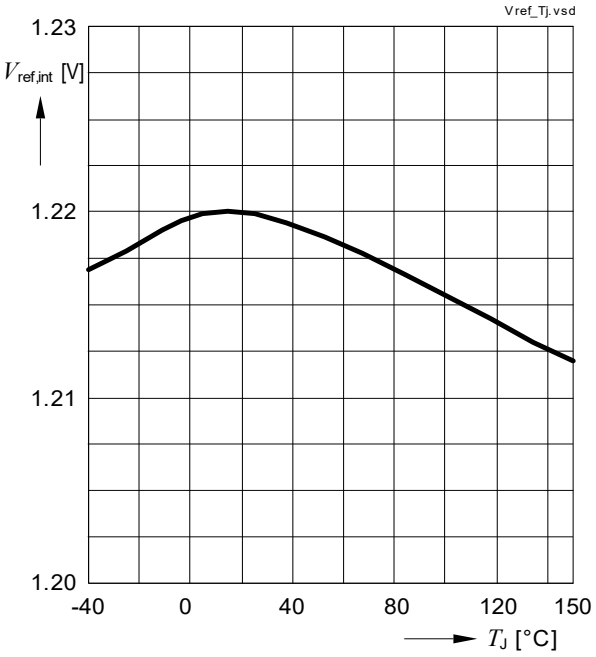
$V_{REF,int}$ is typically 1.22 V.

To avoid errors caused by leakage current I_{ADJ}, we recommend to choose the resistor value for $R_2 < 27$ kΩ.

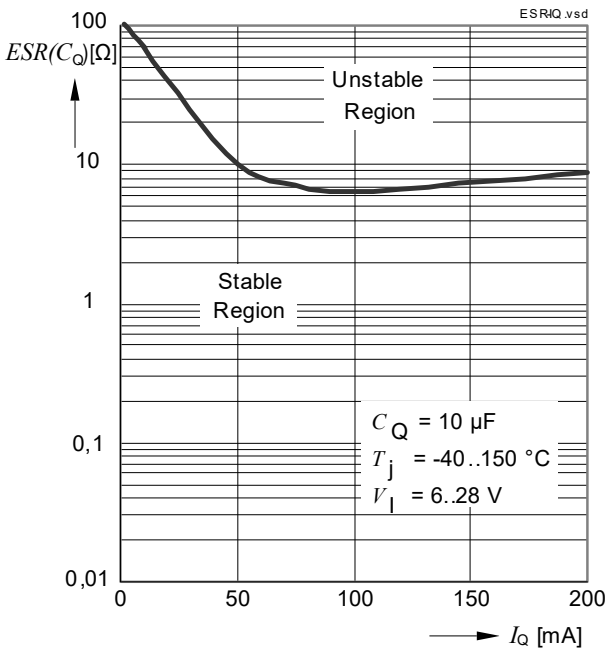
The accuracy of the resistors for the external voltage divider can lead to a higher tolerance of the output voltage.To achieve a reasonable accuracy resistors with a tolerance of 1% or lower are recommended for the feedback divider.

4.4 Typical performance characteristics voltage regulator

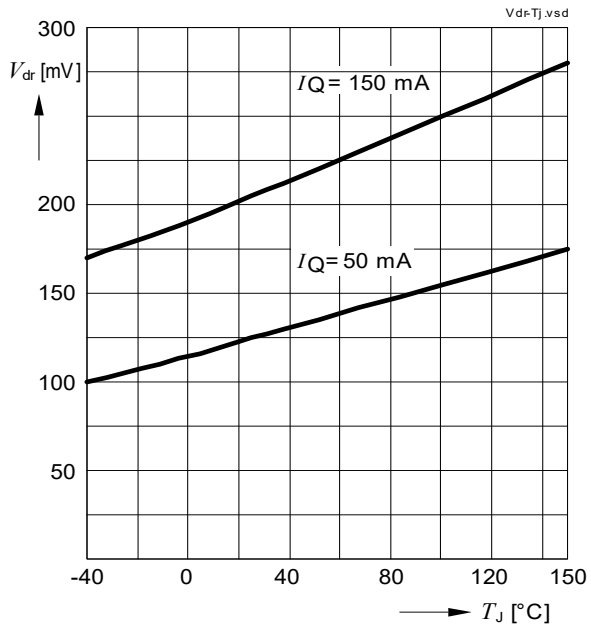
Reference voltage $V_{REF,int}$ vs. junction temperature T_j



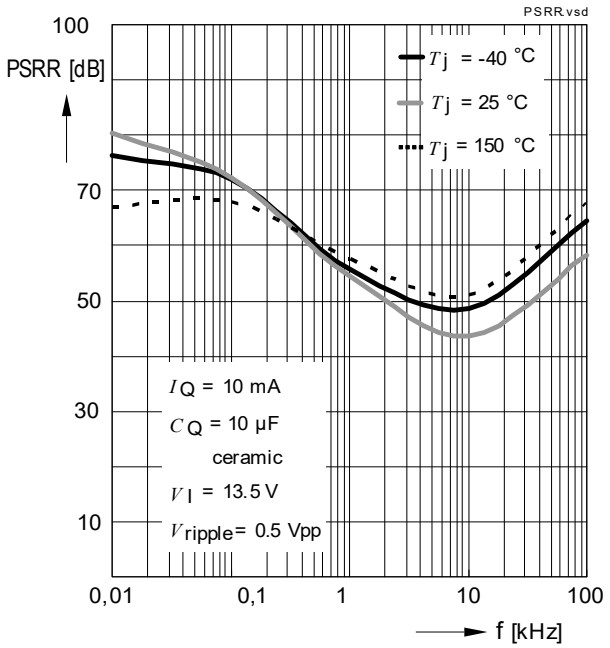
Output capacitor series resistivity ESR_{CQ} vs. output current I_Q



Dropout voltage V_{Dr} vs. output current I_Q



Power supply ripple rejection *PSRR*



5 Current consumption

5.1 Electrical characteristics current consumption

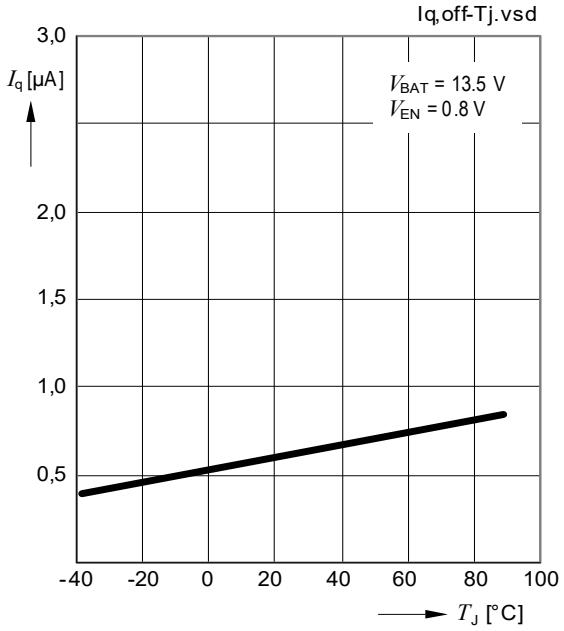
Table 6 Electrical characteristics: current consumption

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground; direction of currents as shown in **Figure 7** (unless otherwise specified)

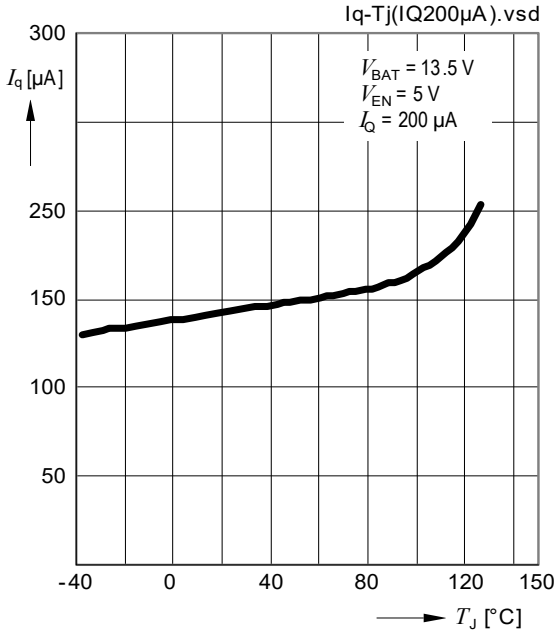
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption	$I_{q,on}$	–	150	200	µA	$I_Q \le 200$ µA; $T_j \le 25$°C; V_{EN} = 5 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.1
		–	175	250	µA	$I_Q \le 200$ µA; $T_j \le 85$°C; V_{EN} = 5 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.2
		–	1.2	2.6	mA	I_Q = 50 mA; V_{EN} = 5 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.3
		–	3.5	6	mA	I_Q = 100 mA; V_{EN} = 5 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.4
		–	5	10	mA	I_Q = 150 mA; V_{EN} = 5 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.5
Current consumption	$I_{q,off}$	–	–	3	µA	$T_j \le 25$°C; V_{EN} = 0.8 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.6
		–	–	5	µA	$T_j \le 85$°C; V_{EN} = 0.8 V; $I_q = I_I + I_{CS2} - I_Q$	P_6.1.7

5.2 Typical performance graphs current consumption

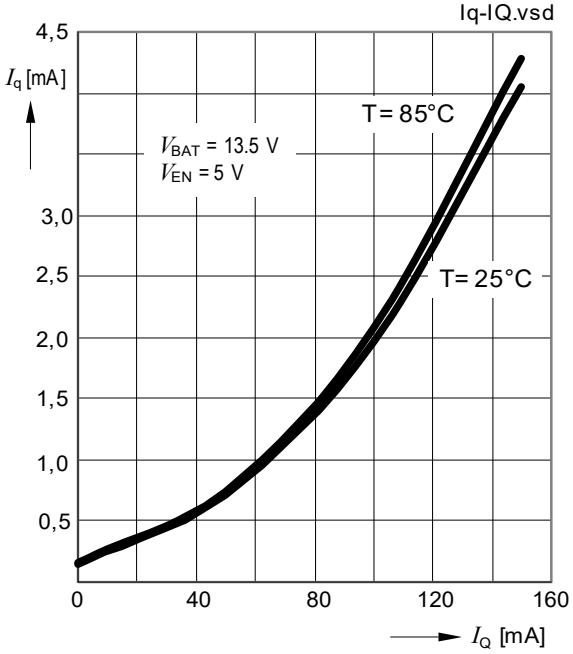
Current consumption $I_{q,off}$ vs. junction temperature T_j



Current consumption $I_{q,on}$ vs. junction temperature T_j



Current consumption $I_{q,on}$ vs. output current I_Q



6 Current and protection monitor functions

6.1 Functional description current and protection monitors

The TLF4277EL provides a set of advanced monitor functionality. The current flowing into the power stage can be monitored at the CSO output. In addition the current limitation can be adjusted via external resistors. Events of the implemented protection functions are reported through dedicated voltage levels at the CSO output. This information can be processed by an external µC for system analysis and failure identification. The monitored events are over-current, overvoltage, and temperature shutdown.

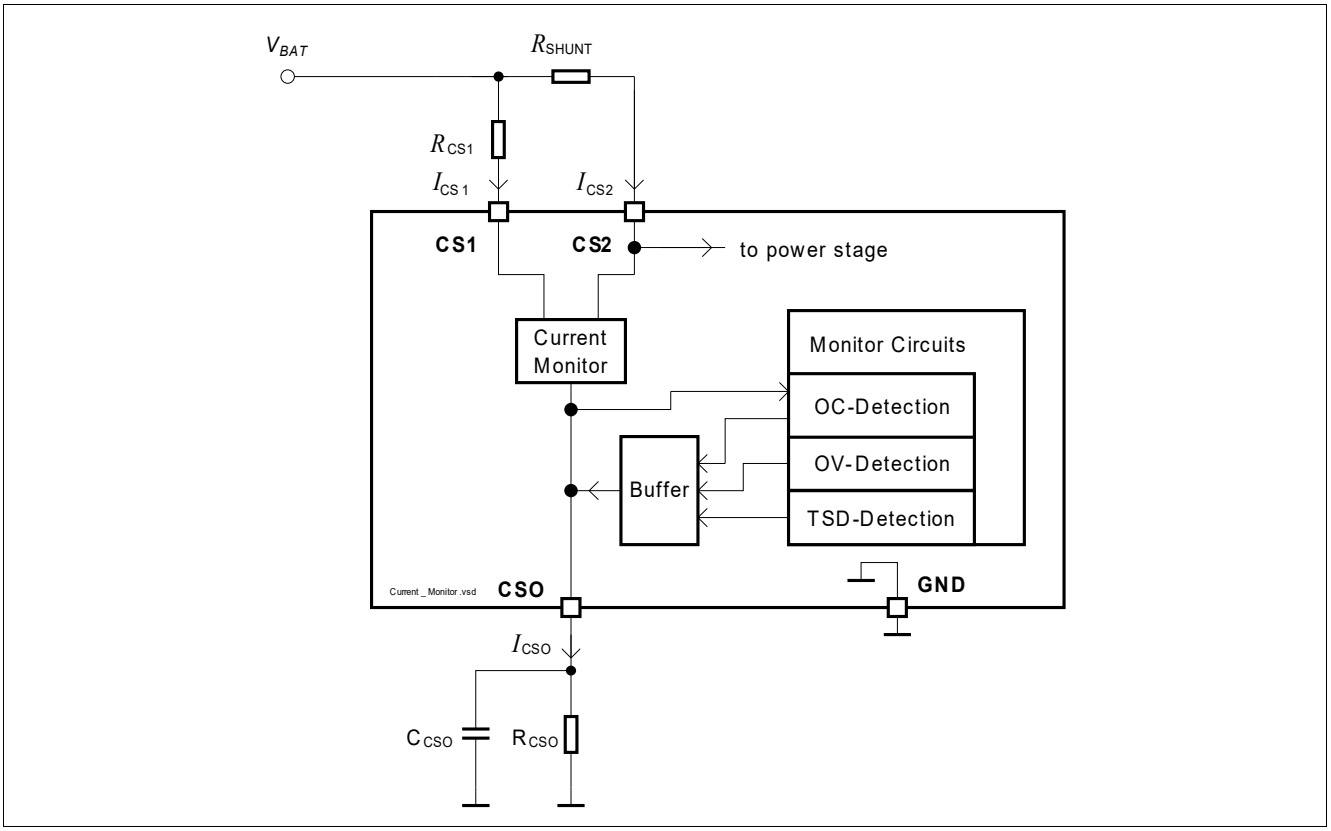


Figure 5 Block diagram current and protection monitor

To reduce possible effects from the supply voltage V_{BAT} additional filtering in of the supply voltage is recommended. A combination of a 100 nF capacitor and an additional buffer capacitor of 10 µF or higher should be placed as close a possible to the IC terminal, which are connected to V_{BAT}.

Figure 6 shows the output level at the CSO pin versus the operation or fault condition. The graph is valid for the following set up of external components:

R_{SHUNT} = 1 Ω

R_{CS1} = 100 Ω

C_{CSO} = 2.2 µF

R_{CSO} = 1.5 kΩ

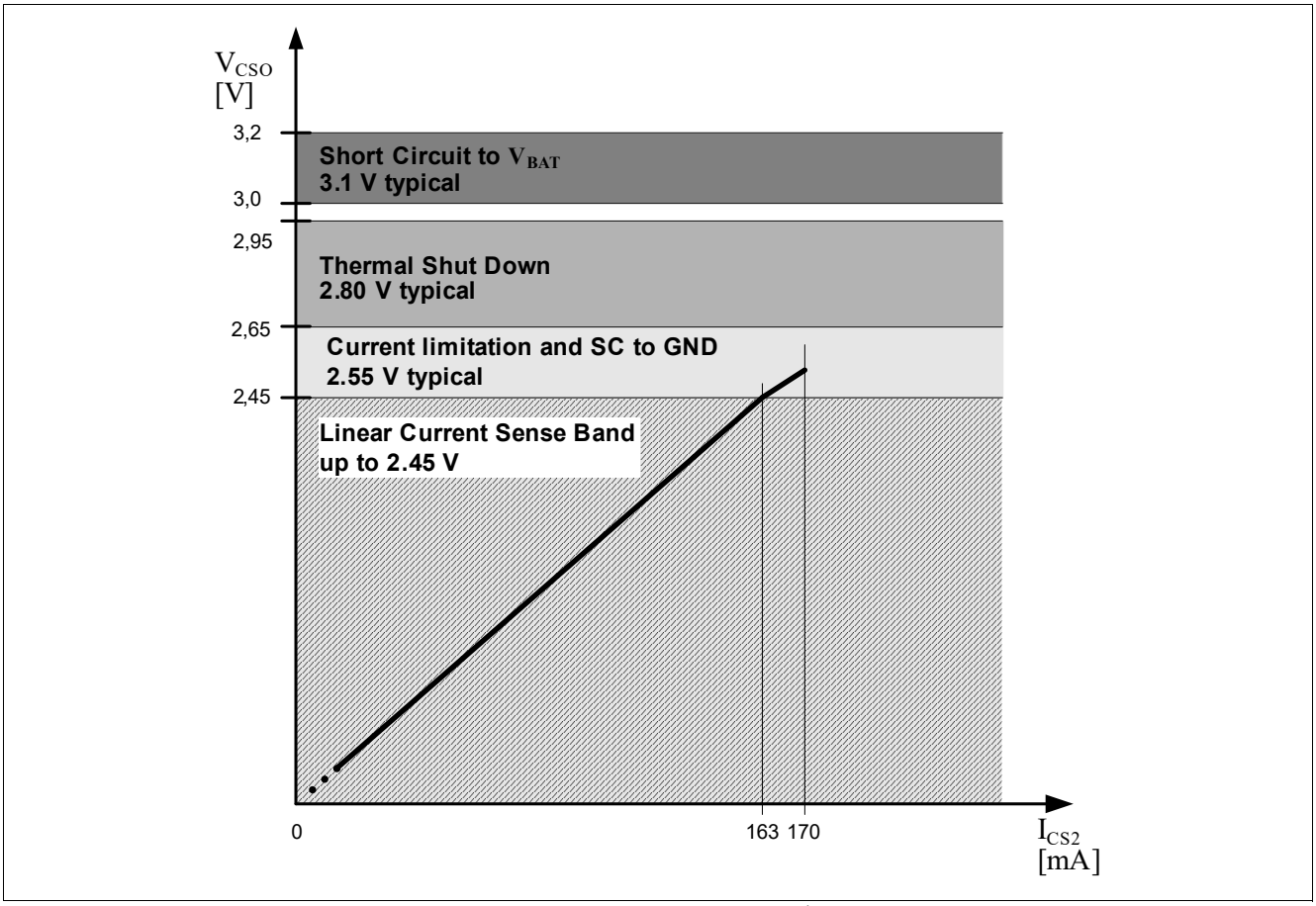


Figure 6 Output levels and functionality of the CSO output[1)]

6.1.1 Linear current monitor

Inside the linear current monitor area the current driven out of the CSO pin is proportional to the voltage which is measured between pin CS1 and CS2.

The level of the current I_{CSO} can be adjusted according to **Equation (6.1)**:

Adjustment I_{CSO}

(6.1)

$$I_{CSO} = \frac{V_{BAT} - V_{CS2}}{R_{CS1}} = I_{CS2} \times \frac{R_{SHUNT}}{R_{CS1}}$$

Adjustment of the voltage level for V_{CSO}

(6.2)

$$V_{CSO} = \frac{(V_{BAT} - V_{CS2}) \times R_{CSO}}{R_{CS1}} = V_{SHUNT} \times \frac{R_{CSO}}{R_{CS1}}$$

1) The graph is just an example and only valid for an certain configuration of the external components.

6.1.2 Adjustable output current limitation

The TLF4277EL has an adjustable current limitation for the current flowing into the power stage (pin CS2). If the level of the voltage drop across the sense resistor R_{SHUNT} is higher than the desired linear monitor range the output current of the TLF4277EL will be limited.

Setting of the adjustable current limitation

(6.3)

$$I_{CS2,lim} = \frac{2.55V \times R_{CS1}}{R_{SHUNT} \times R_{CSO}}$$

A voltage level as defined in **VCSO,cur_lim** will be applied at the CSO pin.

To achieve a current limitation of 170 mA the following configuration can be used:

(6.4)

$$I_{CS2,lim} = \frac{2.55V \times 100\Omega}{1\Omega \times 1.5k\Omega} = 170mA$$

R_{SHUNT} = 1 Ω
R_{CS1} = 100 Ω
R_{CSO} = 1.5 kΩ

6.1.3 Overvoltage detection

To detect a possible short circuit of the output to a higher supply rail the TLF4277EL has an overvoltage detection implemented. An overvoltage will be detected, if the voltage level at the ADJ pin is 20% higher than the internal reference voltage $V_{REF,int}$ defined in **Table 5**.

Under this condition the CSO pin will be driven through an internal voltage buffer with a voltage level as defined in **VCSO,OV**.

6.1.4 Thermal shutdown detection

If the junction temperature will exceed the limits defined in the **Table 5** the TLF4277EL will disable the output voltage. In this case a voltage level as defined in **VCSO,TSD** will be applied at the CSO pin.

6.2 Electrical characteristics current and protection monitor

Table 7 Electrical characteristics: current monitor function

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Linear Current Monitor							
Current sense output current I_{CSO} (V_{SHUNT} = 10 mV)	I_{CSO}	0.08	0.1	0.12	mA	T_j=25°C R_{SHUNT} = 1 Ω R_{CS1} = 100 Ω R_{CSO} = 1.5 kΩ [1]	P_7.2.1
(V_{SHUNT} = 50 mV)		0.47	0.5	0.53	mA		P_7.2.2
(V_{SHUNT} = 100 mV)		0.97	1	1.03	mA		P_7.2.3
(V_{SHUNT} = 150 mV)		1.45	1.5	1.55	mA		P_7.2.4
Adjustable current limitation							
Adjustable current limit	$I_{CS2,lim}$	162	170	187	mA	R_{SHUNT} = 1 Ω R_{CS1} = 100 Ω R_{CSO} = 1.5 kΩ $V_Q < 0{,}95 \times V_{Q,nom}$ [1]	P_7.2.5
CSO voltage level Current limitation	V_{CSO,cur_lim}	2.45	2.55	2.65	V	R_{SHUNT} = 1 Ω R_{CS1} = 100 Ω R_{CSO} = 1.5 kΩ $V_Q < 0{,}95 \times V_{Q,nom}$ [1]	P_7.2.6
Output level overvoltage detected							
CSO voltage level Overvoltage detected	$V_{CSO,OV}$	3.0	3.1	3.2	V	$V_{ADJ} > 1.2 \times V_{REF,nom}$ [1]	P_7.2.7
Output level overtemperature detected							
CSO voltage level Overtemperature detected	$V_{CSO,TSD}$	2.65	2.8	2.95	V	150°C < T_j < 180°C [2]	P_7.2.8

1) Referring to the device tolerance only, the tolerance of the external components can cause additional deviation.

2) Specified by design; not subject to production test.

7 Enable function

7.1 Description enable function

The TLF4277EL can be turned on or turned off via the EN Input. With voltage levels higher than $V_{EN,high}$ applied to the EN input the device will be completely turned on. A voltage level lower than $V_{EN,low}$ sets the device to low quiescent current mode. In this condition the device is turned off and is not functional. The enable input has an build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input.

7.2 Electrical characteristics enable function

Table 8 Electrical characteristics: enable function

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable Low signal valid	$V_{EN,low}$	–	–	0.8	V	–	P_8.2.1
Enable High signal valid	$V_{EN,high}$	2	–	–	V	V_Q settled	P_8.2.2
Enable Threshold hysteresis	$V_{EN,hyst}$	50	–	–	mV	–	P_8.2.3
Enable Input current	I_{EN}	–	–	2	µA	V_{EN} = 5 V	P_8.2.4
Enable Internal pull-down resistor	R_{EN}	3	4.5	6	MΩ	–	P_8.2.5

8 Application information

8.1 Measurement circuit

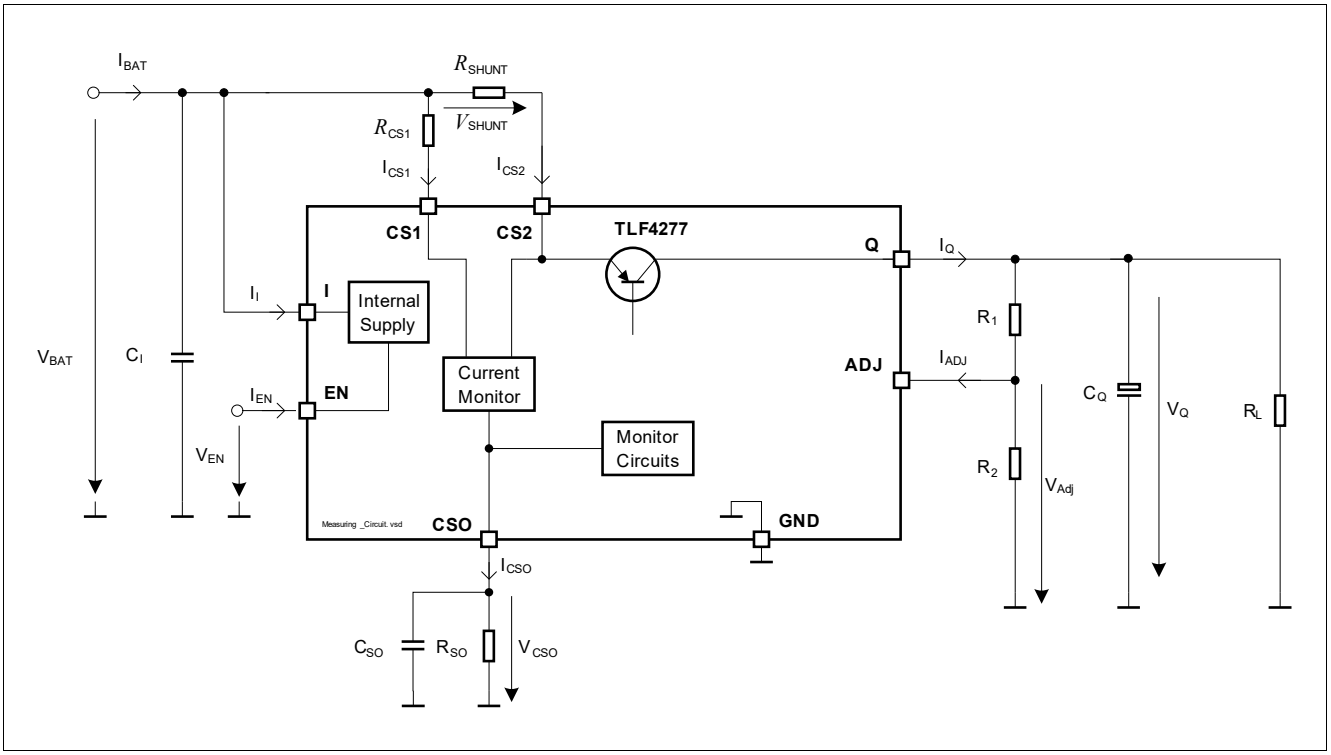


Figure 7 Measuring circuit

Measurement set up:

R_{SHUNT} = 1 Ω

R_{CS1} = 100 Ω

C_{CSO} = 2.2 µF

R_{CSO} = 1.5 kΩ

R_1 = 38 kΩ

R_2 = 12 kΩ

C_Q = 10 µF

9 Package information

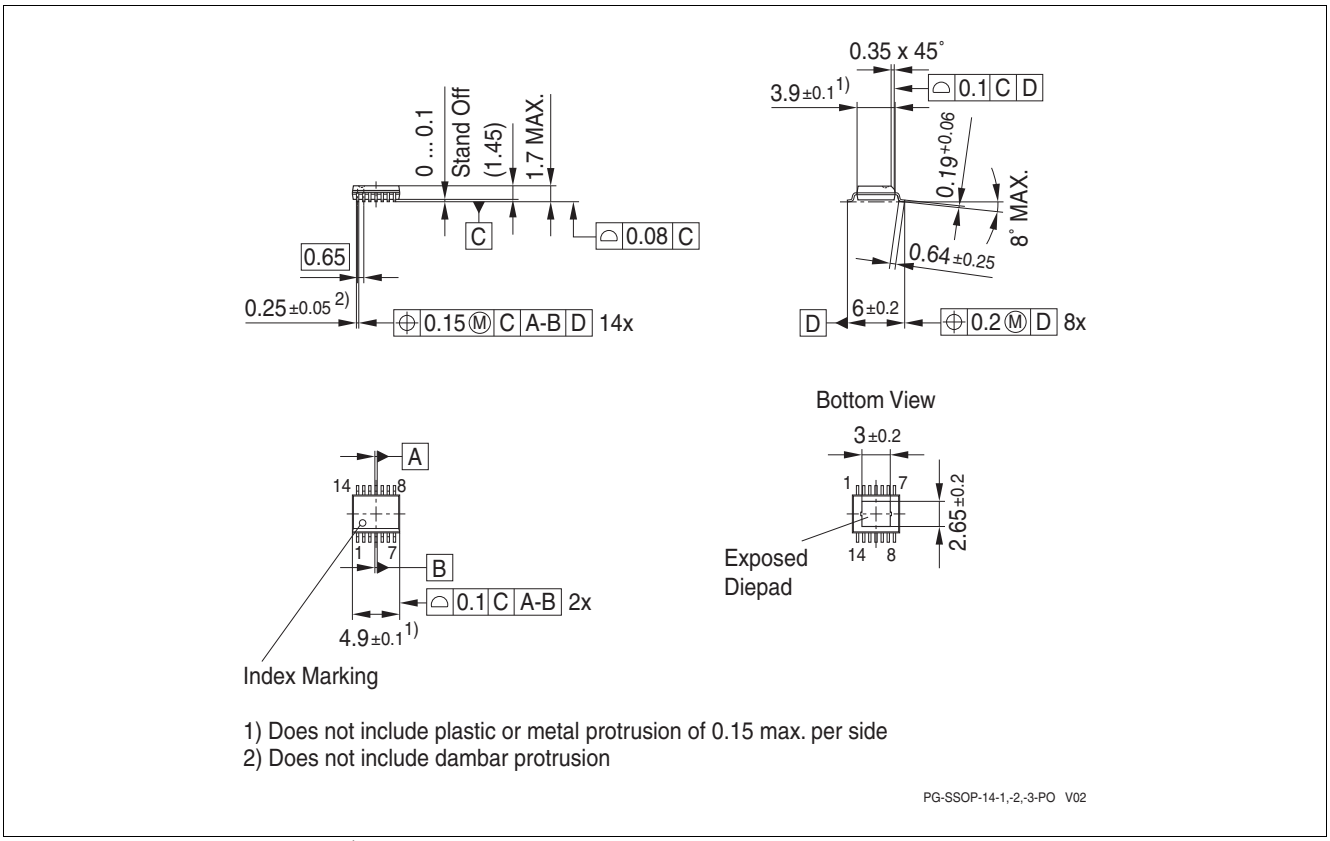


Figure 8 PG-SSOP14 EP[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

10 Revision history

Revision	Date	Changes
1.1	2022-03-08	Updated layout and structure. Editorial changes.
1.02	2011-07-04	Updated cover page. Fixed linear current monitor formulas (2,3) on **Page 16**.
1.01	2011-05-07	Template update.
1.0	2009-05-07	Initial release.

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