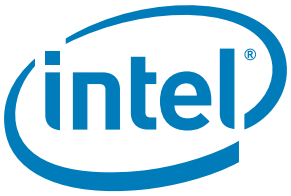


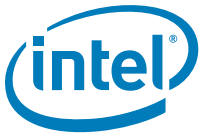
Intel® Atom™ Processor D400 and D500 Series

Datasheet- Volume One

This is volume 1 of 2. Refer to document 322845 for Volume 2

June 2010

Document Number: 322844-002



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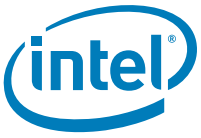
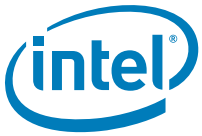




Figures

Tables

Revision History

Revision Number	Description	Revision Date
001	• Initial Release	December 2009
002	• Added DDR3 SKU	June 2010

§

1 Introduction

The Intel® Atom™ Processor D400 and D500 Series processors are built on 45-nanometer Hi-K process technology. The processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the chipset and enables higher performance, lower cost, easier validation, and improved x-y footprint.

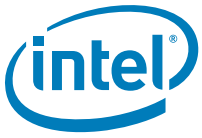
Note: Throughout this document, Intel® Atom™ Processor D400 and D500 Series is referred to as processor and Intel® NM10 Express Chipset is referred to as chipset.

Included in this family of processors is an integrated memory controller (IMC), integrated graphics processing unit (GPU) and integrated I/O (IIO) (such as DMI) on a single silicon die. This single die solution is known as a monolithic processor.

1.1 Intel® Atom™ Processor D400 and D500 Series Features

The following list provides some of the key features on this processor:

- On die, primary 32-kB instructions cache and 24-kB write-back data cache
- Intel® Hyper-Threading Technology 2-threads per core
- On die 2 x 512-kB, 8-way L2 cache for D510 dual-core processor, 1 x 512-kB, 8-way L2 cache for D410 single-core processor
- Support for IA 32-bit
- Intel® Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3) and Supplemental Streaming SIMD Extensions 3 (SSSE3) support
- Intel® 64 architecture
- Micro-FCBGA8 packaging technologies
- Thermal management support via Intel® Thermal Monitor (TM1)
- Supports C0 and C1 states only
- Execute Disable Bit support for enhanced security



1.2 System Memory Features

- DDR2 (D410, D510, D425, and D525)
  - — One channel of DDR2 memory (consists of 64 data lines):
    - ■ Maximum of two DIMMs per channel, containing single or double-sided DIMM
  - — Memory DDR2 data transfer rates of 667 and 800 MT/s
  - — Only non-ECC DIMMs are supported
  - — Support unbuffered DIMMs
  - — I/O Voltage of 1.8V for DDR2
  - — Supports 512-Mb, 1-Gb & 2-Gb technologies for DDR2
  - — Support 4 banks for 512 Mbit densities for DDR2
  - — Support 8 banks for 1-Gb and 2-Gb densities for DDR2
  - — Support 2 DIMMs, 4 GB (assuming 2-Gb density device technology) maximum
  - — Support up to 32 simultaneous open pages per channel (assuming 4 ranks of 8i devices)
  - — Support Partial Writes to memory using Data Mask signals (DM)
  - — Enhances Address Mapping
  - — Support DIMM page size of 4KB and 8KB
  - — Support data burst length of 8 for all memory configurations
  - — Support memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered by either on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.
- DDR3 SO-DIMM only (D525 and D425)
  - — Support for DDR3 at data transfer rate of 800 MT/s only
  - — One channel of DDR3 memory (consists of 64-bit data lines); maximum of 2 SO-DIMMs in Raw Card A or Raw Card B format
  - — I/O Voltage of 1.5 V for DDR3
  - — Maximum of 4GB memory capacity supported
  - — Memory organizations supported (refer to Platform Design Guide for more details)

    2 SO-DIMM

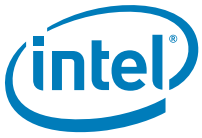
    1 SO-DIMM

1.3 Direct Media Interface Features

- Compliant to Direct Media Interface (DMI)
- Support 4 lanes in each direction, 2.5 Gbps per lane per direction, point-to-point DMI interface to Intel® NM10 Express Chipset.
- 100 MHz reference clock.
- Support 64 bit downstream address (only 36-bit addressable from CPU)
- Support APIC messaging support. Will send Intel-defined “End of Interrupt” broadcast message when initiated by CPU.
- Support messaging in both directions, including Intel-Vendor specific messages.
- Support Message Signal Interrupt (MSI) messages.
- Support Power Management state change messages.
- Support SMI, SCI and SERR error indication.
- Support PCI INTA interrupt from CHAP Counters device and Integrated Graphics.
- Support legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive and LPC bus masters.
- Support Intel NM10 Express Chipset with on board hybrid AC-DC coupling solution.
- Support x4 link width configuration.
- Support polarity inversion

1.4 Graphics Processing Unit Features

- The GPU contains a refresh of the 3rd generation graphics core
- Intel® Dynamic Video Memory Technology support 4.0
- Directx* 9 compliant Pixel Shader* v2.0
- 400 MHz render clock frequency
- 2 display ports: LVDS and RGB
  - — Single LVDS channel supporting resolution up to 1366 * 768, 18bpp
  - — Analog RGB display output resolution up to 2048 * 1536@ 60 Hz
- Intel® Clear Video Technology
  - — MPEG2 Hardware Acceleration
  - — ProcAmp



1.5 Clocking

- Differential Core clock of 166MHz and 200 MHz (BCLKP/BCLKN). Core clock and Host clock need to match one another. If Core clock is 166 MHz, Host clock needs to be 166 MHz.
- Differential Host clock of 166 MHz and 200 MHz (HPL_CLKINP/HPL_CLKINN).
- Memory clocks
  - When running DDR2-667, memory clocks are generated from internal Host PLL.
  - When running DDR2-800, memory clocks are generated from the Memory PLL
- The differential DMI clock of 100 MHz (EXP_CLKINP/EXP_CLKINN) generates the DMI core clock of 250 MHz.
- Display timings are generated from display PLLs that use a 96 MHz differential SSC and non-SSC, and 100 MHz differential clock with SSC as reference.
- Host, Memory, DMI, Display PLLs and all associated internal clocks are disabled until PWROK is asserted.

1.6 Power Management

- PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 kB)
- Support extended SMRAM space above 256 MB, additional 1MB TSEG from the base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by CPU).
- ACPI Rev 1.0b compatible power management
- Support CPU states: C0 and C1
- Support System states: S0, S3, S4 and S5
- Support CPU Thermal Management 1 (TM1)

1.6.1 Terminology

Term	Description
BGA	Ball Grid Array
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR2	Second generation Double Data Rate SDRAM memory technology
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code

Term	Description
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Micro-FBGA	Micro Flip Chip Ball Grid Array
(G)MCH	Legacy component - Graphics Memory Controller Hub. Platforms designed for the Intel Atom Processor D400 and D500 Series do not use an (G)MCH.
GPU	Graphics Processing Unit
ICH	The legacy I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the legacy (G)MCH over a proprietary interconnect called DMI. Platforms designed for the Intel® Atom™ Processor D400 and D500 Series do not use an ICH.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
LCD	Liquid Crystal Display
LLC	Last Level Cache. The LLC is the shared cache amongst all processor execution cores
LVDS	Low Voltage Differential Signaling A high speed, low power data transmission standard used for display connections to LCD panels.
MCP	Multi-Chip Package
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
Processor	The 64-bit, single-core or multi-core component (package)
Processor Core	The term “processor core” refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
SMT	Simultaneous Multi-Threading

Term	Description
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to “free air” (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TOM	Top of Memory
TTM	Time-To-Market
V_{CC}	Processor core power supply
V_{SS}	Processor ground
V_{CCGFX}	Graphics core power supply
V_SM	DDR2 power rail
VLD	Variable Length Decoding

1.7 References

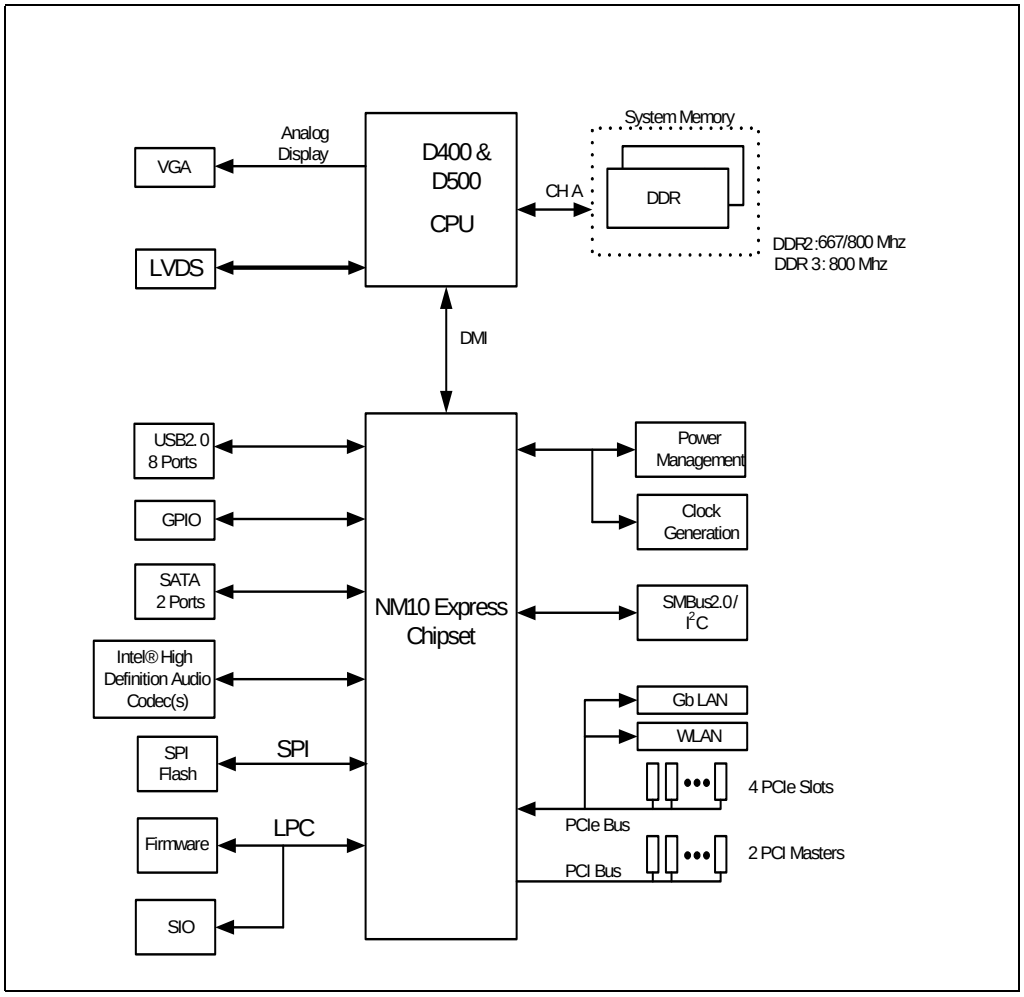
Material and concepts available in the following documents may be beneficial when reading this document:

Table 1-1. References

Document	Document Number
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/products/processor/manuals/index.htm
Intel® Atom™ Processor D500 Specification Update	322862-002
Intel® Atom™ Processor D400 Specification Update	322861-002
Intel® Atom™ Processor D400 and D500 Series Thermal Mechanical Design Guidelines	322856-002
Intel® NM10 Express Chipset Datasheet	322896-001
Intel® NM10 Express Chipset Specification Update	322897-001

1.8 System Block Diagram

Figure 1-1. Intel Atom Processor D400 and D500 Series System Block Diagram



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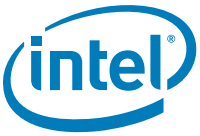


2 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type:

Table 2-2. Signal Type

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal.

Table 2-3. Signal Description Buffer Types

Signal	Description
CMOS	CMOS buffers. 1.05 V tolerant
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signalling Environment AC Specifications but are DC coupled. The buffers are not 3.3V tolerant.
HVCMOS	High Voltage buffers. 3.3V tolerant
DDR2	DDR2 buffers: 1.8 V tolerant
GTL+	Open Drain Gunning Transceiver Logic signaling technology. Refer to GTL+ I/O Specification fro complete details.
TAP	Test Access Port signal
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Ref	Voltage reference signal
Asynch	This signal is asynchronous and has no timing relationship with any reference clock.
LVDS	Low Voltage Differential Signalling. A high speed, low power data transmission standard used for display connections to LCD panels.
SSTL - 1.8	Stub Series Termination Logic. These are 1.8V output capable buffers. 1.8V tolerant.

2.1 CPU Legacy Signal

Table 2-4. CPU Legacy Signal

Signal Name	Description	Direction	Type
A20M#	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.	I	Core CMOS
BSEL[2:0]	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency.	O	Core CMOS
EXTBGREF	External Bandgap Reference. Debug feature.	I	Core Analog
FERR#/PBE#	FERR# (Floating-point Error)/PBE# (Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*- type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *Intel® Processor Identification and CPUID Instruction Application Note*. For termination requirements, refer to the platform design guide.	O	Core Open Drain

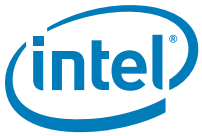


Table 2-4. CPU Legacy Signal

Signal Name	Description	Direction	Type
IGNNE#	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.	I	Core CMOS
INIT#	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.	I	Core CMOS
LINT00, LINT10	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT00 signal becomes INTR, a maskable interrupt request signal, and LINT10 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT00/LINT10. Because the APIC is enabled by default after Reset, operation of these pins as LINT00/LINT10 is the default configuration.	I	Core CMOS

Table 2-4. CPU Legacy Signal

Signal Name	Description	Direction	Type
CPUPWRGOOD	CPUPWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Rise time and monotonicity requirements are shown in Chapter 4 Electrical Specifications. CPUPWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of CPUPWRGOOD. It must also meet the minimum pulse width specification. The CPUPWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	I	Core CMOS
SMI#	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.	I	Core CMOS
STPCLK#	Stop clock.	I	Core CMOS
GTLREF	GTL reference voltage for BPM* pins. Refer Platform Design Guide for connection recommendation.	I	Core Analog
THERMDA_1 THERMDC_1	Thermal Diode - Anode & Cathode. Suffix 1 refers to core #1. Suffix 1 refers to core #1.	I O	Core Analog
THERMDA_2 THERMDC_2	Thermal Diode - Anode & Cathode. Suffix 2 refers to core #2. Suffix 2 refers to core #2. No connect for single-core processor.	I O	Core Analog
BPM_1#[3:0] BPM_2#[3:0]	Breakpoint and Performance Monitor Signals: Output from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM_2# is no connect for single-core processor.	I/O	GTL+
PRDY#	PRDY# is a processor output used by debug tools to determine processor debug readiness.	I/O	GTL+

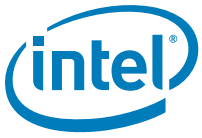


Table 2-4. CPU Legacy Signal

Signal Name	Description	Direction	Type
PREQ#	PREQ# is used by debug tools to request debug operation of the processor.	I	GTL+
DPRSTP#	DPRSTP# when asserted on the platform causes the processor to transition from Deep Sleep State to the Deeper Sleep State. To return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the chipset. This function is not supported for Intel Atom Processor D400 and D500 Series.	I	Core CMOS
DPSLP#	DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep State. To return to the Sleep State, DPSLP# must be de-asserted. DPSLP# is driven by the chipset. This function is not supported for Intel Atom Processor D400 and D500 Series.	I	Core CMOS

2.2 System Memory Interface

Table 2-5. Memory Channel A

Signal Name	Description	Direction	Type
DDR_A_CK_5:0	SDRAM Differential Clock: (3 per DIMM)	O	SSTL-1.8
DDR_A_CKB_5:0	SDRAM Inverted Differential Clock: (3 per DIMM)	O	SSTL-1.8
DDR_A_CSB_3:0	Chip Select: (1 per Rank)	O	SSTL-1.8
DDR_A_CKE_3:0	Clock Enable: (power management - 1 per Rank)	O	SSTL-1.8
DDR_A_MA_14:0	Multiplexed Address	O	SSTL-1.8
DDR_A_BS_2:0	Bank Select	O	SSTL-1.8
DDR_A_RASB	RAS Control Signal	O	SSTL-1.8
DDR_A_CASB	CAS Control Signal	O	SSTL-1.8
DDR_A_WEB	Write Enable Control Signal	O	SSTL-1.8
DDR_A_DQ_63:0	Data Lines	I/O	SSTL-1.8 2x
DDR_A_DM_7:0	Data Mask: These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes	O	SSTL-1.8 2x
DDR_A_DQS_7:0	Data Strobes	I/O	SSTL-1.8 2x
DDR_A_DQSB_7:0	Data Strobe Complements (DDR2)	I/O	SSTL-1.8 2x
DDR_A_ODT_3:0	On Die Termination: Active Termination Control (DDR2)	O	SSTL-1.8 2x

Table 2-6. Memory Reference and Compensation

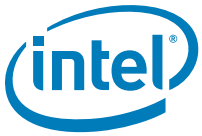
Signal Name	Description	Direction	Type
DDR_RPD	System Memory RCOMP signal. Refer Platform Design for connection recommendation.	I/O	Analog
DDR_RPU	System Memory RCOMP signal. Refer Platform Design for connection recommendation.	I/O	Analog
DDR_VREF	SDRAM Reference Voltage: external reference voltage input for each DQ, DQS. Internal VREF is also supported.	I	Analog
DDR_PREF	Reserved.	O	N/A

NOTE: Please refer to appropriate platform design guide for connections recommendations.

Table 2-7. Reset and Miscellaneous Signal

Signal Name	Description	Direction	Type
RSTINB	Reset In: When asserted, this signal will asynchronously reset the CPU logic. The signal is connected to the PCIRST# output of the Intel NM10 Express Chipset. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3-V tolerant.	I	HVCMOS
PWROK	Power OK: When asserted, PWROK is an indication to the CPU that core power has been stable for at least 10us. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3V tolerant.	I	HVCMOS
DDR3_DRAM_PWROK	DDR3 power good monitor. Driven by platform logic for DDR3. Reserved for DDR2 designs	I	CMOS-1.5
DDR3_DRAMRST#	DDR3 DRAM reset. Reset signal from IMC to DRAM devices. One for all SO-DIMMs. Used only in DDR3 mode. Reserved for DDR2 designs.	O	SSTL-1.5
RSVD_*	Reserved. Must be left unconnected on the board. Intel does not recommend a test point on the board for this ball.	NC	
RSVD_NCTF_*	Reserved/non-critical to function. Pin for package mechanical reliability. A test point may be placed on the board for this ball.	I/O	
RSVD_TP_*	Reserved-test-point. A test point may be placed on the board for this ball.	I/O	
XDP_RSVD_[17:0]	Reserved XDP debug signals.		

NOTE: RSVD_* numbering needs to be observed for BSDL testing purposes.



2.3 DMI - Direct Media Interface

Table 2-8. DMI - Processor to Intel NM10 Express Chipset Serial Interface

Signal Name	Description	Direction	Type
DMI_RXP[3:0] DMI_RXN[3:0]	DMI input from Intel NM10 Express Chipset: Direct Media Interface receive differential pair.	I	DMI
DMI_TXP[3:0] DMI_TXN[3:0]	DMI output to Intel NM10 Express Chipset: Direct Media Interface transmit differential pair.	O	DMI
EXP_ICOMPI	PCI Express-G Input Current Compensation. Connect to a 50-Ohm resistor to ground. EXP_ICOMPI and EXP_RCOMPO are shorted off-die and should be connected to the same 50-Ohm resistor.	I	Analog
EXP_RCOMPO	PCI-Express-G Resistance Compensation. Connect to a 50-Ohm resistor to ground. EXP_ICOMPI and EXP_RCOMPO are shorted off-die and should be connected to the same 50-Ohm resistor.	I/O	Analog
EXP_RBIAS	PCI-Express CML Bias control: Connect to a 750-Ohm resistor to ground.	I/O	Analog

2.4 PLL Signals

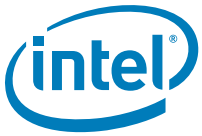
Table 2-9. PLL Signals

Signal Name	Description	Direction	Type
BCLKP[0] BCLKN[0]	Differential Core Clock In	I	Diff Clk CMOS
HPL_CLKINP HPL_CLKINN	Differential Host Clock In	I	Diff Clk CMOS
EXP_CLKINP EXP_CLKINN	Differential DMI Clock In	I	Diff Clk CMOS
DPL_REFCLKINN DPL_REFCLKINP	Differential PLL Clock In	I	Diff Clk CMOS
DPL_REFSSCLKINN DPL_REFSSCLKINP	Differential Spread Spectrum Clock In	I	Diff Clk CMOS

2.5 Analog Display Signals

Table 2-10.Analog Display Signals

Signal Name	Description	Direction	Type
CRT_RED	RED Analog Video Output: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ohm routing impedance but the terminating resistor to ground will be 75 Ohms (e.g., 75 Ohm resistor on the board, in parallel with 75 Ohm CRT load).	O	Analog
CRT_GREEN	GREEN Analog Video Output: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ohm routing impedance but the terminating resistor to ground will be 75 Ohms (e.g., 75 Ohm resistor on the board, in parallel with 75 Ohm CRT load).	O	Analog
CRT_BLUE	BLUE Analog Video Output: This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 Ohm routing impedance but the terminating resistor to ground will be 75 Ohms (e.g., 75 Ohm resistor on the board, in parallel with 75 Ohm CRT load).	O	Analog
CRT_IRTN	Current return path. Shorted to ground	O	Analog
DAC_IREF	Resistor Set: Set point resistor for the internal color palette DAC. A 665 Ohm 0.5% resistor is required between DAC_IREF and motherboard ground.	I/O	Analog
CRT_HSYNC	CRT Horizontal Synchronization: This signal is used as the vertical sync (polarity is programmable) or “sync interval”. 3.3V output.	O	HVCMOS
CRT_VSYNC	CRT Vertical Synchronization: This signal is used as the vertical sync (polarity is programmable). 3.3V output.	O	HVCMOS
CRT_DDC_CLK	Monitor Control Clock	I/O	COD
CRT_DDC_DATA	Monitor Control Data	I/O	COD



2.6 LVDS Signals

Table 2-11.LVDS Signals

Signal Name	Description	Direction	Type
LVD_A_DATAP[2:0]	Differential data output - positive	O	LVDS
LVD_A_DATAN[2:0]	Differential data output - negative	O	LVDS
LVD_A_CLKP	Differential clock output - positive	O	LVDS
LVD_A_CLKN	Differential clock output - negative	O	LVDS
LVD_IBG	LVDS Reference Current. Need 2.37 kOhms pull-down resistor	I/O	Ref
LVD_VBG	Reserved. No connect.	O	Analog
LVD_VREFH	Reserved. Can be connected to V_{SS} or left as No Connect.	I	Ref
LVD_VREFL	Reserved. Can be connected to V_{SS} or left as No Connect.	I	Ref
LVDD_EN	LVDS panel power enable: Panel power control enable control. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.	O	HVCMOS
LBKLT_EN	LVDS backlight enable: Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry. Note: The accuracy of the PWM duty cycle of LBKLT_CTL signal for any given value will be within ±20 ns.	O	HVCMOS
LBKLT_CTL	Panel backlight brightness control: Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM clock input signal.	O	HVCMOS
LCTLA_CLK	I2C based control signal (clock) for External SSC clock chip control - optional	I/O	COD
LCTLB_DATA	I2C based control signal (data) for External SSC clock chip control - optional	I/O	COD
LDDC_CLK	Display Data Channel clock	I/O	COD
LDDC_DATA	Display Data Channel data	I/O	COD

2.7 JTAG / ITP Signals

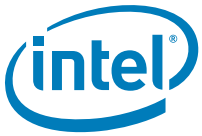
Table 2-12.JTAG / ITP Signals

Signal Name	Description	Direction	Type
TCK	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).	I	TAP OD
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I	TAP OD
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	O	TAP OD
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.	I	TAP OD
TRST#	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Refer to the Nehalem Processor Debug Port Design Guide for complete implementation details.	I	TAP OD

2.8 Error and Thermal Protection

Table 2-13.Error and Thermal Protection

Signal Name	Description	Direction	Type
PROCHOT#	PROCHOT# will go active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operation temperature Output: This indicates that the processor (core0 and core1) Thermal Control Circuit has been activated, if enabled. Input: This signal can also be driven to the processor to activate the Thermal Control Circuit in core0 and core1. This signal does not have on-die termination and must be terminated on the system board, and 60 Ohm resistor to Vcc.	I/O	I: CMOS O: OD
THERMTRIP#	Thermal Trip: The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125 C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O	Open Drain



2.9 Processor Core Power Signals

Table 2-14.Processor Core Power Signals

Signal Name	Description	Direction	Type
VCC	Processor core power supply. The voltage supplied to these pins is determined by the VID pins.		PWR
VCC_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.		Analog
VID[6:0]	VID[6:0] (Voltage ID) are used to support automatic selection of power supply voltages (VCC). Intel Atom Processor D400 and D500 Series support only a single fused voltage. Refer to the appropriate platform design guide or Voltage Regulator-Down (VRD) 11.0 Design Guidelines for more information. The voltage supply for these signals must be valid before the VR can supply VCC to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals become valid. The VR must supply the voltage that is requested by the signals, or disable itself.	I/O	CMOS
VSS_SENSE	VCC_SENSE and VSS_SENSE provide an isolated, low impedance connection to the processor core voltage and ground. They can be used to sense or measure voltage near the silicon.		Analog
VCCA	Processor PLL power supply.		PWR

2.10 Graphics, DMI and Memory Core Power Signals

Table 2-15.Power Signals

Signal Name	Description	Direction	Type
VCCP	LGI power supply	1.05	PWR
VCCGFX	Graphics core power supply	1.05	PWR
VCCSM	DDR power supply	1.8	PWR
VCCA_DMI	DMI power supply	1.05	PWR
VCCACRTDAC	CRT power supply	1.8	PWR
VCC_GIO	GPIO power supply	3.3	PWR
VCC_LGI_VID	LGIO power supply	1.05	PWR
VCCA_DDR	DDR power supply	1.05	PWR
VCCD_HMPLL	HMPLL power supply	1.05	PWR
VCCDLVD	LVDS power supply	1.8	PWR
VCCALVD	LVDS power supply	1.8	PWR

Table 2-15.Power Signals

Signal Name	Description	Direction	Type
VCCSFR_DMIHMPLL	DMI, HPLL, MPLL power supply	1.8	PWR
VCCACK_DDR	DDR power supply	1.05	PWR
VCCD_AB_DPL	DPLL power supply	1.05	PWR
VCCSFR_AB_DPL	DPLL power supply	1.8	PWR
VCCRING_EAST	DAC, GIO, LVDS power supply	1.05	PWR
VCCRING_WEST	LGIO power supply	1.05	PWR
VCCCK_DDR	DDR clock power supply	1.8	PWR

2.11 Ground

Table 2-16.Ground

Signal Name	Description	Direction	Type
VSS	VSS are the ground pins for the processor and should be connected to the system ground plane.		GND

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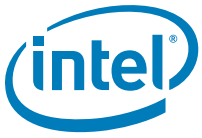


3 Functional Description

3.1 System Memory Controller

The system memory controller supports DDR2 and DDR3 (SO-DIMM only protocols) with one 64 bit wide channel accessing two DIMMs. The controller supports a maximum of two non-ECC DDR2 DIMMs or two un-buffered DIMMs, single or double sided; thus allowing up to four device ranks. Intel® Fast Memory Access (Intel® FMA) is supported.

3.1.1 System Memory Organization Modes

The system memory controller supports only one memory organization mode: single channel. In this mode, all memory cycles are directed to a single channel.

3.1.2 System Memory Technology Supported

3.1.2.1 DDR2

The system memory controller supports the following DDR2 Data Transfer Rates, DIMM Modules and DRAM Device Technologies:

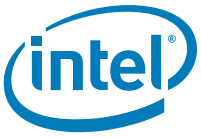
- DDR2 Data Transfer Rates: 667 (PC 5300), non-ECC
  - Rawcard C = single sided x16
  - Rawcard D = single sided x8
  - Rawcard E = double sided x8
- DDR2 Data Transfer Rates: 800 (PC 6400), non-ECC
  - Rawcard C = single sided x16
  - Rawcard D= single sided x8
  - Rawcard E = double sided x8

“Single sided” above is a logical term referring to the number of Chip Selects attached to the DIMM. A real DIMM may put the components on both sides of the substrate, but be logically indistinguishable from single sided DIMM if all components on the DIMM are attached to the same Chip Select signal.

- x8 means that each component has 8 data lines.
- x16 means that each component has 16 data lines.

There is no support for DIMMs with different technologies or capacities on opposite sides of the same DIMM. If one side of a DIMM is populated, the other side is either identical or empty.

There is no support for 4Gb and 8Gb technology.



Supported components for DDR2 at 667 (PC5300) and 800 (PC6400) include:

- 256Mb technology
  - — 32M cells x8 data bits/cell

    1K columns

    4 banks

    8K rows

    each component has a 1KB page

    one DIMM has 8 components resulting in an 8KB page

    the capacity of one rank is 256MB
  - — 16M cells x16 data bits/cell

    512 column

    4 banks

    8K rows

    each component has 1KB page

    one DIMM has 4 components resulting in a 4KB page

    the capacity of one rank is 128MB
- 512Mb technology
  - — 64M cells x8 data bits/cell

    1K columns

    4 banks

    16K rows

    each component has a 1KB page

    one DIMM has 8 components resulting in a 8KB page

    the capacity of one rank is 512MB
  - — 32M cells x16 data bits/cell

    1K columns

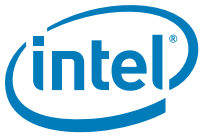
    8 banks

    16K rows

    each component has a 1KB page

    one DIMM has 8 components resulting in a 8KB page

    the capacity of one rank is 256MB



- 1Gb technology
  - — 128M cells x8 data bits/cell
    - 1K columns
    - 8 banks
    - 16K rows
    - each component has 1KB page
    - one DIMM has 8 components resulting in a 8KB page
    - the capacity of one rank is 1GB
  - — 64M cells x16 data bits/cell
    - 1K columns
    - 8 banks
    - 8K rows
    - each component has a 2KB page
    - one DIMM has 4 components resulting in an 8KB page
    - the capacity of one rank is 512MB
- 2Gb technology
  - — 256M cells x8 data bits/cell
    - 1K columns
    - 8 banks
    - 16K rows
    - each component has a 1KB page
    - one DIMM has 8 components resulting in a 8KB page
    - the capacity of one rank is 2GB
  - — 128M cells x16 data bits/cell
    - 1K columns
    - 8 banks
    - 8K rows
    - each component has a 2KB page
    - one DIMM has 4 components resulting in a 8KB page
    - the capacity of one rank is 1GB

3.1.2.2 DDR3 (SO-DIMM Only)

The system memory controller supports the following DDR3 data transfer rates, SO-DIMM modules and DRAM device technologies:

- DDR3 data transfer rate of 800 MT/s
- DDR3 SO-DIMM modules (unbuffered, non-ECC)
  - — Raw card A = 2 ranks of x16 SDRAMs (double sided)
  - — Raw card B = 1 rank of x8 SDRAM (double sided)

Note: x16/x8 means that each SDRAM component has 16/8 data lines.

- — DDR3 DRAM Device Technology:

  Standard 1-Gb and 2-Gb technologies and addressing are supported for x16/x8 devices. There is no support for SO-DIMMs with different technologies or capacities on opposite sides of the same SO-DIMM. If one side of a SO-DIMM is populated, the other side is either identical or empty.

- — Supported DDR3 SO-DIMM module configurations

Raw Card Type	DIMM Capacity	DRAM Device Tech.	DRAM Organization	# of DRAM Devices	# of Ranks	# of Banks
A	1 GB	1 Gb	64 M x16	8	2	8
A	2 GB	2 Gb	128 M x16	8	2	8
B	1 GB	1 Gb	128 M x8	8	1	8
B	2 GB	2 Gb	256 M x8	8	1	8

3.1.3 Rules for Populating DIMM Slots

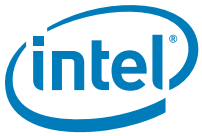
The frequency of system memory will be the lowest frequency of all DIMMs in the system, as determined through the SPD registers on the DIMMs. Timing parameters [CAS latency (or CL + AL for DDR2), tRAS, tRCD, tRP] must be programmed to match within a channel.

In single channel mode, any DIMM slot within the channel may be populated in any order. To take advantage of enhanced addressing, it is best to populate both DIMM slots with identical DIMMs.

3.2 Graphics Processing Unit

This section details the integrated graphics engines (3D, 2D and video), 3D pipeline, and the respective capabilities.

The CPU's graphics processing unit (GPU) contains several types of components. The major components in the GPU are the engines, planes, pipes and ports. The GPU has a 3D/2D instruction processing unit to control the 3D and 2D engines respectively. The



CPU's 3D and 2D engines are fed with data through the memory controller. The outputs of the engines are surfaces sent to the memory, which are then retrieved and processed by the CPU planes.

3.2.1 3D Graphics Pipeline

This CPU is the next step in the evolution of integrated graphics. In addition to running the graphics engine at 400 MHz, the GPU has two pixel pipelines.

The 3D graphics pipeline has a deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive. The 3D graphics pipeline is broken up into four major stages: geometry processing, setup (vertex processing), texture application and rasterization.

The graphics is optimized by using the processor for advance software based transform and lighting (geometry processing) as defined by DirectX*. The other three stages of 3D processing are handled on the GPU. The setup stage is responsible for vertex processing - converting vertices to pixels. The texture application stage applies textures to pixels. The rasterization engine takes textured pixels and applies lighting and other environment affects to produce the final pixel value. From the rasterization stage, the final pixel value is written to the frame buffer in memory so it can be displayed.

3.2.1.1 3D Engine

The 3D engine on the GPU has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitive or portions of the same primitive. The GPU supports Perspective-Correct Texture Mapping, Multi-textures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, ground shading, Alpha-blending, Vertex and Per Pixel Fog and Z/W Buffering.

The 3D Pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the setup engine, scan converter, texture pipeline, and raster pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

3.2.1.2 Texture Engine

The GPU allows an image, pattern, or video to be placed on the surface of the 3D polygon. The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear, bilinear interoplation), and YUV-to-RGB conversions.

3.2.2 Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in Hardware. The CGPU engine includes a number of encompassments over the previous generation capabilities, which have been listed above.

3.2.3 2D Engine

3.2.4 Analog Display Port Characteristics

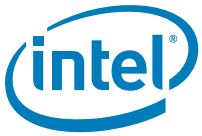
The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

Table 3-17.Analog Port Characteristics

Signal	Port Characteristics	Support
RGB	Voltage Range	0.7 Vp-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	3.3V
	Enable/Disable	Port control
	Polarity Adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	External buffered to 5V
	Control	Through GPIO interface

3.2.4.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. CPU's integrated 350 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 60 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.



3.2.4.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

3.2.4.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

3.2.4.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug- and-play systems to be realized. Support for DDC 1 and DDC 2 is implemented. The CPU uses the CRT_DDC_CLK and CRT_DDC_DATA signals to communicate with the analog monitor. The CPU will generate these signals at 3.3V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The CPU implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 100 kHz.

3.2.5 Multiple Display Configurations

Microsoft Windows* 2000, Windows* XP, and Windows* Vista operating systems provide support for multi-monitor display. The CPU supports Dual Display Clone and Extended Desktop (LVDS + VGA).

3.3 Thermal Sensor

There are several registers that need to be configured to support the uncore thermal sensor functionality and SMI# generation. Customers must enable the Catastrophic Trip Point as protection for the CPU. If the Catastrophic Trip Point is crossed, then the CPU will instantly turn off all clocks inside the device. Customers may optionally enable the Hot Trip Point to generate SMI#. Customers will be required to then write their own SMI# handler in BIOS that will speed up the CPU (or system) fan to cool the part.

3.3.1 PCI Device 0, Function 0

The SMICMD register requires that a bit be set to generate an SMI# when the Hot Trip point is crossed. The ERRSTS register can be inspected for the SMI alert.

Address	Register Symbol	Register Name	Default Value	Access
C8-C9	ERRST	Error Status	0000h	RWC/S, RO
CC-CDh	SMICMD	SMI Command	0000h	RO, R/W

3.4 Power Management

The CPU uncore has many permutations of possibly concurrently operating modes. Care should be taken (Hardware and Software) to disable unused sections of the silicon when this can be done with sufficiently low performance impact. Refer to the *ACPI Specification, Rev3.0* for an overview of the system power states mentioned in this section.

3.4.1 Main Memory Power Management

Table 3-18.Targeted Memory State Conditions

Mode	Memory State with Internal Graphics
C0, C1	Dynamic memory rank power down based on idle conditions
S3	Self Refresh Mode
S4	Memory power down (contents lost)

This section details the support provided by the CPU uncore corresponding to the various processor/display/system ACPI states.

Table 3-19.Platform System States

State	Description
G0/S0	Full On
G1/S3-cold	Suspend to RAM (STR). Context saved to memory (S3-Hot is not supported)
G1/S4	Suspend to Disk (STD). All power lost (except wakeup on Intel NM10 Express Chipset).
G2/S5	Soft off. All power lost (except wake on Intel NM10 Express Chipset). Total reboot.
G3	Hard off. All power (AC) removed from system.

Table 3-20.Processor Power States

State	Description
C0	Full On
C1	Auto Halt

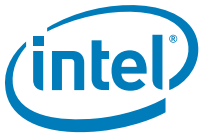


Table 3-21.Graphics Processing Unit

State	Description
D0	Display active
D3	Power-off display

3.4.2 Interface Power States Supported

Table 3-22.Main Memory States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge power down	CKE deasserted (not self-refresh) with all banks closed.
Active power down	CKE deasserted (not self-refresh) with minimum one bank active.

3.4.3 State Combinations

Table 3-23.G, S and C State Combinations

Global (G) state	Sleep (S) state	Processor (C) state	Processor state	System clocks	Description
G0	S0	C0	Full on	On	Full on
G0	S0	C1	Auto-Halt	On	Auto Halt
G1	S3	power-off	-	Off, except RTC	Suspend to RAM
G1	S4	power-off	-	Off, except RTC	Suspend to Disk
G1	S5	power-off	-	Off, except RTC	Soft off
G3	NA	power-off	-	Power-off	Hard off

Table 3-24.D, S and C State Combinations

Display (D)	Sleep State (S)	CPU State (C)	Description
D0	S0	C0	Full on, displaying
D0	S0	C1	Auto-Halt, displaying
D3	S0	C0-1	Not displaying
D3	S3	---	Not displaying
D3	S4	---	Not displaying

3.4.4 System Suspend States

This group is the system states that are at a lower power level than S0. This represents long wakeup latency but lower power states that are used as suspend states.

3.4.4.1 S1 - Power and clock on Standby to RAM

Not supported.

3.4.4.2 S3 - Standby to RAM

Supported.

3.4.4.3 S4/S5 - Standby to Disk/Soft-Off

Supported.

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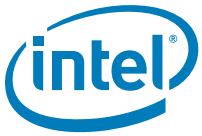


4 Electrical Specifications

This chapter contains signal group descriptions, absolute maximum ratings, voltage identification and power sequencing. The chapter also includes DC and AC specifications, including timing diagrams.

4.1 Power and Ground Balls

The processor has V_{CC*} and V_{SS} (ground) inputs for on-chip power distribution. All power balls must be connected to their respective processor power planes, while all V_{SS} balls must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The V_{CC} balls must be supplied with the voltage determined by the processor Voltage IDentification (VID) signals.

4.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full-power states. This may cause voltages on power planes to sag below their minimum values, if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand (for example, coming out of an idle condition). Similarly, capacitors act as a storage well for current when entering an idle condition from a running condition. To keep voltages within specification, output decoupling must be properly designed.

Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications. Failure to do so can result in timing violations or reduced lifetime of the processor.

4.2.1 Voltage Rail Decoupling

The voltage regulator solution needs to provide:

- bulk capacitance with low effective series resistance (ESR).
- a low path impedance from the regulator to the CPU.
- bulk decoupling to compensate for large current swings generated during power-on, or low-power idle state entry/exit.

The power delivery solution must ensure that the voltage and current specifications are met, as defined in Table 4-29. For further information regarding power delivery, decoupling, and layout guidelines refer to the appropriate platform design guide.

4.3 Processor Clocking

- BCLKP, BCLKN, HPL_CLKINP, HPL_CLKINN, EXP_CLKINP, EXP_CLKINN, DPL_REFCLKINP, DPL_REFCLKINN

The processor utilizes differential clocks to generate the processor core(s) and uncore operating frequencies, memory controller frequency, and other internal clocks. The processor core frequency is determined by multiplying the processor core ratio by 200 MHz. Clock multiplying within the processor is provided by an internal phase locked loop (PLL), which requires a constant frequency input, with exceptions for Spread Spectrum Clocking (SSC). PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 4-29 for DC specifications and to the platform design guide for decoupling and routing guidelines.

4.4 Voltage Identification (VID)

The VID specification for the processor is defined by the *Voltage Regulator Down (VRD) 11.0 Design Guidelines*. The processor uses seven voltage identification signals, VID[6:0], to support automatic selection of voltages. Table 4-26 specifies the voltage level corresponding to the state of VID[6:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. Do take note of the VID pin mapping of the processor to the VR chip. If the processor is not soldered on board (VID[6:0] = 1111111), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. Refer to the *Voltage Regulator Down (VRD) 11.0 Design Guidelines* for further details.

VID signals are CMOS push/pull drivers. Refer to Table 4-33 for the DC specifications for these signals. Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different VID settings.

The VR utilized must be capable of regulating its output to the value defined by the VID values issued. DC specifications are included in Table 4-28 and Table 4-29.

VRD11.0 has 8 VID pins (VID[7:0]) compared to 7 VID pins for the processor. VRD11.0 VID[n] pin should be connected to processor VID[n-1] pin. VRD11.0 VID[0] pin should be tied to Vss. Refer Table 4-27 for mapping details.

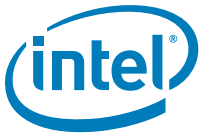


Table 4-25.Voltage Identification Definition

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCC (V)
0	1	0	0	0	0	1	1.2000
0	1	0	0	0	1	0	1.1875
0	1	0	0	0	1	1	1.1750
0	1	0	0	1	0	0	1.1625
0	1	0	0	1	0	1	1.1500
0	1	0	0	1	1	0	1.1375
0	1	0	0	1	1	1	1.1250
0	1	0	1	0	0	0	1.1125
0	1	0	1	0	0	1	1.1000
0	1	0	1	0	1	0	1.0875
0	1	0	1	0	1	1	1.0750
0	1	0	1	1	0	0	1.0625
0	1	0	1	1	0	1	1.0500
0	1	0	1	1	1	0	1.0375
0	1	0	1	1	1	1	1.0250
0	1	1	0	0	0	0	1.0125
0	1	1	0	0	0	1	1.0000
0	1	1	0	0	1	0	0.9875
0	1	1	0	0	1	1	0.9750
0	1	1	0	1	0	0	0.9625
0	1	1	0	1	0	1	0.9500
0	1	1	0	1	1	0	0.9375
0	1	1	0	1	1	1	0.9250
0	1	1	1	0	0	0	0.9125
0	1	1	1	0	0	1	0.9000
0	1	1	1	0	1	0	0.8875
0	1	1	1	0	1	1	0.8750
0	1	1	1	1	0	0	0.8625
0	1	1	1	1	0	1	0.8500
0	1	1	1	1	1	0	0.8375
0	1	1	1	1	1	1	0.8250
1	0	0	0	0	0	0	0.8125
1	0	0	0	0	0	1	0.8000
1	0	0	0	0	1	0	0.7875
1	0	0	0	0	1	1	0.7750
1	0	0	0	1	0	0	0.7625

Table 4-25.Voltage Identification Definition

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCC (V)
1	0	0	0	1	0	1	0.7500
1	0	0	0	1	1	0	0.7375
1	0	0	0	1	1	1	0.7250
1	0	0	1	0	0	0	0.7125
1	0	0	1	0	0	1	0.7000

Table 4-26.VID Pin Mapping

Processor VID pin	map to VRD11 VID pin
6	7
5	6
4	5
3	4
2	3
1	2
0	1
	0 (tie to ground)

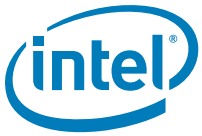
4.5 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 degree Celsius (maximum), or the THERMTRIP# signal is asserted, the Vcc supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to the thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

4.6 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left un-connected



Arbitrary connection of these signals to V_{CC}*, V_{SS}*, or to any other signal (including each other) may result in component malfunction. See Chapter 8 for a land listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines.

4.7 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Chapter 2. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR2 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

All Control Sideband Asynchronous signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 4.10 for the DC and AC specifications.

4.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

4.9 Absolute Maximum and Minimum Ratings

Table 4-28 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 4-27.Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1, 2, 7]
V_{CC}, V_{CCP}	Processor Core, LGI voltages with respect to V_{SS}	-0.3	1.45	V	6
V_{CCSM}, V_{CCCK_DDR}	Processor DDR voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CCA}	Processor PLL voltage with respect to V_{SS}	-0.3	1.45	V	
V_{CCGFX}	Processor GFX voltage with respect to V_{SS}	-0.3	1.55	V	
V_{CCDLVD}, V_{CCALVD}	Processor LVDS voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CCA_DDR}, V_{CCACK_DDR}	Processor DDR PLL voltage with respect to V_{SS}	-0.3	1.45	V	
V_{CCRING_EAST}, V_{CCRING_WEST}, $V_{CC\_LGI\_VID}$,	Processor DAC, GIO, LVDS, & LGIO voltage with respect to V_{SS}	-0.3	1.45	V	
$V_{CCD\_AB\_DPL}$, V_{CCD_HMPLL}	Processor DPLL, & HMPLL voltage with respect to V_{SS}	-0.3	1.45	V	
$V_{CCSFR\_AB\_DPL}$	Processor SFR DPLL voltage with respect to V_{SS}	-0.3	2.25	V	
$V_{CCACRTDAC}$	Processor CRT voltage with respect to V_{SS}	-0.3	2.25	V	
$V_{CCSFR\_DMIHMPLL}$	Processor DMI SFR voltage with respect to V_{SS}	-0.3	2.25	V	
V_{CC_GIO}	Processor GIO voltage with respect to V_{SS}	3.135	3.465	V	
$T_{STORAGE}$	Storage temperature	-40	85	°C	3, 4, 5
VinAGTL+	AGTL+ Buffer DC Input Voltage with Respect to V_{SS},	-0.1	1.45	V	
VinAsynch_CMOS	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.45	V	

NOTES:

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Chapter 5. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.
5. Failure to adhere to this specification can affect the long-term reliability of the processor.
6. V_{CC} is a VID based rail.1
7. These are pre-silicon estimates and are subject to change

Possible damage to the processor may occur if the processor temperature exceeds 150 °C. Intel does not ensure functionality for parts that have exceeded temperature above 150 °C due to specification violation.

4.10 DC Specifications

This section lists the DC specifications for the processor and are valid only while meeting the thermal specifications (as specified in *Intel® Atom™ Processor D400 and D500 Series Thermal Mechanical Design Guidelines*, #322856-001), clock frequency, and input voltages. Table 4-29 lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

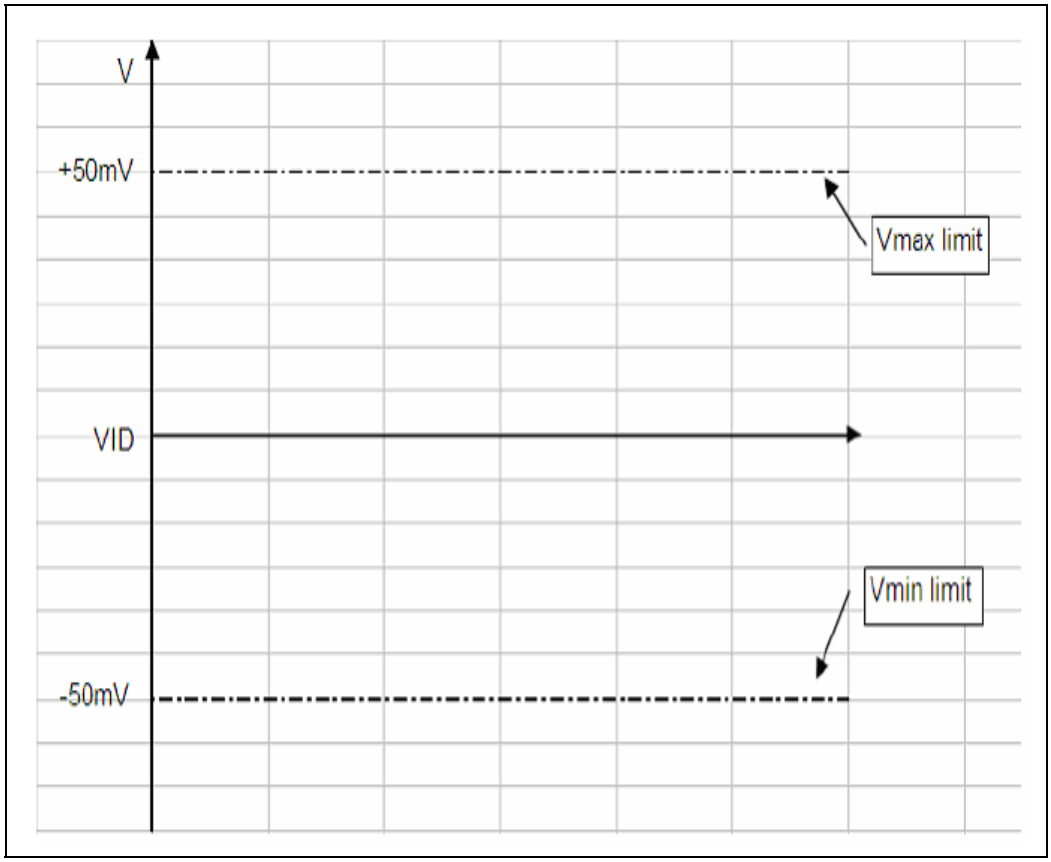
4.10.1 Flexible Motherboard Guidelines (FMB)

This is not applicable for Intel Atom Processor D400 and D500 Series on Pinetrail-D platform.

4.10.2 Voltage and Current Specifications

The V_{CC} tolerance for processor core should be ±50mV, inclusive of ripple, VR tolerance (AC and DC) and transient (droop and overshoot). Since processor is soldered down with no loadline and no dynamic VID, some legacy parameters are not present.

Figure 4-2. V_{CC} Tolerance Band

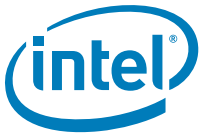


- Parameters not present for V_{CC}:
  - No socket loadline slope - SKT_LL
  - No socket loadline tolerance band
  - No maximum overshoot above VID (OS_AMP)
  - No maximum overshoot time duration above VID (OS_TIME)
  - No peak-to-peak ripple amplitude (RIPPLE)
  - No thermal compensation voltage drift (THERMAL_DRIFT)
  - No maximum DC test (current I_DC_MAX)
  - No minimum DC test (current I_DC_MIN)
- Parameters present for V_{CC}:
  - Tolerance band (TOB) of ±50 mV

Table 4-28.Processor Core Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
VID	VID Range	0.8		1.175	V	
V_{CC}	V_{CC} for processor core	See Table 4-26 and Figure 4-2 0.800 - 1.175			V	2, 3
$V_{CC,BOOT}$	Default V_{CC} voltage for initial power up	1.045	1.1	1.26	V	
I_{CC}	I_{CC} for processor core Dual Core Single Core			 10.8 5.4	A	
I_{AH}	I_{CC} Auto-Halt Dual Core Single Core			 6.5 3.25	A	
$dI_{CC/DT}$	V_{CC} power supply current slew rate at the processor pin package Dual Core Single Core			 5 2.5	A/µs	

NOTES:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Please note this differs from the VID employed by the processor during a power management event.
3. These are pre-silicon estimates and are subject to change.



The I/O buffer supply voltage should be measured at the processor package pins. The tolerances shown in Table 4-29 are inclusive of all noise from DC up to 20 MHz. The voltage rails should be measured with a bandwidth limited oscilloscope with a roll-off of 3 dB/decade above 20 MHz under all operating conditions. Table 4-29 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltage rails that are connected to a filter, they should be measured at the input of the filter. If the recommended platform decoupling guidelines cannot be met, the system designer will have to make trade-offs between the voltage regulator out DC tolerance and the decoupling performances of the capacitor network to stay within the voltage tolerances listed below.

Table 4-29.Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note 1
V_{CCA}	Processor Core analog supply voltage (DC + AC specification)	1.425	1.5	1.575	V	
I_{CCA}	Processor Core analog supply current Single Core Dual Core			 0.075 0.15	A	
V_{CCGFX}	GFX supply voltage	0.9975	1.05	1.1025	V	
I_{CCGFX}	GFX supply current			3.4A	A	
V_{CCDLVD}, V_{CCALVD}	LVDS supply voltage	1.71	1.8	1.89	V	
I_{CCDLVD}, I_{CCALVD}	LVDS supply current			0.08	A	
V_{CCA_DMI}	DMI analog supply voltage	0.9975	1.05	1.1025	V	
V_{CCD_HMPLL}	HMPLL supply voltage	0.9975	1.05	1.1025		
I_{CCA_DMI}, I_{CCD_HMPLL}	DMI analog and HMPLL supply current			0.55	A	
$V_{CCSFR\_DMIHMPLL}$, $V_{CCSFR\_AB\_DPL}$	DMI & HMPLL & DPLL SFR supply voltage	1.71	1.8	1.89	V	
$I_{CCSFR\_DMIHMPLL}$, $I_{CCSFR\_AB\_DPL}$	DMI & HMPLL SFR supply current			0.1721	A	
V_{CCA_DDR}, V_{CCACK_DDR}	DDR analog supply voltage	0.9975	1.05	1.1025	V	
I_{CCA_DDR}, I_{CCACK_DDR}	DDR analog supply current			1.32	A	
V_{CCSM}, V_{CCCK_DDR}	DDR supply voltage DDR2 DDR3	 1.71 1.425	 1.8 1.5	 1.89 1.575	V	
I_{CC_DDR}, I_{CCCK_DDR}	DDR supply current			2.270	A	
V_{CCRING_EAST}, V_{CCRING_WEST}, $V_{CC\_LGI\_VID}$, $V_{CCD\_AB\_DPL}$	DAC, GIO, LVDS, LGIO, HMPLL supply voltage	0.9975	1.05	1.1025	V	
I_{CCRING_EAST}, I_{CCRING_WES}	DAC, GIO, LVDS, LGIO supply current			0.24	A	
$I_{CCD\_AB\_DPL}$, $I_{CC\_LGI\_VID}$	LGIO, DPLL supply current			0.07	A	
V_{CC_GIO}	GIO supply voltage	3.135	3.3	3.465	V	

Table 4-29. Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note 1
I_{CC_GIO}	GIO supply current			0.015	A	
$V_{CCACRTDAC}$	CRT DAC supply voltage	1.71	1.8	1.89	V	
$I_{CCACRTDAC}$	Display CRT DAC supply current			0.144	A	

NOTE: Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.

4.10.3 DC Specifications

Platform reference voltages at the top of Table 4-29 are specified at DC only. V_{REF} measurements should be made with respect to the supply voltage.

4.10.3.1 Input Clock DC Specification

Table 4-30. Input Clocks (BCLK, HPL_CLKIN, DPL_REFCLKIN, EXP_CLKIN) Differential Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.30	0		V	
V_{IH}	Input High Voltage			1.15	V	
V_{CROSS}	Absolute crossing voltage	0.3		0.550	V	2,3
dV_{CROSS}	Range of crossing points			0.14	V	
C_{IN}	Input Capacitance	1.0		3.0	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. Crossing voltage defined as instantaneous voltage when rising edge of CLKN equalize CLKP. The crossing point must meet the absolute and relative crossing point specification simultaneously.

4.10.3.2 DDR2/DDR3 DC Specifications

Table 4-31. DDR2 Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1,9]
V_{IL}(DC)	Input Low Voltage			DDR_VREF - 0.2	V	2,4,10
V_{IH}(DC)	Input High Voltage	DDR_VREF + 0.2			V	3,10
V_{IL}(AC)	Input Low Voltage			DDR_VREF - 0.25	V	2,4,10
V_{IH}(AC)	Input High Voltage	DDR_VREF + 0.25			V	3,10

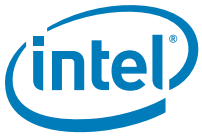


Table 4-31.DDR2 Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1,9]
V_{OL}	Output Low Voltage DDR2 DDR3			 0.27 0.20		9
V_{OH}	Output High Voltage DDR2 DDR3	 1.47 1.22			V	4,9
R_{ON}	DDR2 Clock Buffer On Resistance		22		Ω	5
I_{LI}	Input Leakage Current			10	µA	
V_{REF}	DDR Reference Voltage	V_{CCSM} / 2	V_{CCSM} / 2	V_{CCSM} / 2		8
$C_{I/O}$	DQ/DQS/DQSB DDR2 I/O Pin Capacitance	3.5	3.5	3.6	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCSM}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance. Refer to processor *I/O Buffer Models* for I/V characteristics.
6. The minimum and maximum values for these signals are programmable by BIOS
7. DDR2 values are pre-silicon estimations and subject to change.
8. V_{CCSM} varies with typical/min/max cases. Refer Table 4-29 for details.
9. Determined with 2x Buffer Strength Settings into a 50 to 0.5x VCCSM test load.
10. DDR_VREF could either be from external or internal reference voltage.

4.10.3.3 LGIO Signal DC Specification

Table 4-32.GTL Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{CCP}	I/O Voltage	1	1.05	1.1	V	
GTLREF	GTL Reference Voltage	2/3 V_{CCP}		2/3 V_{CCP}	V	6
R_{ODT}	On Die Termination	55		55	Ohm	10
V_{IH}	Input High Voltage	GTLREF + 0.1		V_{CCP} + 0.1	V	3,6
V_{IL}	Input Low Voltage	-0.1		GTLREF - 0.1	V	2,4
V_{OH}	Output High Voltage	V_{CCP} - 0.1		V_{CCP}	V	6
R_{TT}	Termination Resistance	20	55	70	Ohm	7
R_{ON}	Buffer on Resistance	14	25	40	Ω	5
I_{LI}	Input Leakage Current	-100		100	µA	8
C_{PAD}	Pad Capacitance	2.35	2.5	2.6	pF	9

NOTES: See notes in the next page

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. VIL is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. VIH and VOH may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at 0.31 * V_{CCP}. R_{ON}(min) = 0.4 * R_{TT}, R_{ON}(typ) = 0.455 * R_{TT}, R_{ON}(max) = 0.51 * R_{TT}. R_{TT} typical value of 55 Ohm is used for R_{ON} typ/min/max calculations.
6. GTLREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at VOL of the AGTL+ output driver. Measured at 0.31 * V_{CCP}. R_{TT} is connected to V_{CCP} on die. Refer to processor I/O Buffer Models for I/V characteristics.
8. Specified with on-die R_{ON} and R_{TT} are turned off. Vin between 0 and V_{CCP}.
9. C_{PAD} includes die capacitance only. No package parasitic are included.
10. On die termination resistance, measured at 0.33 * V_{CCP}.

Table 4-33.Legacy CMOS Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
V_{IH}	Input High Voltage	0.7 * V_{CCP}		V_{CCP} + 0.1	V	2
V_{IL}	Input Low Voltage	-0.1	0	0.3 * V_{CCP}	V	2, 3
V_{OH}	Output High Voltage	0.9 * V_{CCP}	V_{CCP}	V_{CCP} + 0.1	V	2, 4
V_{OL}	Output Low Voltage	-0.1		0.1 * V_{CCP}	V	2, 5
I_{LI}	Input Leakage Current	-100		100	uA	6
C_{PAD1}	Pad Capacitance	2.35	2.5	2.6	pF	7
C_{PAD2}	Pad Capacitance for CMOS Input	0.85	1.0	1.05	pF	8

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at Iout = -1.1mA.
5. Measured at Iout = 1.1mA.
6. For V_{IN} between 0V and V_{CCP}. Measured when driver is tri-stated.
7. C_{PAD1} includes die capacitance only for DPRSTP#, DPSLP#, BSEL[2:0], VID[6:0]. No package parasitic are included.
8. C_{PAD2} includes die capacitance for all other CMOS input signals. No package parasitics are included.

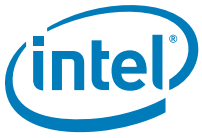


Table 4-34.Open Drain Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OH}	Output High Voltage	V_{CCP} - 5%		V_{CCP} + 5%	V	3
V_{OL}	Output Low Voltage	--		0.20	V	
I_{OL}	Output Low Current	16		60	mA	2
I_{LI}	Input Leakage Current	-200		200	uA	4
C_{PAD}	Pad Capacitance	1.8	2.1	2.6	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. Measured at 0.2V
3. VOH is determined by value of the external pull-up resistor to V_{CCP}. Refer to platform design guide for details.
4. For V_{IN} between 0V and V_{CCP}.
5. C_{PAD} includes die capacitance only. No package parasitic are included.

Table 4-35.PWROK and RSTIN# DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.3		0.8	V	2
V_{IH}	Input High Voltage	2.7		3.6	V	2
L_I	Input Leakage Current			10	uA	
C_{PAD1}	Pad Capacitance			1.5	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
3. With respect to PAD input.

Table 4-36.CPUPWRGOOD DC Specification

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-0.1	0.3 * V_{CCP}	V	
V_{IH}	Input High Voltage	0.7 * V_{CCP}	V_{CCP} + 0.1	V	2
V_{HYS}	Hysterisis of Schmitt Trigger Inputs	100	--	mV	
L_I	Input Current of Each I/O Pin	-10	10	uA	
C_I	Capacitance of Each I/O Pin	--	1.5	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. V_{IH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.

4.10.3.4 DDR3_DRAM_PWROK DC Specification

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	-	0.29	V	
V_{IH}	Input High Voltage	1.25	-	V	2
L_I	Input leakage	-	20	uA	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. V_{IH} may experience excursions above $V_{CCSM.}$. However, input signal drivers must comply with the signal quality specifications.

4.10.3.5 JTAG DC Specification

Table 4-37.TAP Signal Group DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
RPD_{GTL}	GTL mode pull-down impedance (JTAG mode)		25		Ohm	
V_{T-}	Input fall transition threshold voltage	0.54* V_{CCP}	-	0.66* V_{CCP}	V	2,4
V_{T+}	Input rise transition threshold voltage	0.74* V_{CCP}	-	0.86* V_{CCP}	V	1,3
I_{LI}	Input Leakage Current			50	uA	

NOTES:
1. Positive transitions must cross above VT+(max) to trigger input.
2. Negative transitions must cross below VT-(min) to trigger input.
3. Input low noise must not cross VT+(min).
4. Input high noise must not cross VT-(max).
5. Unless otherwise noted, all specifications in this table apply to all processor frequencies.

4.10.3.6 Display DC Specification

The Analog Video Signal DC Specifications are referred to the VESA Video Signal Standard, version 1 revision 2.

Table 4-38.CRT_DDC_DATA. CRT_DDC_CLK, LDDC_DATA, LDDC_CLK, LCTLA_CLK, and LCTLB_DATA DC Specification (Sheet 1 of 2)

Symbol	Parameter	Standard mode 100kbits/s		Units	Notes[1]
		Min	Max		
V_{IL}	Input Low Voltage	-0.5	0.3 V_{CCGIO}	V	
V_{IH}	Input High Voltage	0.7 V_{CCGIO}	0.5 + V_{CCGIO}	V	

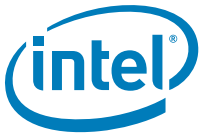


Table 4-38.CRT_DDC_DATA. CRT_DDC_CLK, LDDC_DATA, LDDC_CLK, LCTLA_CLK, and LCTLB_DATA DC Specification (Sheet 2 of 2)

Symbol	Parameter	Standard mode 100kbits/s		Units	Notes[1]
		Min	Max		
V_{OL1}	Output Low Voltage - 1	0	0.4	V	2
L_I	Input Leakage Current	-50	50	uA	3
C_I	Capacitance	--	10	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. 3mA sink current.
3. 0.1 V_{CCGIO} < Vi < 0.9 V_{CCGIO_MAX}

Table 4-39.CRT_HSYNC and CRT_VSYNC DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OH}	Output High Voltage	2.4	--	V_{CCGIO}	V	
V_{OL}	Output Low Voltage	0	--	0.5	V	
I_{OH}	Output High Current	--	--	8	mA	
I_{OL}	Output Low Current	--	--	8	mA	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.

Table 4-40.LVDS Interface DC Specification (functional operating range, V_{CCLVD} = 1.8V ±5%)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OD}	Differential Output Voltage	250	350	450	mV	2
ΔV_{OD}	Change in V_{OD} between Complementary Output States			50	mV	2
V_{OS}	Offset Voltage	1.125	1.25	1.375	V	2
ΔV_{OS}	Change in V_{OS} between Complementary Output States			50	mV	2
I_{OS}	Output Short Circuit Current		-3.5	-10	mA	2
I_{OZ}	Output TRI-STATE Current		±1	±10	uA	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. All LVDS active lanes must be terminated with 100 Ohm resistor for correct V_{OS} performance and measurement.

Table 4-41.LVDD_EN, LBKLT_EN and LBKLT_CTL DC Specification

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OL}	Output Low Voltage	0	--	0.4	V	2
V_{OH}	Output High Voltage	V_{CCGIO} - 0.5	--	V_{CCGIO}	V	2
I_L	Input Leakage	-50	--	50	uA	3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. These are pre-silicon estimates and are subject to change.
2. I_{OL} = 6 mA; I_{OH}= 2 mA.
3. For power and unpowered devices.

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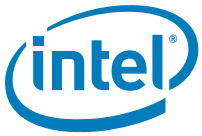

5 Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, overshoot and undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is important that the design ensures acceptable signal quality across all systematic variations encountered in volume manufacturing.

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6 Low Power Features

This chapter provides information on power management topics.

6.1 Low Power States

The low states supported by the processor are described in this section.

Table 6-42.System States

State	Description
G0/S0	Full On
G2/S5	Soft off. All power lost (except wakeup on Intel NM10 Express Chipset). Total reboot. (swh - I changed to ecpd_2#)
G3	Mechanical/hard off. All power (AC and battery) (AC and battery) removed from system.

Table 6-43.Processor Core Idle States

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.

6.1.1 Processor Core Low Power States

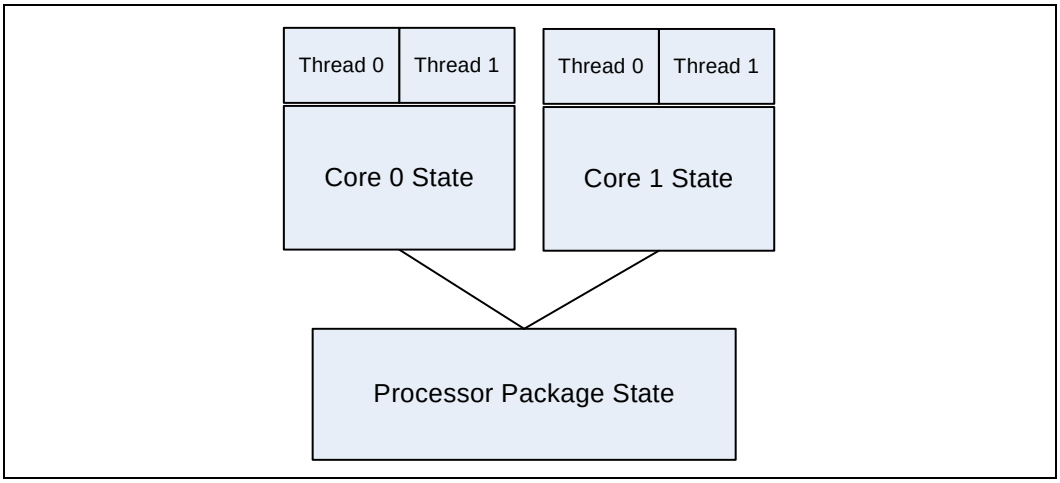
When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor core package level. Thread level C-states are available if Hyper-Threading Technology is enabled.

6.1.1.1 Clock Control and Low-Power States

The processor core supports low power states at the thread level and core/package level. Thread states (TCx) loosely correspond to ACPI processor core power states (Cx). A thread may independently enter TC1/AutoHALT, TC1/MWAIT but this does not always cause a power state transition. Only when both threads request a low-power state (TCx) greater than the current processor core state will a transition occur. The central power management logic ensures the entire processor core enters the new common processor core power state. Package states are states that require external intervention and typically map back to processor core power states. Package states for processor core include Normal (C0, C1) states.

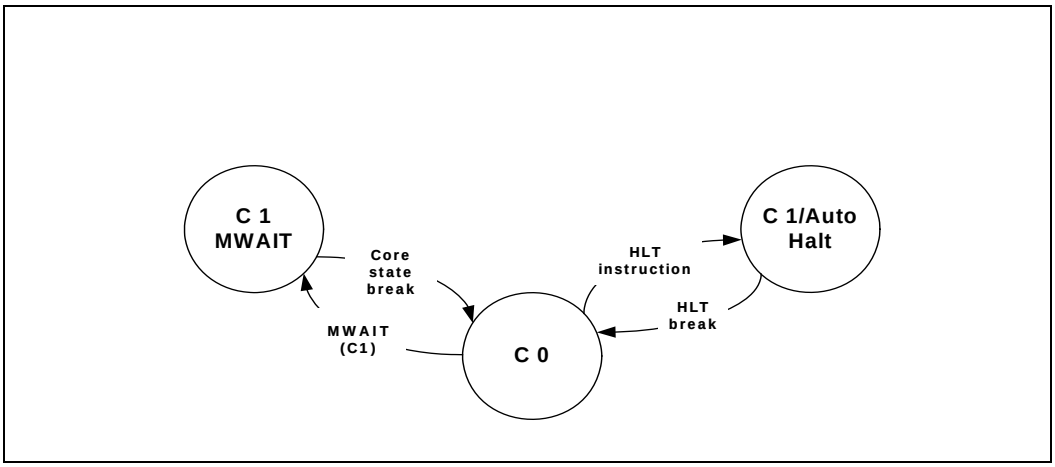
The processor core implements two software interfaces for requesting low power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor core's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor core and do not directly result in I/O reads on the processor core bus. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR by BIOS.

Figure 6-3. Idle Power Management Breakdown of the Processor Cores



Entry and exit of C-states at the thread and core level are show in the following figure.

Figure 6-4. Thread and Core C-state



NOTES:
1. halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, SMI# or APIC interrupt.

Table 6-44. Coordination of Thread Low-power States at the Package/Core Level

Thread1\Thread0	TC0	TC1
TC0	Normal (C0)	Normal (C0)
TC1	Normal (C0)	AutoHalt (C1)

6.1.2 Processor Core C-states Description

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (e.g., Thread0 requests C0 while thread1 requests C1, resulting in a core C0 state).
- A core transitions to C0 state when:
  - an interrupt occurs.
  - there is an access to the monitored address if the state was entered via an MWAIT instruction.
- For core C1, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- Any interrupt coming into the processor package may wake any core.

The following state descriptions assume that both threads are in common low power state. For cases when only 1 thread is in a low power state, no change in power state will occur.

6.1.2.1 Normal State (C0, C1)

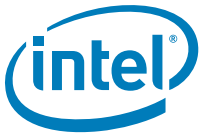
This is the normal operating state for the processor core. The processor core remains in the Normal state when the processor core is in the C0, C1/AutoHALT, or C1/MWAIT state. C0 is the active execution state.

6.1.2.2 C1/AutoHALT Power Down State

C1/AutoHALT is a low-power state entered when one thread executes the HALT instruction while the other is in the TC1 or greater thread state. The processor core will transition to the C0 state upon occurrence of SMI#, INIT#, LINT00/LINT10 (NMI, INTR), or internal bus interrupt messages. RSTINB will cause the processor core to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT power down state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

While in AutoHalt power down state, the processor core will process bus snoops. The processor core will enter an internal snoopable sub-state to process the snoop and then return to the AutoHALT power down state.



6.1.2.3 C1/MWAIT Power Down State

C1/MWAIT is a low-power state entered when one thread executes the MWAIT (C1) instruction while the other thread is in the TC1 or greater thread state. processor core behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M and Volume 2B: Instruction Set Reference, N-Z,* for more information.

Table 6-45. Coordination of Core Power States at the Package Level

Package C-State		Core 1					
		C0		C1		--	
Core 0	C0	C0		C0		--	
	C1	C0		C1		--	

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7 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section Thermal Specifications. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsink attached to the exposed processor die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a system fan used to evacuate or pull air through the system. For more information on designing a component level thermal solution, please refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.7). Alternatively, the processor may be in a fan-less system, but would likely still use a multi-component heat spreader. Note that trading of thermal solutions also involves trading performance.

7.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 7-46. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.7).

The case temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 7-46 instead of the maximum processor power consumption. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section Section 7.1.2. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

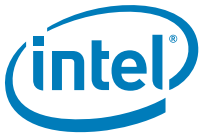


Table 7-46.Power Specifications for the Standard Voltage Processor

Symbol	Processor Number	Core Frequency	Thermal Design Power			Unit	Tj min (°C)	Tj max (°C)	Notes
TDP	D510	1.66		<=13		W	0	100	1, 3, 4, 5
	D410	1.66		<=10		W		100	
	D525	1.80		<=13		W			
	D425	1.80		<=10		W			
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**			
P_{IDLE}	Idle Power D510			4.5		W			2
	Idle Power D410			3.8		W			
	Idle Power D525			4.8		W			
	Idle Power D425			4.0		W			

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
4. V_{CC} is determined by processor VID[6:0].
5. Silicon projection.

The processor incorporates 3 methods of monitoring die temperature: Digital Thermal Sensor, Intel Thermal Monitor, and the Thermal Diode. The Intel Thermal Monitor (detailed in Section Section 7.1.2) must be used to determine when the maximum specified processor junction temperature has been reached.

7.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal “diode”, with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. See Section 7.1.2 for more details. See Section Section 7.1.2 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest

location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode T_{offset} value programmed into the processor Model Specific Register (MSR).

Table 7-47 and Table 7-48 provide the diode interface and specifications. Transistor model parameters shown in Table 7-48 providing more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 7-47.Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THRMDA_1	D30	Thermal diode anode
THRMDA_2	C30	Thermal diode anode (for dual-core only)
THRMDC_1	E30	Thermal diode cathode
THRMDC_2	D31	Thermal diode cathode (for dual-core only)

Table 7-48.Thermal Diode Parameters using Transistor Model

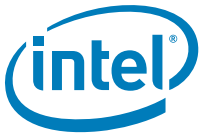
Symbol	Parameter	Min	Typ	Max	Unit	Notes
IFW	Forward Bias Current	5		200	μA	1
IE	Emitter Current	5		200	μA	1
nQ	Transistor Ideality	0.997	1.001	1.015		2,3,4
Beta		0.25		0.65		2,3
RT	Series Resistance	2.79	4.52	6.24	Ω	2,5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_QkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, provided in the Diode Model Table (Table 7-48) can be used for more accurate readings as needed.



When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 7-48. In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} * (1 - n_{actual}/n_{trim})$$

where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

7.1.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

Intel Thermal Monitor 1 (TM1) mode is selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processors.

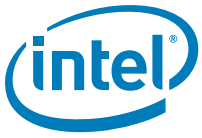
The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 4.



7.1.3 Digital Thermal Sensor

The processor also contains an on die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). Each core of the processor will have a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}. Catastrophic temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Spec status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor 1(TM1) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 hardware thermal control mechanism will activate. The DTS and TM1 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

Note: The Digital Thermal Sensor (DTS) accuracy is in the order of -5°C to +10°C around 100°C. I deteriorates to -10°C to +15°C at 50°C. The DTS temperature reading saturates at some temperature below 50°C. Any DTS reading below 50°C should be considered to indicate only a temperature below 50°C and not a specific temperature. External thermal sensor with “BJT” model is required to read thermal diode temperature if more accurate temperature reading is needed.

7.1.4 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor’s TM1 is triggered and the temperature

remains high, an “Out Of Spec” status and sticky bit are latched in the status MSR register and generates thermal interrupt. For more details on the interrupt mechanism, refer to the *RS - Intel® Atom™ Processor D400 and D500 Series BIOS Writer’s Guide*.

7.1.5 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and *RS - Intel® Atom™ Processor D400 and D500 Series BIOS Writer’s Guide* for specific register and programming details.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If TM1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clock modulated. It is important to note that Intel recommends TM1 to be enabled.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

Refer to the *Pinetrail-D Platform Design Guide* for details on implementing the bi-directional PROCHOT# feature.

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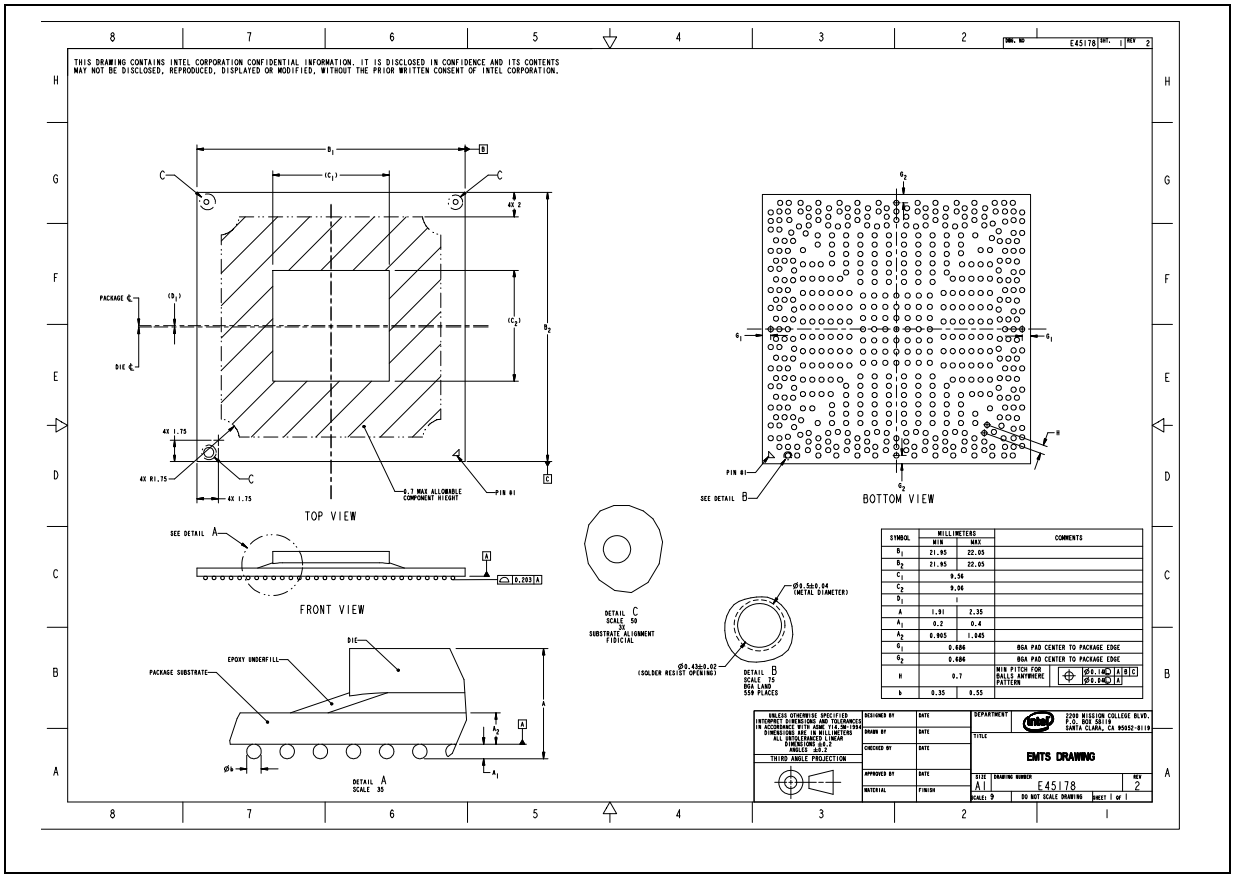
8 Package Mechanical Specifications and Ball Information

This chapter provides the package specifications, and ballout assignments.

8.1 Package Mechanical Specifications

8.1.1 Package Mechanical Drawings

Figure 8-5. Package Mechanical Drawings



8.1.2 Package Loading Specifications

Package loading is 15lb max static compressive.

8.2 Processor Ballout Assignment

Figure 8-6 to Figure 8-9 are graphic representations of the processor ballout assignments. Table 8-49 lists the ballout by signal name.

Figure 8-6. Package Pinmap (Top View, Upper-Left Quadrant)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	---	---	RSVD_NCTF_1	RSVD_NCTF_11	---	---	XDP_RSVD_1	---	XDP_RSVD_8	---	VSS	---	GTLREF	---	---	VSS
B	---	VCCRING_WEST	VCC	VCCP	VSS	---	XDP_RSVD_7	XDP_RSVD_11	VSS	XDP_RSVD_15	XDP_RSVD_14	XDP_RSVD_16	VSS	TCK	---	VSS
C	RSVD_NCTF_7	VCCRING_WEST	VCCRING_WEST	---	XDP_RSVD_3	XDP_RSVD_5	XDP_RSVD_4	XDP_RSVD_10	---	XDP_RSVD_12	XDP_RSVD_17	VSS	---	TMS	---	TRST_B
D	---	---	---	VCCP	---	XDP_RSVD_2	---	XDP_RSVD_6	XDP_RSVD_9	XDP_RSVD_13	---	XDP_RSVD_0	TDO	TDI	---	---
E	RSVD_NCTF_9	VCCP	---	---	IGNNE_B	---	SMI_B	VSS	---	VSS	PRDY_B	---	THERMTRIP_B	---	BPM_1B_1	---
F	---	DMI_RXN_0	DMI_RXP_0	VSS	---	---	---	STPCLK_B	---	LINT00	LINT10	---	BPM_1B_3	---	PREQ_B	---
G	DMI_TXN_0	DMI_TXP_0	DMI_RXN_1	---	RSVD_16	DPRSTP_B	---	INIT_B	---	DPSLP_B	BPM_1B_0	---	BPM_1B_2	---	VSS	---
H	---	VSS	DMI_TXP_1	DMI_RXP_1	BSEL_1	FERR_B	A20M_B	VSS	---	BCLKN	VSS	---	RSVD_4	---	VSS	---
J	DMI_RXN_2	DMI_TXN_1	---	VSS	---	---	---	---	---	BCLKP	VSS	---	VSS	---	VSS	---
K	---	DMI_RXP_2	DMI_TXP_2	VSS	BSEL_0	BSEL_2	EXTBGREF	VSS	RSVD_TP_4	---	VSS	---	VSS	---	VCC	---
L	VSS	DMI_TXN_2	DMI_RXN_3	---	PWROK	RSVD_8	RSVD_6	EXP_RBIAS	EXP_ICOMPI	EXP_RCOMPO	RSVD_9	---	VSS	VCC	---	VCC
M	---	DMI_TXP_3	VSS	DMI_RXP_3	---	---	---	---	---	---	---	---	---	---	---	---
N	VSS	DMI_TXN_3	---	VSS	VSS	EXP_CLKINP	EXP_CLKINN	VSS	RSVD_11	RSVD_10	RSVD_TP_10	---	VSS	VCC	---	VCC
P	---	RSVD_3	VSS	VSS	---	---	---	---	---	---	RSVD_TP_11	---	VSS	VSS	---	VSS
R	---	---	---	---	RSVD_TP_3	RSVD_TP_2	VSS	VSS	RSVD_13	RSVD_12	---	---	---	---	---	---

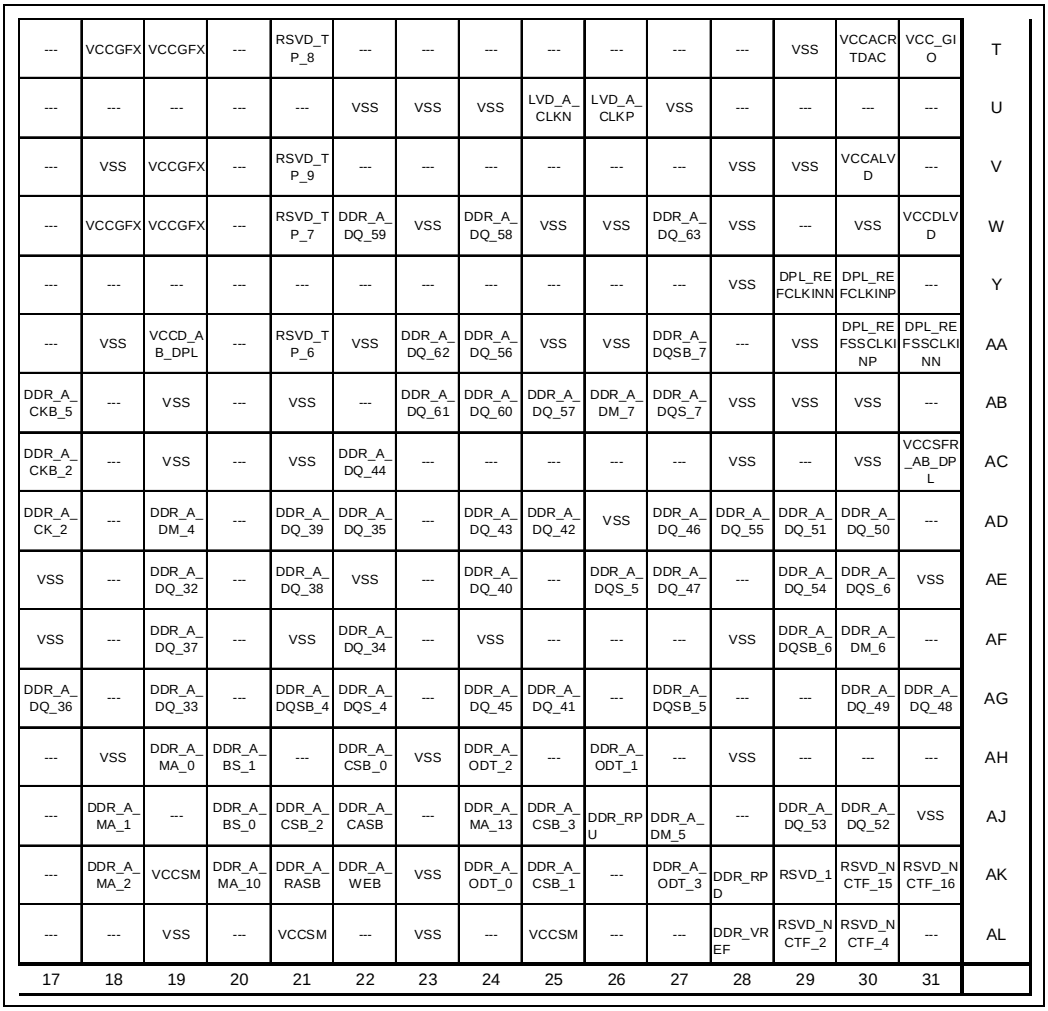
Figure 8-7. Package Pinmap (Top View, Upper-Right Quadrant)

17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
---	---	VSS	---	VCC_LGI_VID	---	VCC	---	VCC	---	VCC	---	RSVD_NCTF_0	RSVD_NCTF_10	---	A
---	BPM_2B_0	VSS	BPM_2B_1	BPM_2B_3	VSS	VCC	VCC	VCC	VCC	VCC	---	VSSSENSE	RSVD_NCTF_5	RSVD_NCTF_6	B
---	PROCHOT_B	---	BPM_2B_2	VSS	VSS	---	VCC	VSS	VCC	---	---	VCCSENSE	THRMDA_2	RSVD_NCTF_8	C
---	RSVD_5	RSVD_TP_5	RSVD_7	---	VSS	VCC	VCC	---	VCC	---	VCC	---	THRMDA_1	THRMDC_2	D
RSVD_0	---	VSS	---	VSS	VCC	---	VCC	VSS	---	VCC	---	VID_6	THRMDC_1	---	E
VSS	---	VSS	---	VCC	VCC	---	VSS	VCC	---	---	VSS	VID_5	---	---	F
VSS	---	VCC	---	VCC	VSS	---	VCC	---	---	VSS	---	VID_4	VID_3	VSS	G
VCC	---	VCC	---	VSS	VCC	---	VCC	VSS	LVDD_EN	VSS	VID_2	VID_1	VID_0	---	H
VCC	---	VCC	---	VCC	VCC	---	---	---	---	---	LVD_VBG	---	RSVD_14	VCCRING_EAST	J
VCC	---	VSS	---	VCC	---	LDDC_CLK	LDDC_DATA	LCTLB_DATA	VSS	VSS	VSS	RSVD_15	VSS	---	K
---	VSS	VCC	---	VCC	VSS	LCTLA_CLK	VSS	VSS	LBKLT_CTL	LBKLT_EN	---	VSS	CRT_DDC_CLK	CRT_DDC_DATA	L
---	---	---	---	---	---	---	---	---	---	---	VSS	CRT_VSYNC	CRT_HSYNC	---	M
---	VSS	VCC	---	VCC	LVD_VREFH	LVD_VREFL	VSS	VSS	LVD_A_DATAN_1	LVD_A_DATAP_1	VSS	---	CRT_IRTN	CRT_RED	N
---	VSS	VSS	---	VSS	---	---	---	---	---	---	DAC_IREF	CRT_BLUE	CRT_GREEN	---	P
---	---	---	---	---	LVD_IBG	LVD_A_DATAN_0	LVD_A_DATAP_0	VSS	LVD_A_DATAN_2	LVD_A_DATAP_2	---	---	---	---	R

Figure 8-8. Package Pinmap (Top View, Lower-Left Quadrant)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
T	VCCA_DMI	VCCA_DMI	VCCA_DMI	---	---	---	---	---	---	---	VSS	---	VCCGFX	VCCGFX	---	VCCGFX
U	---	---	---	---	VCCA_DDR	VCCA_DDR	VCCA_DDR	VCCA_DDR	VCCA_DDR	VCCA_DDR	---	---	---	---	---	---
V	---	VCCA_DDR	VCCA_DDR	VCCA_DDR	---	---	---	---	---	---	VCCD_HMPLL	---	VCCGFX	VSS	---	VSS
W	CPUPWRGOOD	VSS	---	VSS	VSS	VSS	VSS	HPL_CLKINN	HPL_CLKINP	VCCA_DDR	VCCA_DDR	---	VSS	VCCGFX	---	VCCGFX
Y	---	VCCA	VSS	VSS	---	---	---	---	---	---	---	---	---	---	---	---
AA	VCCSFR_DMIHMPLL	VSS	RSTINB	---	DDR_A_DQ_12	RSVD_TP_12	RSVD_TP_13	VSS	DDR_A_DM_1	VCCACK_DDR	VCCACK_DDR	---	VSS	VSS	---	VSS
AB	---	DDR_A_DQ_4	DDR_A_DQ_5	DDR3_DRAM_PWROK	DDR_A_DQ_13	DDR_A_DQ_8	DDR_A_DQ_9	DDR_A_DQS_1	DDR_A_DQ_14	---	RSVD_TP_0	---	RSVD_TP_1	---	DDR_A_CK_5	---
AC	DDR_A_DQ_1	VSS	---	DDR_A_DQ_0	---	---	---	---	---	VSS	VSS	---	DDR_A_CKB_1	---	DDR_A_CK_3	---
AD	---	DDR_A_DQSB_0	DDR_A_DQS_0	DDR_A_DM_0	VSS	DDR_A_DQ_15	DDR_A_DQSB_1	DDR_A_DQS_2	---	DDR_A_DQSB_2	DDR_A_DQ_22	---	DDR_A_CK_1	---	DDR_A_CKB_3	---
AE	VSS	DDR_A_DQ_6	DDR_A_DQ_7	---	DDR_A_DQ_10	---	---	DDR_A_DM_2	---	DDR_A_DQ_23	VSS	---	VSS	---	VSS	---
AF	---	---	DDR_A_DQ_28	DDR_A_DQ_2	---	---	DDR_A_DQ_20	DDR_A_DQ_21	---	DDR_A_DQ_18	VSS	---	DDR_A_CK_4	---	DDR_A_CKB_0	---
AG	---	DDR_A_DQ_3	VSS	---	DDR_A_DQ_11	---	DDR_A_DQ_17	DDR_A_DQ_16	---	VSS	DDR_A_DQ_19	---	DDR_A_CKB_4	---	DDR_A_CK_0	---
AH	DDR_A_DQ_24	DDR_A_DQ_29	---	VSS	---	VSS	---	VSS	DDR_A_CKE_1	DDR_A_CKE_0	---	DDR_A_MA_11	DDR_A_MA_8	DDR_A_MA_5	---	---
AJ	RSVD_NCTF_12	DDR_A_DQ_25	DDR_A_DM_3	---	---	DDR_A_DQ_31	DDR_A_DQ_27	DDR_A_CKE_3	---	DDR_A_MA_14	DDR_A_MA_12	DDR_A_MA_7	---	DDR_A_MA_4	---	VSS
AK	RSVD_NCTF_13	RSVD_NCTF_14	DDR_A_DQSB_3	---	DDR_A_DQS_3	DDR_A_DQ_26	VCCCK_DDR	DDR3_DRAMRST#	VCCSM	DDR_A_CKE_2	DDR_A_BS_2	DDR_A_MA_9	VCCSM	DDR_A_MA_6	---	DDR_A_MA_3
AL	---	RSVD_NCTF_17	RSVD_NCTF_3	---	DDR_A_DQ_30	---	VCCCK_DDR	---	VSS	---	VSCCSM	---	VSS	---	---	VCCSM

Figure 8-9. Package Pinmap (Top View, Lower-Right Quadrant)



---	VCCGFX	VCCGFX	---	RSVD_TP_8	---	---	---	---	---	---	---	VSS	VCCACRTDAC	VCC_GIO	T
---	---	---	---	---	VSS	VSS	VSS	LVD_A_CLKN	LVD_A_CLKP	VSS	---	---	---	---	U
---	VSS	VCCGFX	---	RSVD_TP_9	---	---	---	---	---	---	VSS	VSS	VCCALVD	---	V
---	VCCGFX	VCCGFX	---	RSVD_TP_7	DDR_A_DQ_59	VSS	DDR_A_DQ_58	VSS	VSS	DDR_A_DQ_63	VSS	---	VSS	VCCDLVD	W
---	---	---	---	---	---	---	---	---	---	---	VSS	DPL_REFCLKINN	DPL_REFCLKINP	---	Y
---	VSS	VCCD_AB_DPL	---	RSVD_TP_6	VSS	DDR_A_DQ_62	DDR_A_DQ_56	VSS	VSS	DDR_A_DQSB_7	---	VSS	DPL_REFSSCLKINP	DPL_REFSSCLKINN	AA
DDR_A_CKB_5	---	VSS	---	VSS	---	DDR_A_DQ_61	DDR_A_DQ_60	DDR_A_DQ_57	DDR_A_DM_7	DDR_A_DQS_7	VSS	VSS	VSS	---	AB
DDR_A_CKB_2	---	VSS	---	VSS	DDR_A_DQ_44	---	---	---	---	---	VSS	---	VSS	VCCSFR_AB_DPL	AC
DDR_A_CK_2	---	DDR_A_DM_4	---	DDR_A_DQ_39	DDR_A_DQ_35	---	DDR_A_DQ_43	DDR_A_DQ_42	VSS	DDR_A_DQ_46	DDR_A_DQ_55	DDR_A_DQ_51	DDR_A_DQ_50	---	AD
VSS	---	DDR_A_DQ_32	---	DDR_A_DQ_38	VSS	---	DDR_A_DQ_40	---	DDR_A_DQS_5	DDR_A_DQ_47	---	DDR_A_DQ_54	DDR_A_DQS_6	VSS	AE
VSS	---	DDR_A_DQ_37	---	VSS	DDR_A_DQ_34	---	VSS	---	---	---	VSS	DDR_A_DQSB_6	DDR_A_DM_6	---	AF
DDR_A_DQ_36	---	DDR_A_DQ_33	---	DDR_A_DQSB_4	DDR_A_DQS_4	---	DDR_A_DQ_45	DDR_A_DQ_41	---	DDR_A_DQSB_5	---	---	DDR_A_DQ_49	DDR_A_DQ_48	AG
---	VSS	DDR_A_MA_0	DDR_A_BS_1	---	DDR_A_CSB_0	VSS	DDR_A_ODT_2	---	DDR_A_ODT_1	---	VSS	---	---	---	AH
---	DDR_A_MA_1	---	DDR_A_BS_0	DDR_A_CSB_2	DDR_A_CASB	---	DDR_A_MA_13	DDR_A_CSB_3	DDR_RPU	DDR_A_DM_5	---	DDR_A_DQ_53	DDR_A_DQ_52	VSS	AJ
---	DDR_A_MA_2	VCCSM	DDR_A_MA_10	DDR_A_RASB	DDR_A_WEB	VSS	DDR_A_ODT_0	DDR_A_CSB_1	---	DDR_A_ODT_3	DDR_RPD	RSVD_1	RSVD_NCTF_15	RSVD_NCTF_16	AK
---	---	VSS	---	VCCSM	---	VSS	---	VCCSM	---	---	DDR_VREF	RSVD_NCTF_2	RSVD_NCTF_4	---	AL
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	

Table 8-49. Processor Ball List by Ball Name (Sheet 1 of 9)

Pin Name	Pin Number	Type	Dir.
A20M_B	H7	CPU legacy	I/O
BCLKN	H10	CPU legacy	I
BCLKP	J10	CPU legacy	I
BPM_1B_0	G11	CPU legacy	I/O
BPM_1B_1	E15	CPU legacy	I/O
BPM_1B_2	G13	CPU legacy	I/O
BPM_1B_3	F13	CPU legacy	I/O
BPM_2B_0	B18	CPU legacy	I/O
BPM_2B_1	B20	CPU legacy	I/O

Pin Name	Pin Number	Type	Dir.
DDR_A_CKB_4	AG13	MEM_Clk_A	O
DDR_A_CKB_5	AB17	MEM_Clk_A	O
DDR_A_CKE_0	AH10	MEM_Cntl_A	O
DDR_A_CKE_1	AH9	MEM_Cntl_A	O
DDR_A_CKE_2	AK10	MEM_Cntl_A	O
DDR_A_CKE_3	AJ8	MEM_Cntl_A	O
DDR_A_CSB_0	AH22	MEM_Cntl_A	O
DDR_A_CSB_1	AK25	MEM_Cntl_A	O
DDR_A_CSB_2	AJ21	MEM_Cntl_A	O

Table 8-49.Processor Ball List by Ball Name (Sheet 2 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
BPM_2B_2	C20	CPU legacy	I/O	DDR_A_CSB_3	AJ25	MEM_Cntl_A	O
BPM_2B_3	B21	CPU legacy	I/O	DDR_A_DM_0	AD4	MEM_Ad	O
BSEL_0	K5	CPU legacy	I/O	DDR_A_DM_1	AA9	MEM_Ad	O
BSEL_1	H5	CPU legacy	I/O	DDR_A_DM_2	AE8	MEM_Ad	O
BSEL_2	K6	CPU legacy	I/O	DDR_A_DM_3	AJ3	MEM_Ad	O
CPUPWRGOOD	W1	CPU legacy	I	DDR_A_DM_4	AD19	MEM_Ad	O
CRT_BLUE	P29	CRTDAC	O	DDR_A_DM_5	AJ27	MEM_Ad	O
CRT_DDC_CLK	L30	CRTDAC	I/O	DDR_A_DM_6	AF30	MEM_Ad	O
CRT_DDC_DATA	L31	CRTDAC	I/O	DDR_A_DM_7	AB26	MEM_Ad	O
CRT_GREEN	P30	CRTDAC	O	DDR_A_DQ_0	AC4	MEM_Ad	I/O
CRT_HSYNC	M30	CRTDAC	O	DDR_A_DQ_1	AC1	MEM_Ad	I/O
CRT_IRTN	N30	CRTDAC	O	DDR_A_DQ_10	AE5	MEM_Ad	I/O
CRT_RED	N31	CRTDAC	O	DDR_A_DQ_11	AG5	MEM_Ad	I/O
CRT_VSYNC	M29	CRTDAC	O	DDR_A_DQ_12	AA5	MEM_Ad	I/O
DAC_IREF	P28	CRTDAC	I/O	DDR_A_DQ_13	AB5	MEM_Ad	I/O
DDR_A_BS_0	AJ20	MEM_Cntl_A	O	DDR_A_DQ_14	AB9	MEM_Ad	I/O
DDR_A_BS_1	AH20	MEM_Cntl_A	O	DDR_A_DQ_15	AD6	MEM_Ad	I/O
DDR_A_BS_2	AK11	MEM_Cntl_A	O	DDR_A_DQ_16	AG8	MEM_Ad	I/O
DDR_A_CASB	AJ22	MEM_Cntl_A	O	DDR_A_DQ_17	AG7	MEM_Ad	I/O
DDR_A_CK_0	AG15	MEM_Clk_A	O	DDR_A_DQ_18	AF10	MEM_Ad	I/O
DDR_A_CK_1	AD13	MEM_Clk_A	O	DDR_A_DQ_19	AG11	MEM_Ad	I/O
DDR_A_CK_2	AD17	MEM_Clk_A	O	DDR_A_DQ_2	AF4	MEM_Ad	I/O
DDR_A_CK_3	AC15	MEM_Clk_A	O	DDR_A_DQ_20	AF7	MEM_Ad	I/O
DDR_A_CK_4	AF13	MEM_Clk_A	O	DDR_A_DQ_21	AF8	MEM_Ad	I/O
DDR_A_CK_5	AB15	MEM_Clk_A	O	DDR_A_DQ_22	AD11	MEM_Ad	I/O
DDR_A_CKB_0	AF15	MEM_Clk_A	O	DDR_A_DQ_23	AE10	MEM_Ad	I/O
DDR_A_CKB_1	AC13	MEM_Clk_A	O	DDR_A_DQ_24	AH1	MEM_Ad	I/O
DDR_A_CKB_2	AC17	MEM_Clk_A	O	DDR_A_DQ_25	AJ2	MEM_Ad	I/O
DDR_A_CKB_3	AD15	MEM_Clk_A	O	DDR_A_DQ_28	AF3	MEM_Ad	I/O
DDR_A_DQ_29	AH2	MEM_Ad	I/O	DDR_A_DQ_8	AB6	MEM_Ad	I/O
DDR_A_DQ_3	AG2	MEM_Ad	I/O	DDR_A_DQ_9	AB7	MEM_Ad	I/O
DDR_A_DQ_30	AL5	MEM_Ad	I/O	DDR_A_DQS_0	AD3	MEM_Ad	O
DDR_A_DQ_31	AJ6	MEM_Ad	I/O	DDR_A_DQS_1	AB8	MEM_Ad	O
DDR_A_DQ_32	AE19	MEM_Ad	I/O	DDR_A_DQS_2	AD8	MEM_Ad	O
DDR_A_DQ_33	AG19	MEM_Ad	I/O	DDR_A_DQS_3	AK5	MEM_Ad	O
DDR_A_DQ_34	AF22	MEM_Ad	I/O	DDR_A_DQS_4	AG22	MEM_Ad	O
DDR_A_DQ_35	AD22	MEM_Ad	I/O	DDR_A_DQS_5	AE26	MEM_Ad	O
DDR_A_DQ_36	AG17	MEM_Ad	I/O	DDR_A_DQS_6	AE30	MEM_Ad	O
DDR_A_DQ_37	AF19	MEM_Ad	I/O	DDR_A_DQS_7	AB27	MEM_Ad	O

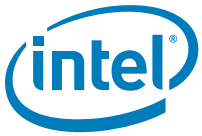


Table 8-49.Processor Ball List by Ball Name (Sheet 3 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
DDR_A_DQ_38	AE21	MEM_Ad	I/O	DDR_A_DQSB_0	AD2	MEM_Ad	O
DDR_A_DQ_39	AD21	MEM_Ad	I/O	DDR_A_DQSB_1	AD7	MEM_Ad	O
DDR_A_DQ_4	AB2	MEM_Ad	I/O	DDR_A_DQSB_2	AD10	MEM_Ad	O
DDR_A_DQ_40	AE24	MEM_Ad	I/O	DDR_A_DQSB_3	AK3	MEM_Ad	O
DDR_A_DQ_41	AG25	MEM_Ad	I/O	DDR_A_DQSB_4	AG21	MEM_Ad	O
DDR_A_DQ_42	AD25	MEM_Ad	I/O	DDR_A_DQSB_5	AG27	MEM_Ad	O
DDR_A_DQ_43	AD24	MEM_Ad	I/O	DDR_A_DQSB_6	AF29	MEM_Ad	O
DDR_A_DQ_44	AC22	MEM_Ad	I/O	DDR_A_DQSB_7	AA27	MEM_Ad	O
DDR_A_DQ_45	AG24	MEM_Ad	I/O	DDR_A_MA_0	AH19	MEM_Cntl_A	O
DDR_A_DQ_46	AD27	MEM_Ad	I/O	DDR_A_MA_1	AJ18	MEM_Cntl_A	O
DDR_A_DQ_47	AE27	MEM_Ad	I/O	DDR_A_MA_10	AK20	MEM_Cntl_A	O
DDR_A_DQ_48	AG31	MEM_Ad	I/O	DDR_A_MA_11	AH12	MEM_Cntl_A	O
DDR_A_DQ_49	AG30	MEM_Ad	I/O	DDR_A_MA_12	AJ11	MEM_Cntl_A	O
DDR_A_DQ_5	AB3	MEM_Ad	I/O	DDR_A_MA_13	AJ24	MEM_Cntl_A	O
DDR_A_DQ_50	AD30	MEM_Ad	I/O	DDR_A_MA_14	AJ10	MEM_Cntl_A	O
DDR_A_DQ_51	AD29	MEM_Ad	I/O	DDR_A_MA_2	AK18	MEM_Cntl_A	O
DDR_A_DQ_52	AJ30	MEM_Ad	I/O	DDR_A_MA_3	AK16	MEM_Cntl_A	O
DDR_A_DQ_53	AJ29	MEM_Ad	I/O	DDR_A_MA_4	AJ14	MEM_Cntl_A	O
DDR_A_DQ_54	AE29	MEM_Ad	I/O	DDR_A_MA_5	AH14	MEM_Cntl_A	O
DDR_A_DQ_55	AD28	MEM_Ad	I/O	DDR_A_MA_6	AK14	MEM_Cntl_A	O
DDR_A_DQ_56	AA24	MEM_Ad	I/O	DDR_A_MA_7	AJ12	MEM_Cntl_A	O
DDR_A_DQ_57	AB25	MEM_Ad	I/O	DDR_A_MA_8	AH13	MEM_Cntl_A	O
DDR_A_DQ_58	W24	MEM_Ad	I/O	DDR_A_MA_9	AK12	MEM_Cntl_A	O
DDR_A_DQ_59	W22	MEM_Ad	I/O	DDR_A_ODT_0	AK24	MEM_Cntl_A	O
DDR_A_DQ_6	AE2	MEM_Ad	I/O	DDR_A_ODT_1	AH26	MEM_Cntl_A	O
DDR_A_DQ_60	AB24	MEM_Ad	I/O	DDR_A_ODT_2	AH24	MEM_Cntl_A	O
DDR_A_DQ_61	AB23	MEM_Ad	I/O	DDR_A_ODT_3	AK27	MEM_Cntl_A	O
DDR_A_DQ_62	AA23	MEM_Ad	I/O	DDR_A_RASB	AK21	MEM_Cntl_A	O
DDR_A_DQ_63	W27	MEM_Ad	I/O	DDR_A_WEB	AK22	MEM_Cntl_A	O
DDR_A_DQ_7	AE3	MEM_Ad	I/O	DDR_RPD	AK28	MEM_Ana	I/O
DDR_RPU	AJ26	MEM_Ana	I/O	LCTLB_DATA	K25	LVDS	I/O
DDR3_DRAM_PWROK	AB4	MEM_Ana	I	LDDC_CLK	K23	LVDS	I/O
DDR_VREF	AL28	MEM_Ana	I	LDDC_DATA	K24	LVDS	I/O
DMI_RXN_0	F2	3GIO_CTC_rx	I	LINT00	F10	CPU_sideband	I
DMI_RXN_1	G3	3GIO_CTC_rx	I	LINT10	F11	CPU_sideband	I
DMI_RXN_2	J1	3GIO_CTC_rx	I	LVD_A_CLKN	U25	LVDS	O
DMI_RXN_3	L3	3GIO_CTC_rx	I	LVD_A_CLKP	U26	LVDS	O
DMI_RXP_0	F3	3GIO_CTC_rx	I	LVD_A_DATAN_0	R23	LVDS	O
DMI_RXP_1	H4	3GIO_CTC_rx	I	LVD_A_DATAN_1	N26	LVDS	O

Table 8-49.Processor Ball List by Ball Name (Sheet 4 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
DMI_RXP_2	K2	3GIO_CTC_rx	I	LVD_A_DATAN_2	R26	LVDS	O
DMI_RXP_3	M4	3GIO_CTC_rx	I	LVD_A_DATAP_0	R24	LVDS	O
DMI_TXN_0	G1	3GIO_CTC_tx	O	LVD_A_DATAP_1	N27	LVDS	O
DMI_TXN_1	J2	3GIO_CTC_tx	O	LVD_A_DATAP_2	R27	LVDS	O
DMI_TXN_2	L2	3GIO_CTC_tx	O	LVD_IBG	R22	LVDS	I/O
DMI_TXN_3	N2	3GIO_CTC_tx	O	LVD_VBG	J28	LVDS	O
DMI_TXP_0	G2	3GIO_CTC_tx	O	LVD_VREFH	N22	LVDS	I
DMI_TXP_1	H3	3GIO_CTC_tx	O	LVD_VREFL	N23	LVDS	I
DMI_TXP_2	K3	3GIO_CTC_tx	O	LVDD_EN	H26	LVDS	O
DMI_TXP_3	M2	3GIO_CTC_tx	O	RSVD_14	J30		I
DPL_REFCLKINN	Y29	Display PLL	I	RSVD_15	K29		I
DPL_REFCLKINP	Y30	Display PLL	I	PRDY_B	E11	CPU_sideband	I/O
DPRSTP_B	G6	CPU_sideband	I	PREQ_B	F15	CPU_sideband	I/O
DPSLP_B	G10	CPU_sideband	I	PROCHOT_B	C18	CPU_legacy	I/O
EXP_CLKINN	N7	3GIO_GFX_clk	I	PWROK	L5	MISC	I/O
EXP_CLKINP	N6	3GIO_GFX_clk	I	RSTINB	AA3	MISC	I
EXP_ICOMPI	L9	3GIO_GFX_ana	I	RSVD_TP_0	AB11		
EXP_RBIAS	L8	3GIO_GFX_ana	I/O	RSVD_TP_1	AB13		
EXP_RCOMPO	L10	3GIO_GFX_ana	I	DDR3_DRAMRST#	AK8		
RSVD_12	R10			RSVD_TP_6	AA21		
RSVD_13	R9			RSVD_TP_7	W21		
EXTBGREF	K7	CPU_legacy	I	RSVD_TP_8	T21		
FERR_B	H6	CPU_sideband	O	RSVD_TP_9	V21		
GTLREF	A13	CPU_legacy	I	DPL_REFSSCLKINN	AA31	Clock for LVDS	I
HPL_CLKINN	W8	Host PLL	I	DPL_REFSSCLKINP	AA30	Clock for LVDS	I
HPL_CLKINP	W9	Host PLL	I	RSVD_9	L11		
IGNNE_B	E5	CPU_sideband	I/O	RSVD_10	N10		
INIT_B	G8	CPU_sideband	I/O	RSVD_11	N9		
LBKLT_CTL	L26	LVDS	O	RSVD_TP_10	N11		
LBKLT_EN	L27	LVDS	O	RSVD_TP_11	P11		
LCTLA_CLK	L23	LVDS	I/O	RSVD_TP_12	AA6		
RSVD_TP_13	AA7			VCC	E27	PWR	
RSVD_TP_2	R6			VCC	F21	PWR	
RSVD_TP_3	R5			VCC	F22	PWR	
RSVD_4	H13			VCC	F25	PWR	
RSVD_5	D18			VCC	G19	PWR	
RSVD_6	L7			VCC	G21	PWR	
RSVD_7	D20			VCC	G24	PWR	
RSVD_8	L6			VCC	H17	PWR	

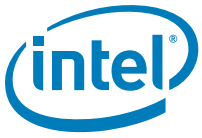


Table 8-49.Processor Ball List by Ball Name (Sheet 5 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
RSVD_0	E17			VCC	H19	PWR	
RSVD_TP_4	K9			VCC	H22	PWR	
RSVD_TP_5	D19			VCC	H24	PWR	
SMI_B	E7	CPU_sideband	I/O	VCC	J17	PWR	
STPCLK_B	F8	CPU_sideband	I	VCC	J19	PWR	
TCK	B14	CPU_legacy	I/O	VCC	J21	PWR	
TDI	D14	CPU_legacy	I/O	VCC	J22	PWR	
TDO	D13	CPU_legacy	I/O	VCC	K15	PWR	
RSVD_16	G5	RSVD		VCC	K17	PWR	
THERMTRIP_B	E13	CPU_sideband	O	VCC	K21	PWR	
THRMDA_1	D30	CPU_legacy	I	VCC	L14	PWR	
THRMDA_2	C30	CPU_legacy	I	VCC	L16	PWR	
THRMDC_1	E30	CPU_legacy	O	VCC	L19	PWR	
THRMDC_2	D31	CPU_legacy	O	VCC	L21	PWR	
TMS	C14	CPU_legacy	I/O	VCC	N14	PWR	
TRST_B	C16	CPU_legacy	I/O	VCC	N16	PWR	
VCC	A23	PWR		VCC	N19	PWR	
VCC	A25	PWR		VCC	N21	PWR	
VCC	A27	PWR		VCCP	B3	PWR	
VCC	B23	PWR		VCCP	B4	PWR	
VCC	B24	PWR		VCCP	E2	PWR	
VCC	B25	PWR		VCCP	D4	PWR	
VCC	B26	PWR		VCCRING_EAST	J31	PWR	
VCC	B27	PWR		VCCRING_WEST	B2	PWR	
VCC	C24	PWR		VCCRING_WEST	C2	PWR	
VCC	C26	PWR		VCCRING_WEST	C3	PWR	
VCC	D23	PWR		VCCSM	AK13	PWR	
VCC	D24	PWR		VCCSM	AK19	PWR	
VCC	D26	PWR		VCCSM	AK9	PWR	
VCC	D28	PWR		VCCSM	AL11	PWR	
VCC	E22	PWR		VCCSM	AL16	PWR	
VCC	E24	PWR		VCCSM	AL21	PWR	
VCCSM	AL25	PWR		VCCSFR_AB_DPL	AC31	PWR	
VCC_GIO	T31	PWR		VCCSFR_DMIHMPLL	AA1	PWR	
VCC_LGI_VID	A21	PWR		VID_0	H30	CPU_legacy	O
VCCA	Y2	PWR		VID_1	H29	CPU_legacy	O
VCCA_DDR	U10	PWR		VID_2	H28	CPU_legacy	O
VCCA_DDR	U5	PWR		VID_3	G30	CPU_legacy	O
VCCA_DDR	U6	PWR		VID_4	G29	CPU_legacy	O

Table 8-49.Processor Ball List by Ball Name (Sheet 6 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
VCCA_DDR	U7	PWR		VID_5	F29	CPU_legacy	O
VCCA_DDR	U8	PWR		VID_6	E29	CPU_legacy	O
VCCA_DDR	U9	PWR		VSS	H27	VSS	
VCCA_DDR	V2	PWR		VSS	A11	VSS	
VCCA_DDR	V3	PWR		VSS	A16	VSS	
VCCA_DDR	V4	PWR		VSS	A19	VSS	
VCCA_DDR	W10	PWR		RSVD_NCTF_0	A29	VSS	
VCCA_DDR	W11	PWR		RSVD_NCTF_1	A3	VSS	
VCCA_DMI	T1	PWR		RSVD_NCTF_10	A30	VSS	
VCCA_DMI	T2	PWR		RSVD_NCTF_11	A4	VSS	
VCCA_DMI	T3	PWR		VSS	AA13	VSS	
VCCALVD	V30	PWR		VSS	AA14	VSS	
VCCACK_DDR	AA10	PWR		VSS	AA16	VSS	
VCCACK_DDR	AA11	PWR		VSS	AA18	VSS	
VCCACRTDAC	T30	PWR		VSS	AA2	VSS	
VCCCK_DDR	AK7	PWR		VSS	AA22	VSS	
VCCCK_DDR	AL7	PWR		VSS	AA25	VSS	
VCCD_AB_DPL	AA19	PWR		VSS	AA26	VSS	
VCCD_HMPLL	V11	PWR		VSS	AA29	VSS	
VCCDLVD	W31	PWR		VSS	AA8	VSS	
VCCGFX	T13	PWR		VSS	AB19	VSS	
VCCGFX	T14	PWR		VSS	AB21	VSS	
VCCGFX	T16	PWR		VSS	AB28	VSS	
VCCGFX	T18	PWR		VSS	AB29	VSS	
VCCGFX	T19	PWR		VSS	AB30	VSS	
VCCGFX	V13	PWR		VSS	AC10	VSS	
VCCGFX	V19	PWR		VSS	AC11	VSS	
VCCGFX	W14	PWR		VSS	AC19	VSS	
VCCGFX	W16	PWR		VSS	AC2	VSS	
VCCGFX	W18	PWR		VSS	AC21	VSS	
VCCGFX	W19	PWR		VSS	AC28	VSS	
VCCSENSE	C29	PWR		VSS	AC30	VSS	
VCCSM	AL25	PWR		VSS	B16	VSS	
VSS	AD26	VSS		VSS	B19	VSS	
VSS	AD5	VSS		VSS	B22	VSS	
VSS	AE1	VSS		RSVD_NCTF_5	B30	VSS	
VSS	AE11	VSS		RSVD_NCTF_6	B31	VSS	
VSS	AE13	VSS		VSS	B5	VSS	
VSS	AE15	VSS					

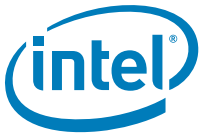


Table 8-49.Processor Ball List by Ball Name (Sheet 7 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
VSS	AE17	VSS		VSS	B9	VSS	
VSS	AE22	VSS		RSVD_NCTF_7	C1	VSS	
VSS	AE31	VSS		VSS	C12	VSS	
VSS	AF11	VSS		VSS	C21	VSS	
VSS	AF17	VSS		VSS	C22	VSS	
VSS	AF21	VSS		VSS	C25	VSS	
VSS	AF24	VSS		RSVD_NCTF_8	C31	VSS	
VSS	AF28	VSS		VSS	D22	VSS	
VSS	AG10	VSS		RSVD_NCTF_9	E1	VSS	
VSS	AG3	VSS		VSS	E10	VSS	
VSS	AH18	VSS		VSS	E19	VSS	
VSS	AH23	VSS		VSS	E21	VSS	
VSS	AH28	VSS		VSS	E25	VSS	
VSS	AH4	VSS		VSS	E8	VSS	
VSS	AH6	VSS		VSS	F17	VSS	
VSS	AH8	VSS		VSS	F19	VSS	
RSVD_NCTF_12	AJ1	VSS		VSS	F24	VSS	
VSS	AJ16	VSS		VSS	F28	VSS	
VSS	AJ31	VSS		VSS	F4	VSS	
RSVD_NCTF_13	AK1	VSS		VSS	G15	VSS	
RSVD_NCTF_14	AK2	VSS		VSS	G17	VSS	
VSS	AK23	VSS		VSS	G22	VSS	
RSVD_NCTF_15	AK30	VSS		VSS	G27	VSS	
RSVD_NCTF_16	AK31	VSS		VSS	G31	VSS	
VSS	AL13	VSS		VSS	H11	VSS	
VSS	AL19	VSS		VSS	H15	VSS	
RSVD_NCTF_17	AL2	VSS		VSS	H2	VSS	
VSS	AL23	VSS		VSS	H21	VSS	
RSVD_NCTF_2	AL29	VSS		VSS	H25	VSS	
RSVD_NCTF_3	AL3	VSS		VSS	H8	VSS	
RSVD_NCTF_4	AL30	VSS		VSS	J11	VSS	
VSS	AL9	VSS		VSS	J13	VSS	
VSS	B13	VSS		VSS	J15	VSS	
VSS	J4	VSS		VSS	T11	VSS	
VSS	K11	VSS		VSS	U22	VSS	
VSS	K13	VSS		VSS	U23	VSS	
VSS	K19	VSS		VSS	U24	VSS	
VSS	K26	VSS		VSS	U27	VSS	

Table 8-49.Processor Ball List by Ball Name (Sheet 8 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
VSS	K27	VSS		VSS	V14	VSS	
VSS	K28	VSS		VSS	V16	VSS	
VSS	K30	VSS		VSS	V18	VSS	
VSS	K4	VSS		VSS	V28	VSS	
VSS	K8	VSS		VSS	V29	VSS	
VSS	L1	VSS		VSS	W13	VSS	
VSS	L13	VSS		VSS	W2	VSS	
VSS	L18	VSS		VSS	W23	VSS	
VSS	L22	VSS		VSS	W25	VSS	
VSS	L24	VSS		VSS	W26	VSS	
VSS	L25	VSS		VSS	W28	VSS	
VSS	L29	VSS		VSS	W30	VSS	
VSS	M28	VSS		VSS	W4	VSS	
VSS	M3	VSS		VSS	W5	VSS	
VSS	N1	VSS		VSS	W6	VSS	
VSS	N13	VSS		VSS	W7	VSS	
VSS	N18	VSS		VSS	Y28	VSS	
VSS	N24	VSS		VSS	Y3	VSS	
VSS	N25	VSS		VSS	Y4	VSS	
VSS	N28	VSS		VSS	T29	VSS	
VSS	N4	VSS		VSSSENSE	B29	PWR	
VSS	N5	VSS		XDP_RSVD_8	A9	XDP	I/O
VSS	N8	VSS		XDP_RSVD_9	D9	XDP	I/O
VSS	P13	VSS		XDP_RSVD_10	C8	XDP	I/O
VSS	P14	VSS		XDP_RSVD_11	B8	XDP	I
VSS	P16	VSS		XDP_RSVD_12	C10	XDP	I/O
VSS	P18	VSS		XDP_RSVD_13	D10	XDP	I/O
VSS	P19	VSS		XDP_RSVD_14	B11	XDP	I/O
VSS	P21	VSS		XDP_RSVD_15	B10	XDP	I/O
VSS	P3	VSS		XDP_RSVD_16	B12	XDP	I/O
VSS	P4	VSS		XDP_RSVD_17	C11	XDP	I
VSS	R25	VSS		XDP_RSVD_0	D12	XDP	I
VSS	R7	VSS		XDP_RSVD_1	A7	XDP	I
VSS	R8	VSS		XDP_RSVD_2	D6	XDP	I
XDP_RSVD_3	C5	XDP	I	DDR_A_DQ_26	AK6	MEM_AD	I/O
XDP_RSVD_4	C7	XDP	I	DDR_A_DQ_27	AJ7	MEM_AD	I/O
XDP_RSVD_5	C6	XDP	I				

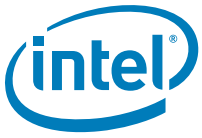


Table 8-49.Processor Ball List by Ball Name (Sheet 9 of 9)

Pin Name	Pin Number	Type	Dir.	Pin Name	Pin Number	Type	Dir.
XDP_RSVD_6	D8	XDP	I				
XDP_RSVD_7	B7	XDP	I/O				
RSVD_3	P2						
RSVD_1	AK29	VSS					

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9 Debug Tool Specifications

The ITP-XDP debug port connector is the recommended debug port for platforms using Intel Atom Processor D400 and D500 Series. Refer to the appropriate Debug Port Design Guide and Platform Design Guide for more detailed information regarding debug tools specifications. Contact your Intel representative for more information.

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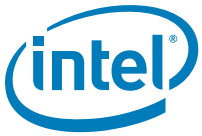

10 Testability

In Intel Atom Processor D400 and D500 Series, testability for Automated Test Equipment (ATE) board level testing has been implemented as JTAG boundary scan.

10.1 JTAG Boundary Scan

The Intel Atom Processor D400 and D500 Series add Boundary Scan ability compatible with the IEEE 1149.1-2001 Standard (Teset Access Port and Boundary-Scan Architecture) specification.

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