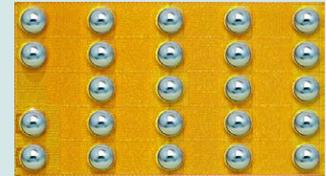


EPC2034 – Enhancement Mode Power Transistor

 V_{DS} , 200 V $R_{DS(on)}$, 10 m Ω I_D , 48 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

| Maximum Ratings | | | |
|-----------------|---|------------|------------------|
| PARAMETER | | VALUE | UNIT |
| V_{DS} | Drain-to-Source Voltage (Continuous) | 200 | V |
| I_D | Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 3^\circ\text{C/W}$) | 48 | A |
| | Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$) | 200 | |
| V_{GS} | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| T_J | Operating Temperature | -40 to 150 | $^\circ\text{C}$ |
| T_{STG} | Storage Temperature | -40 to 150 | |



EPC2034 eGaN® FETs are supplied only in passivated die form with solder bumps. Die Size: 4.6 mm x 2.6 mm

- High Frequency DC-DC Conversion
- Motor Drive
- Industrial Automation
- Class-D Audio

| Thermal Characteristics | | | |
|-------------------------|--|------|--------------------|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.45 | $^\circ\text{C/W}$ |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board | 3.9 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 45 | |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

| Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | | |
|--|--------------------------------|---|-----|-----|-----|------------|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0 \text{ V}$, $I_D = 0.6 \text{ mA}$ | 200 | | | V |
| I_{DSS} | Drain-Source Leakage | $V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$ | | 0.1 | 0.4 | mA |
| I_{GSS} | Gate-to-Source Forward Leakage | $V_{GS} = 5 \text{ V}$ | | 1 | 7 | mA |
| | Gate-to-Source Reverse Leakage | $V_{GS} = -4 \text{ V}$ | | 0.1 | 0.4 | mA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$, $I_D = 7 \text{ mA}$ | 0.8 | 1.4 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS} = 5 \text{ V}$, $I_D = 20 \text{ A}$ | | 7 | 10 | m Ω |
| V_{SD} | Source-Drain Forward Voltage | $I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$ | | 1.8 | | V |

All measurements were done with substrate connected to source.

Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|---|---|-----|-----|------|----------|
| C_{ISS} | Input Capacitance | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ | | 950 | 1140 | pF |
| C_{RSS} | Reverse Transfer Capacitance | | | 2.3 | | |
| C_{OSS} | Output Capacitance | | | 450 | 680 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS} = 0\text{ to }100\text{ V}, V_{GS} = 0\text{ V}$ | | 550 | | |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 750 | | |
| R_G | Gate Resistance | | | 0.5 | | Ω |
| Q_G | Total Gate Charge | $V_{DS} = 100\text{ V}, V_{GS} = 5\text{ V}, I_D = 20\text{ A}$ | | 8.8 | 11 | nC |
| Q_{GS} | Gate to Source Charge | $V_{DS} = 100\text{ V}, I_D = 20\text{ A}$ | | 3 | | |
| Q_{GD} | Gate to Drain Charge | | | 1.8 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 2.2 | | |
| Q_{OSS} | Output Charge | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$ | | 75 | 113 | |
| Q_{RR} | Source-Drain Recovery Charge | | | 0 | | |

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .
 Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1: Typical Output Characteristics at 25°C

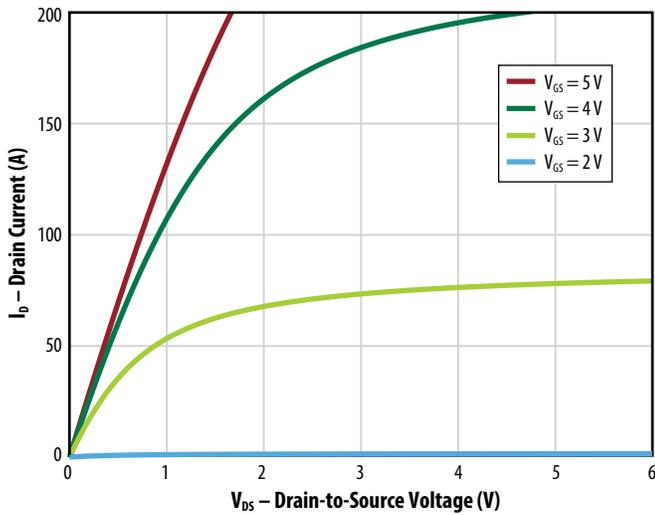


Figure 2: Transfer Characteristics

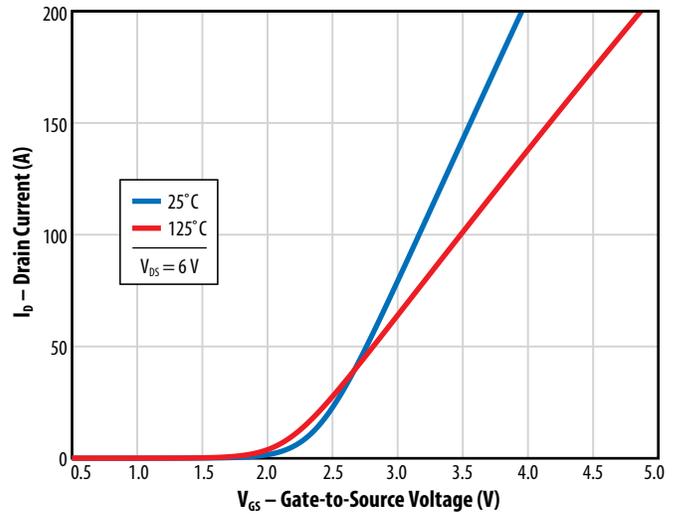


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

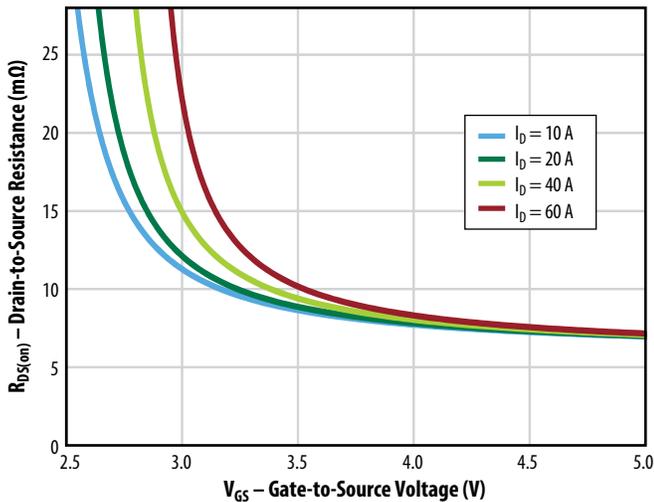


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

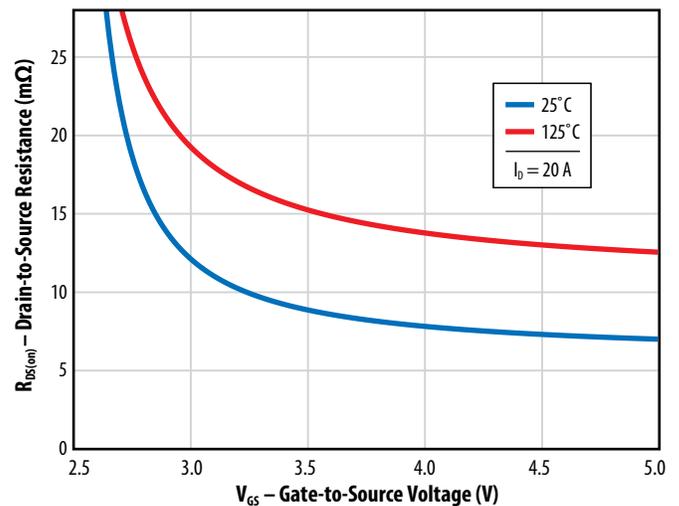


Figure 5a: Capacitance (Linear Scale)

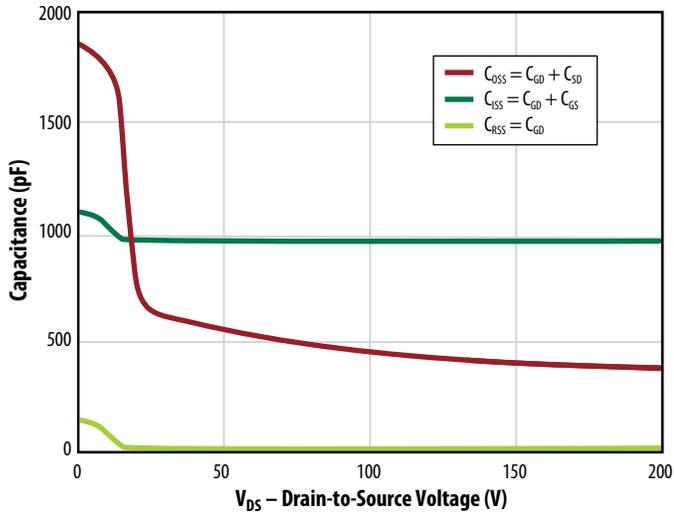


Figure 5b: Capacitance (Log Scale)

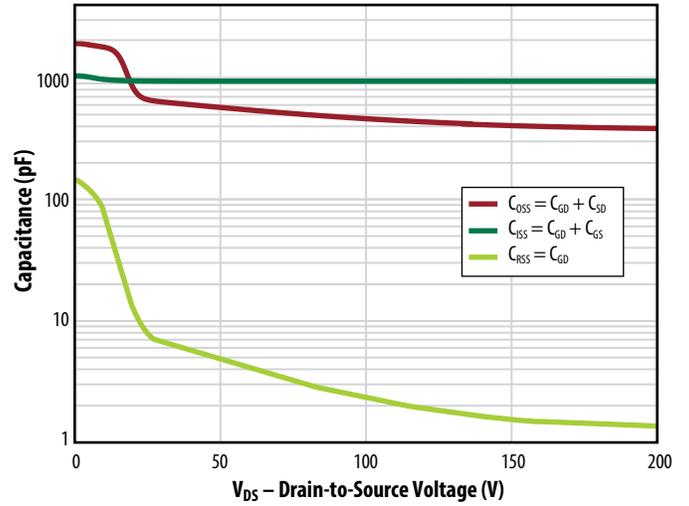


Figure 6: Gate Charge

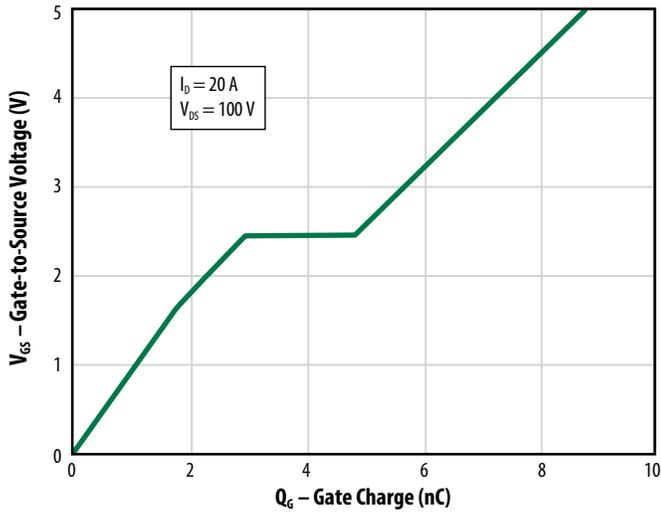


Figure 7: Reverse Drain-Source Characteristics

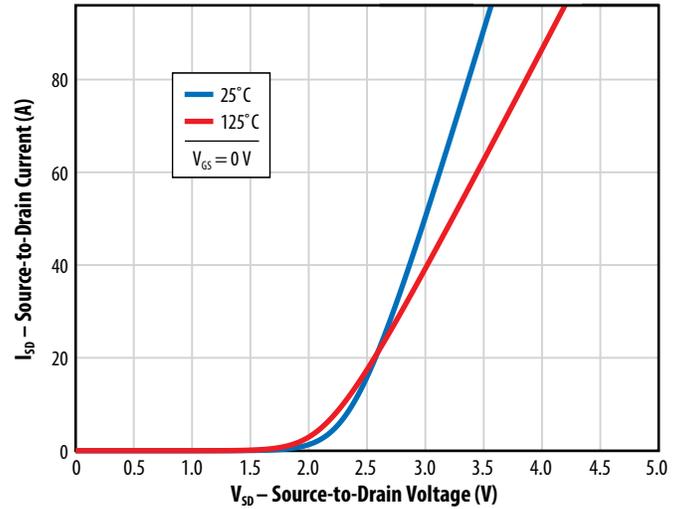


Figure 8: Normalized On-State Resistance vs. Temperature

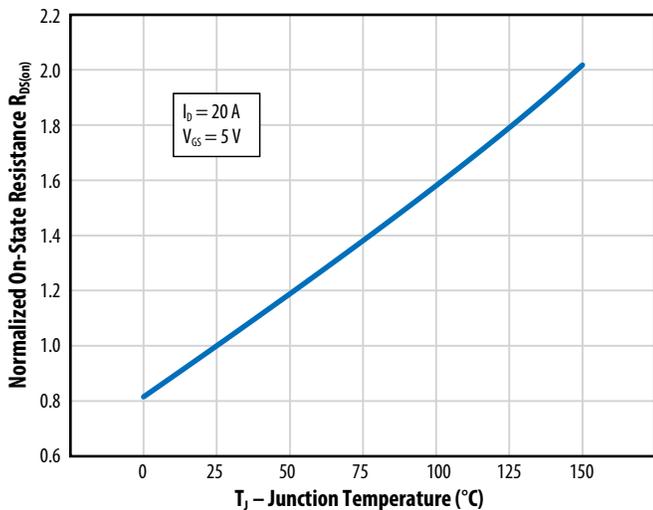
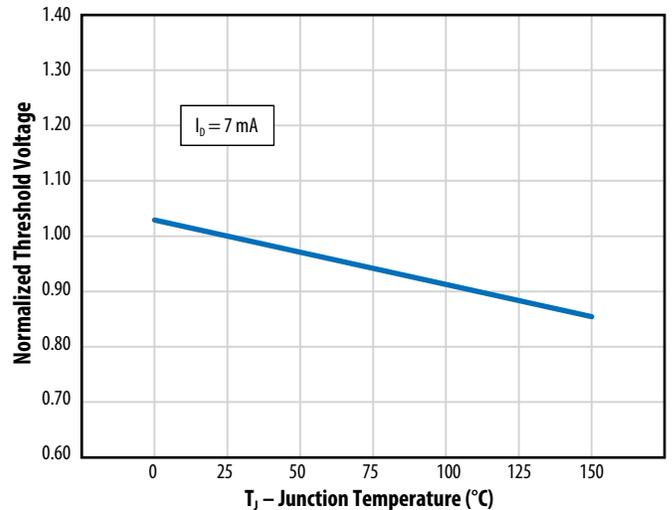


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shorted to source. $T_J = 25^\circ\text{C}$ unless otherwise stated.

Figure 10: Gate Leakage Current

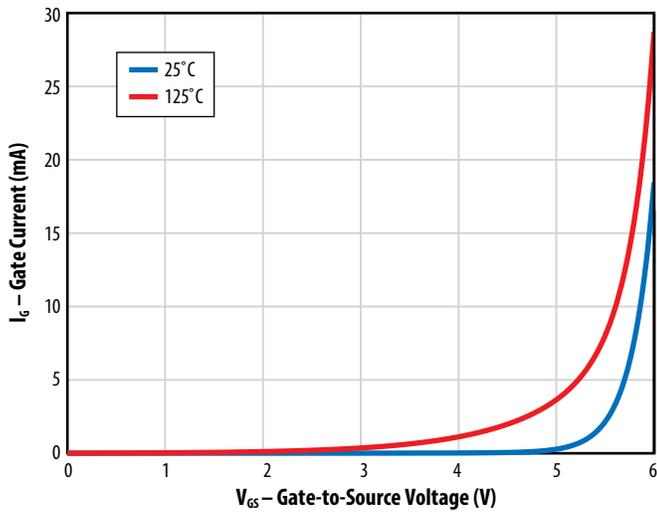


Figure 11: Safe Operating Area

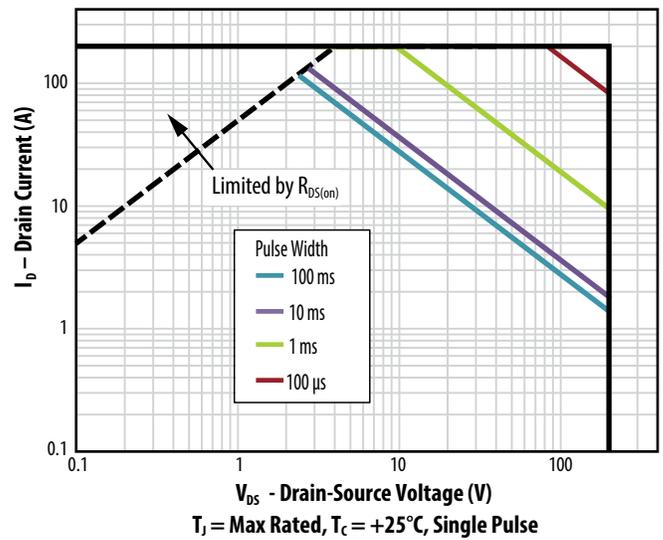
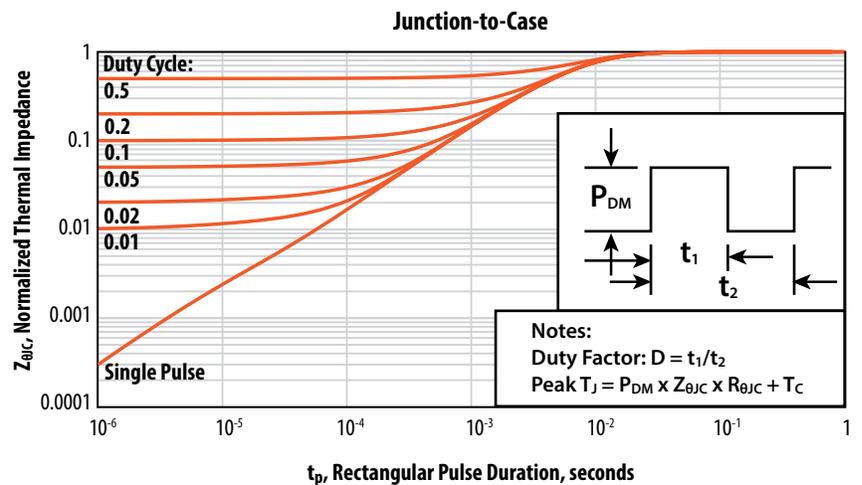
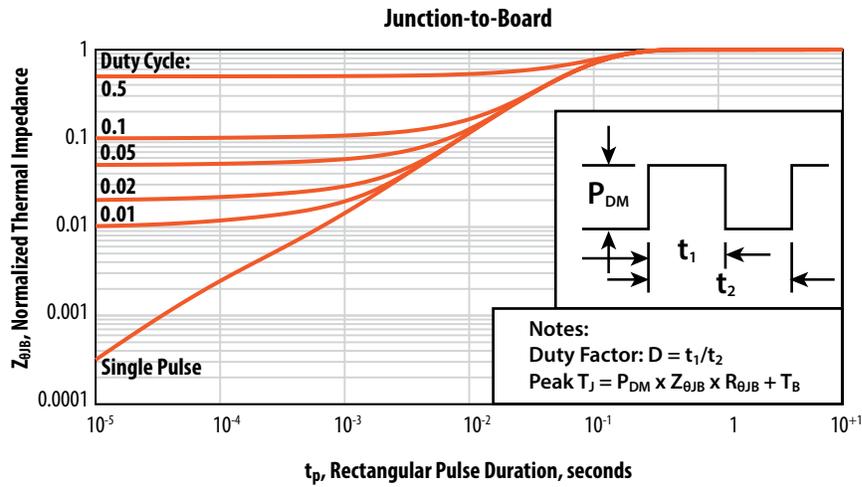
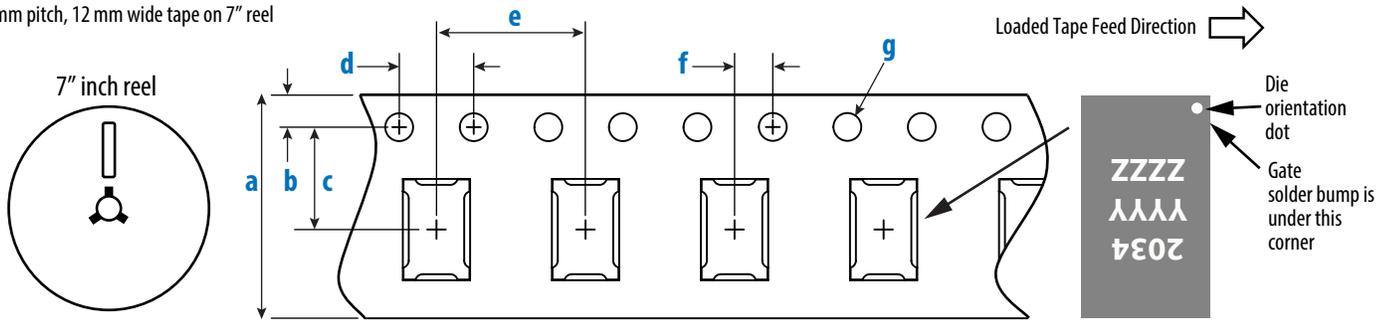


Figure 12: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel



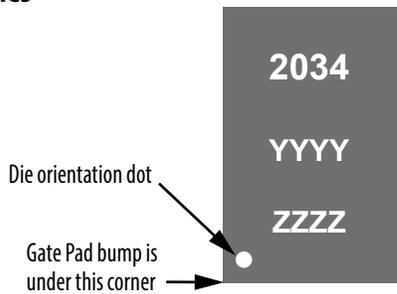
| EPC2034 (Note 1) | Dimension (mm) | | |
|------------------|----------------|-------|-------|
| | Target | MIN | MAX |
| a | 12.00 | 11.90 | 12.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 5.50 | 5.45 | 5.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 8.00 | 7.90 | 8.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |

Die is placed into pocket solder bump side down (face side down)

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

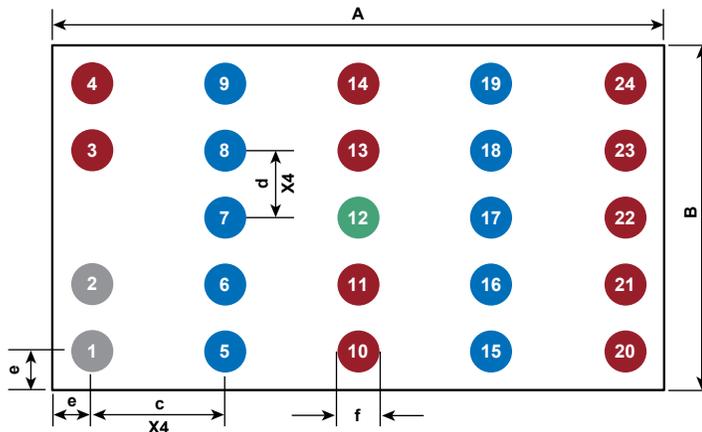
DIE MARKINGS



| Part Number | Laser Markings | | |
|-------------|-----------------------|-------------------------------|-------------------------------|
| | Part # Marking Line 1 | Lot _Date Code Marking Line 2 | Lot _Date Code Marking Line 3 |
| EPC2034 | 2034 | YYYY | ZZZZ |

DIE OUTLINE

Solder Bump View



| DIM | Micrometers | | |
|-----|-------------|---------|------|
| | MIN | Nominal | MAX |
| A | 4570 | 4600 | 4630 |
| B | 2570 | 2600 | 2630 |
| c | 1000 | 1000 | 1000 |
| d | 500 | 500 | 500 |
| e | 285 | 300 | 315 |
| f | 332 | 369 | 406 |

Pads 1 and 2 are Gate;

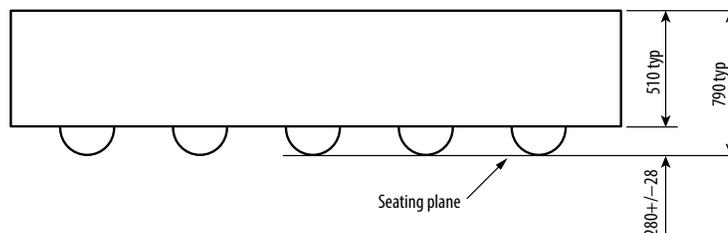
Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;

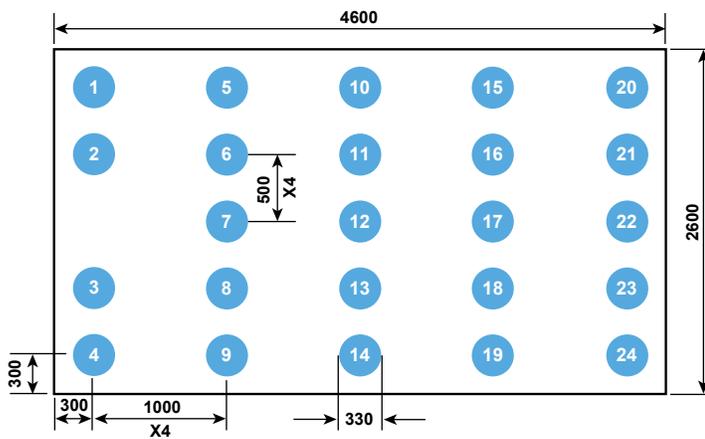
Pad 12 is Substrate*

*Substrate pin should be connected to Source

Side View



RECOMMENDED LAND PATTERN
(units in μm)



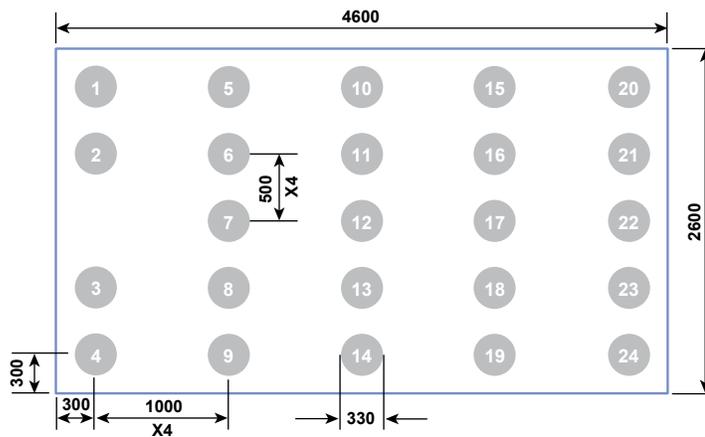
Land pattern is solder mask defined
Solder mask opening is 330 μm
It is recommended to have on-Cu trace PCB vias

Pads 1 and 2 are Gate;
Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;
Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;
Pad 12 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING
(units in μm)

Option 1 : Intended for use with SAC305 Type 4 solder.

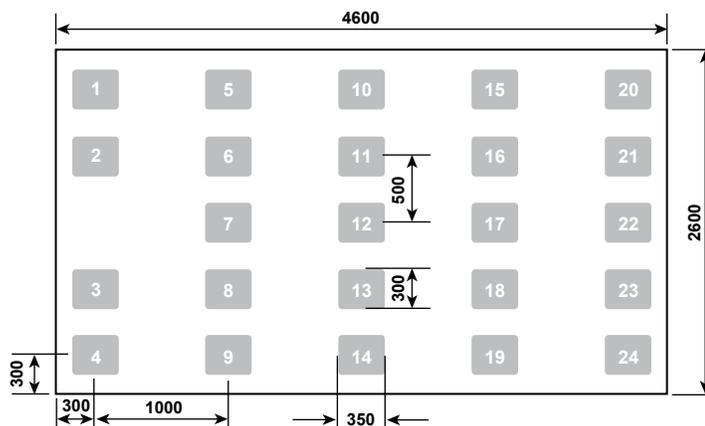


Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Additional assembly resources available at
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

RECOMMENDED STENCIL DRAWING
(units in μm)

Option 2 : Intended for use with SAC305 Type 3 solder.



Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Additional assembly resources available at
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

Errata – EPC2034

Introduction:

This document describes errata to the [EPC2034 eGaN® FET](#) and its datasheet. This document should be used in conjunction with the datasheet and may include updates to the specifications that supersede those stated in the EPC2034 datasheet. Errata may cause a product's behavior to deviate from published specifications.

Errata List:

Input Voltage Clarifications

In the Maximum Ratings table, Maximum V_{DS} is specified at 200 V. For applications purposes, the main input DC supply voltage should be limited to 160 V_{DC} . For transient operation between 160 V and 200 V, please contact EPC at Steve.Colino@epc-co.com

Important Notice:

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