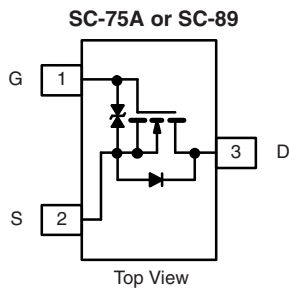


## N-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (mA)
20	0.70 at V <sub>GS</sub> = 4.5 V	600
	0.85 at V <sub>GS</sub> = 2.5 V	500
	1.25 at V <sub>GS</sub> = 1.8 V	350



### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET: 1.8 V Rated
- Gate-Source ESD Protected: 2000 V
- High-Side Switching
- Low On-Resistance: 0.7 Ω
- Low Threshold: 0.8 V (typ.)
- Fast Switching Speed: 10 ns
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

### BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

ORDERING INFORMATION		
Part Number	Package	Marking Code
Si1012R-T1-GE3 (Lead (Pb)-free and Halogen-free)	SC-75A (SOT-416)	C
Si1012X-T1-GE3 (Lead (Pb)-free and Halogen-free)	SC-89 (SOT-490)	A

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20		V	
Gate-Source Voltage	V <sub>GS</sub>	± 6			
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>b</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	600	500	mA
		T <sub>A</sub> = 85 °C	400	350	
Pulsed Drain Current <sup>a</sup>	I <sub>DM</sub>	1000			
Continuous Source Current (Diode Conduction) <sup>b</sup>	I <sub>S</sub>	275	250		
Maximum Power Dissipation <sup>b</sup> for SC-75	P <sub>D</sub>	T <sub>A</sub> = 25 °C	175	150	mW
		T <sub>A</sub> = 85 °C	90	80	
Maximum Power Dissipation <sup>b</sup> for SC-89	P <sub>D</sub>	T <sub>A</sub> = 25 °C	275	250	
		T <sub>A</sub> = 85 °C	160	140	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000		V	

Notes:

- Pulse width limited by maximum junction temperature.
- Surface mounted on FR4 board.

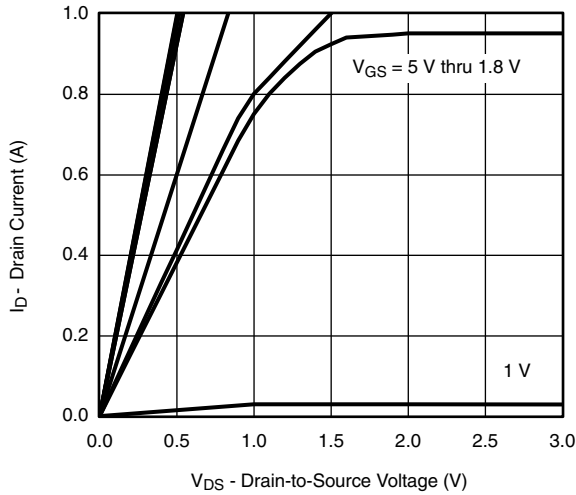
<b>SPECIFICATIONS</b> ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.45		0.9	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$		$\pm 0.5$	$\pm 1.0$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		0.3	100	nA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			5	$\mu\text{A}$
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 4.5\text{ V}$	700			mA
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 600\text{ mA}$		0.41	0.70	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 500\text{ mA}$		0.53	0.85	
		$V_{GS} = 1.8\text{ V}, I_D = 350\text{ mA}$		0.70	1.25	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 400\text{ mA}$		1.0		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 150\text{ mA}, V_{GS} = 0\text{ V}$		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 250\text{ mA}$		750		pC
Gate-Source Charge	$Q_{gs}$			75		
Gate-Drain Charge	$Q_{gd}$			225		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 47\text{ }\Omega$ $I_D \cong 200\text{ mA}, V_{GEN} = 4.5\text{ V}, R_g = 10\text{ }\Omega$		5		ns
Rise Time	$t_r$			5		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall Time	$t_f$			11		

## Notes:

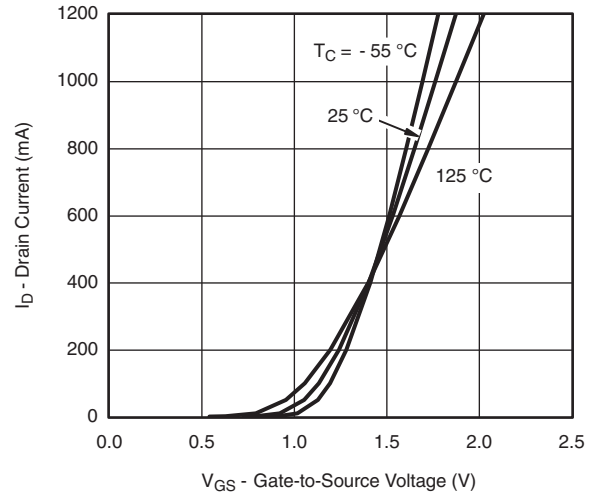
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

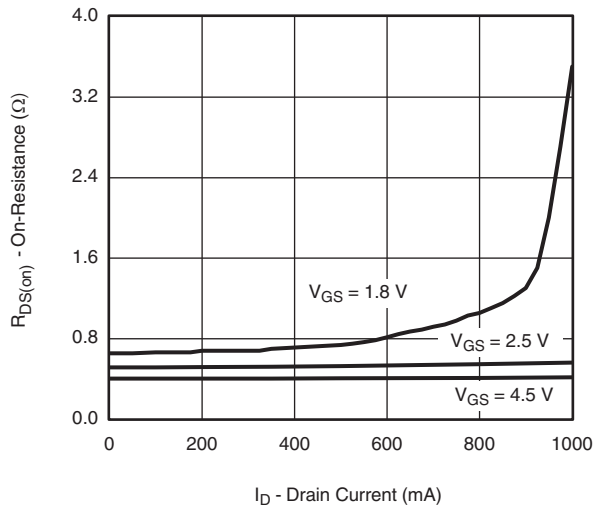
## TYPICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



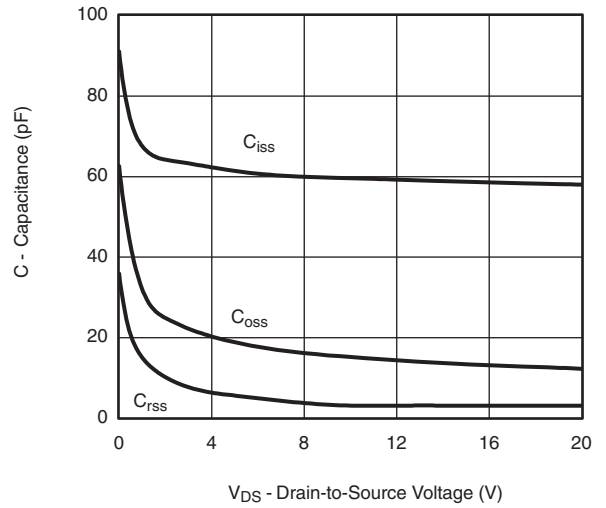
**Output Characteristics**



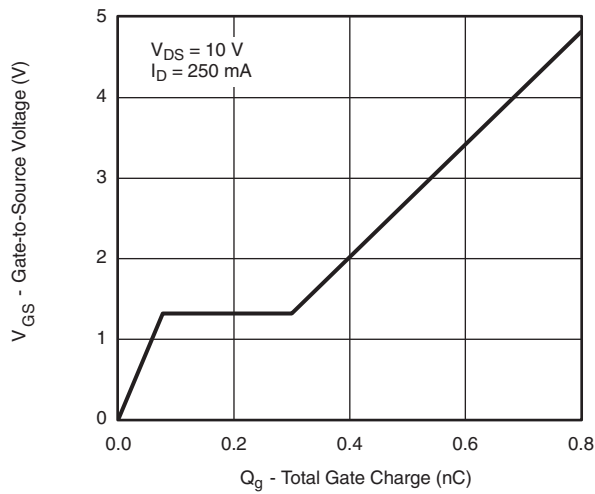
**Transfer Characteristics**



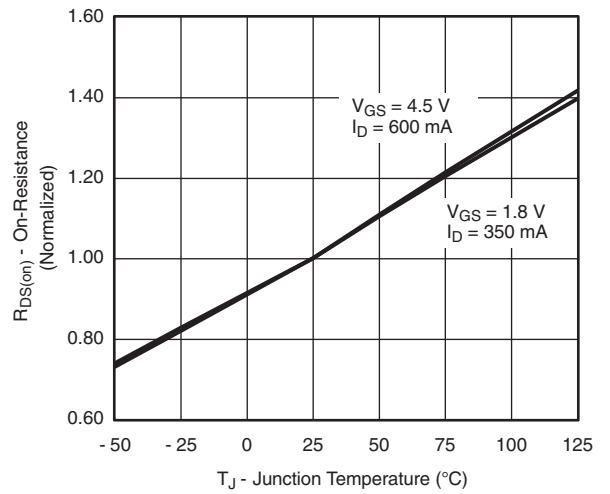
**On-Resistance vs. Drain Current**



**Capacitance**

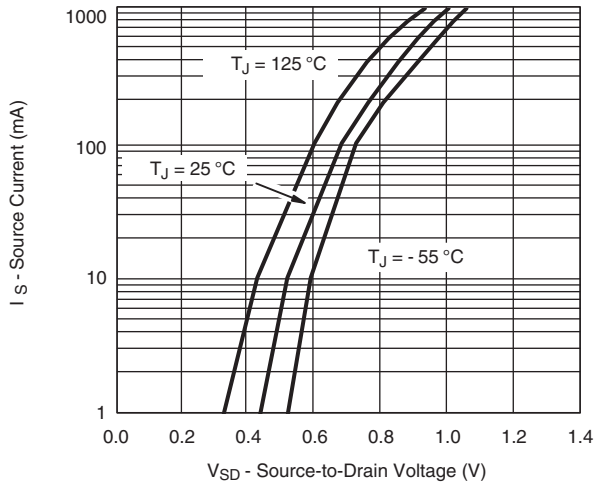


**Gate Charge**

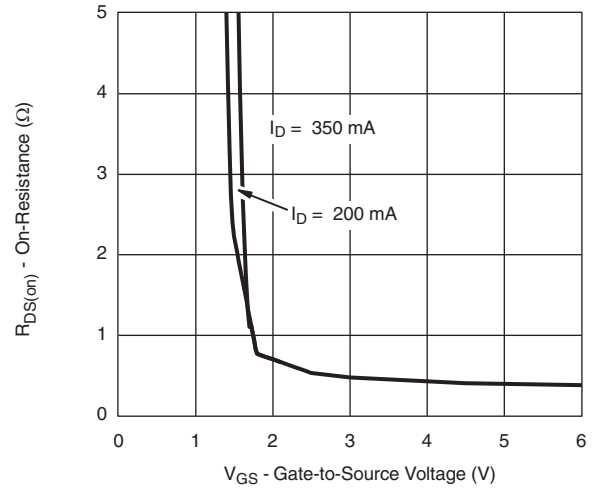


**On-Resistance vs. Junction Temperature**

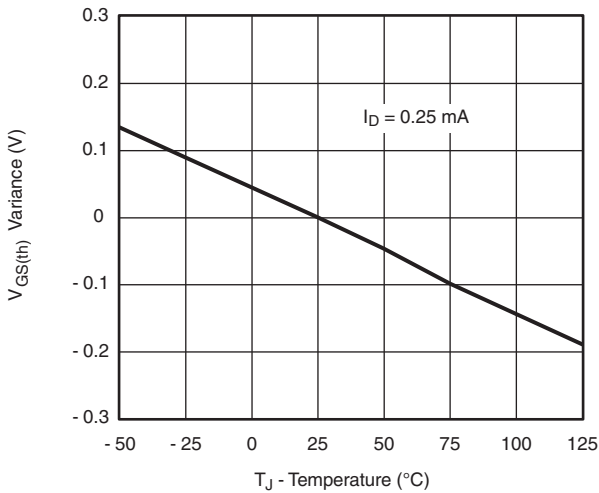
**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



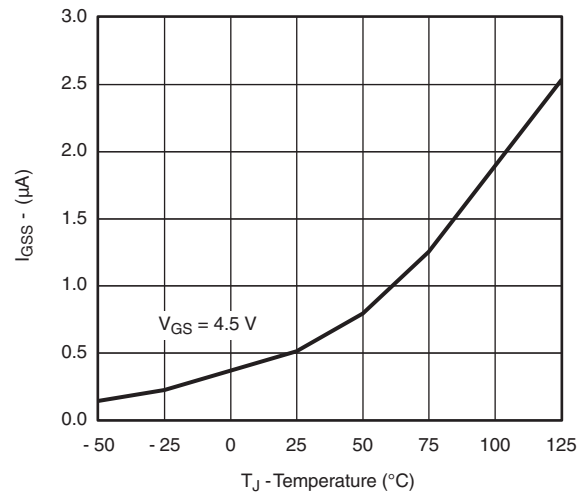
**Source-Drain Diode Forward Voltage**



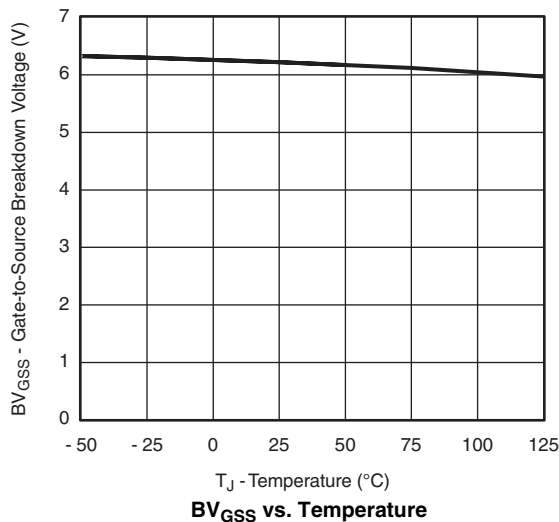
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage Variance vs. Temperature**

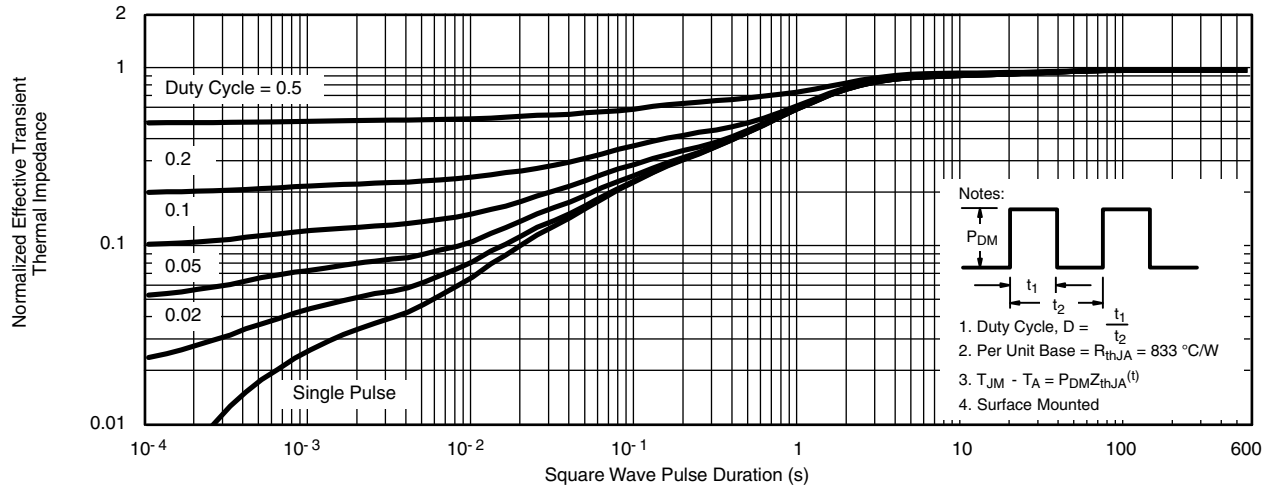


**$I_{GSS}$  vs. Temperature**

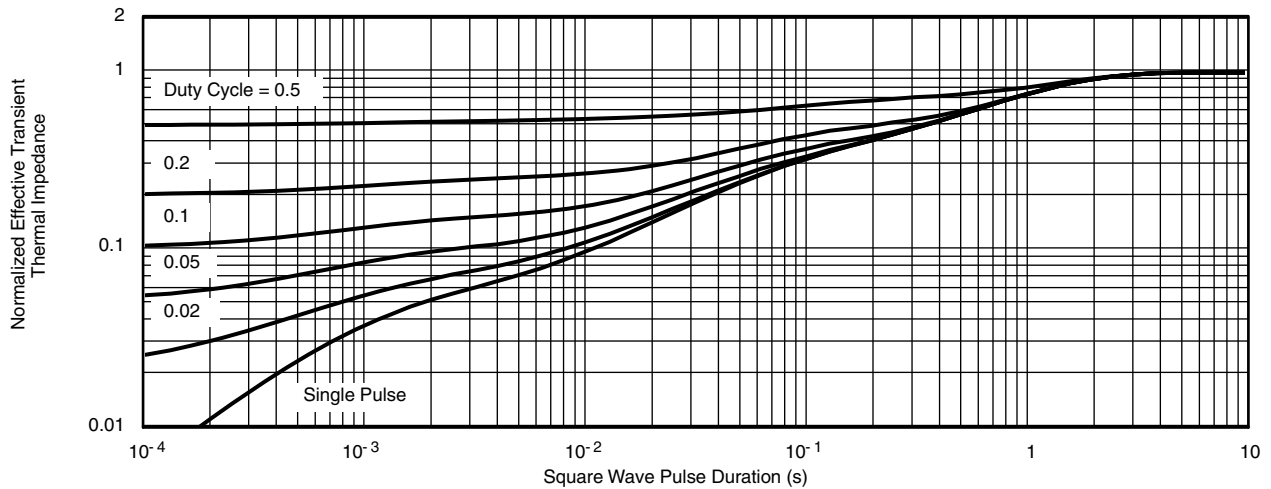


**$BV_{GSS}$  vs. Temperature**

**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient (SC-75A)**

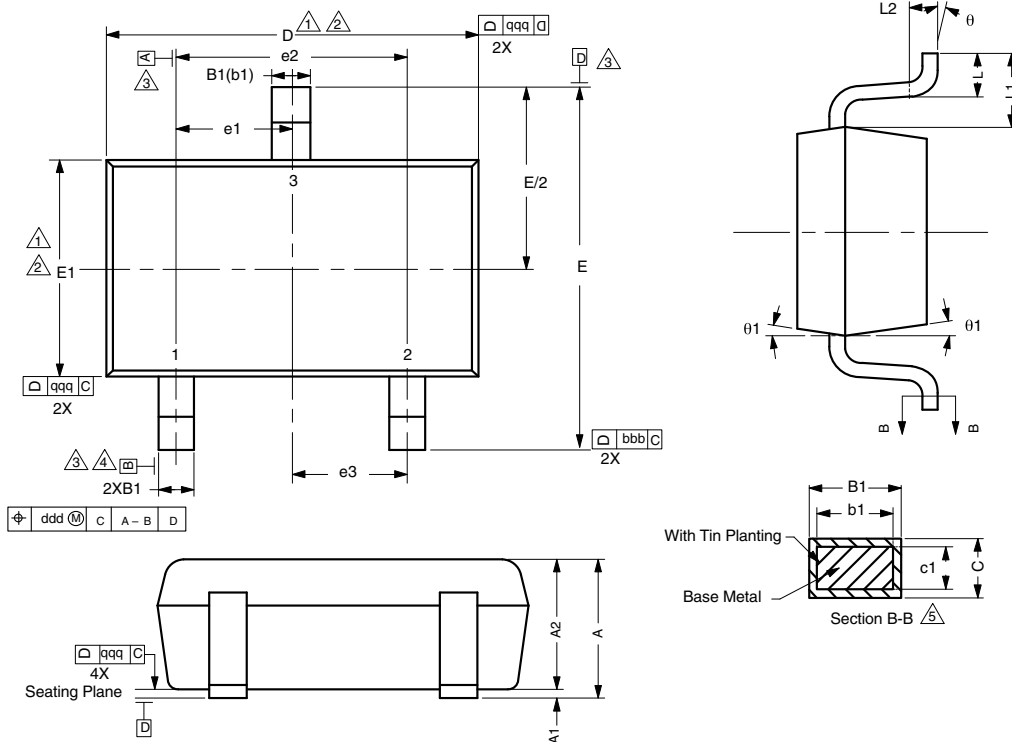


**Normalized Thermal Transient Impedance, Junction-to-Foot**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?71166](http://www.vishay.com/ppg?71166).



SC-75A: 3-LEADS



Notes

Dimensions in millimeters will govern.

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
2. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. Datums A, B and D to be determined 0.10 mm from the lead tip.
4. Terminal positions are shown for reference only.
5. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

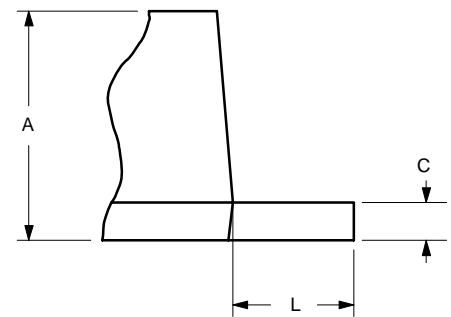
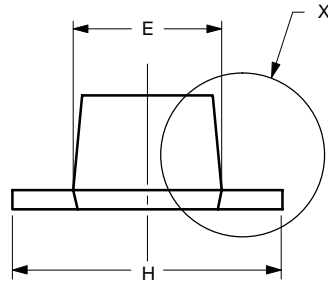
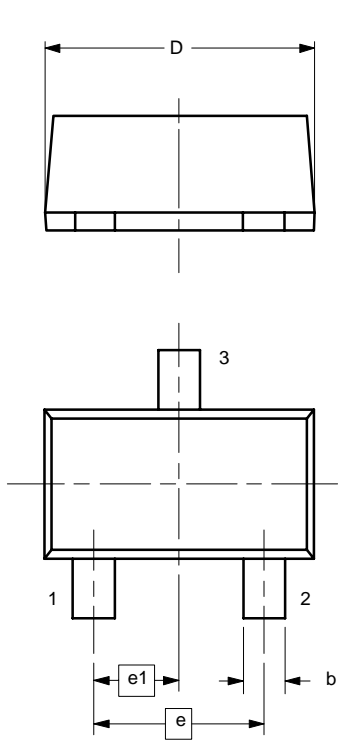
DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	-	-	0.80	
A <sub>1</sub>	0.00	-	0.10	
A <sub>2</sub>	0.65	0.70	0.80	
B <sub>1</sub>	0.19	-	0.24	5
b <sub>1</sub>	0.17	-	0.21	
c	0.13	-	0.15	5
c <sub>1</sub>	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E <sub>1</sub>	0.66	0.76	0.86	1, 2
e <sub>1</sub>	0.50 BSC			
e <sub>2</sub>	1.00 BSC			
e <sub>3</sub>	0.50 BSC			
L	0.15	0.205	0.30	
L <sub>1</sub>	0.40 REF			
L <sub>2</sub>	0.15 BSC			
θ	0°	-	8°	
θ <sub>1</sub>	4°	-	10°	

ECN: E11-2210-Rev. D, 08-Aug-11  
DWG: 5868



SC89-3

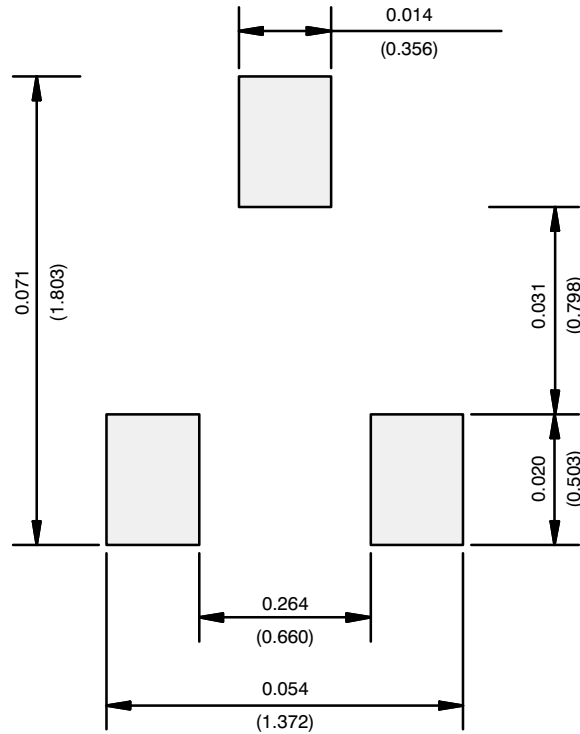


DETAIL X

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	0.60	0.80	0.024	0.031
<b>b</b>	0.23	0.33	0.009	0.013
<b>C</b>	0.10	0.20	0.004	0.008
<b>D</b>	1.50	1.70	0.059	0.067
<b>E</b>	0.75	0.95	0.030	0.037
<b>e</b>	1.00 BSC		0.040 BSC	
<b>e<sub>1</sub></b>	0.50 BSC		0.020 BSC	
<b>H</b>	1.50	1.70	0.059	0.067
<b>L</b>	0.30	0.50	0.012	0.020

ECN: S-03946—Rev. B, 09-Jul-01  
DWG: 5869

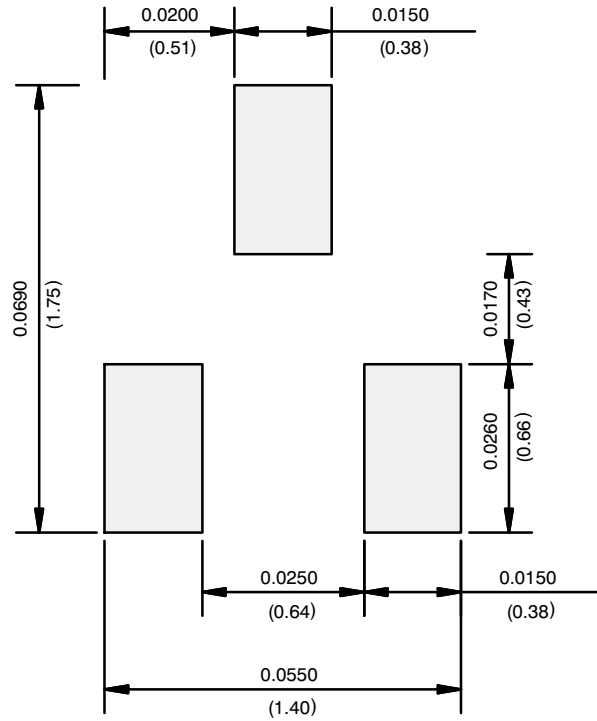
## RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)

## RECOMMENDED MINIMUM PADS FOR SC-89: 3-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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